

Modulating Technique Based Cascaded Multilevel Inverter using Voltage Multiplier

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ABSTRACT: The inclusion of multilevel inverter (MLI) in power electronics is steadily increasing in various industrial sectors. The work in this paper presents symmetrical cascaded H-bridge MLI that can be implemented to reduce the number of dc input power supply and harmonic contents present in it. The involvement of proposed topology with voltage multiplier significantly decreases the number of dc sources, providing equalization of voltage across switches with higher efficiency. The numerous sinusoidal pulse width modulation (SPWM) strategies are analysed to get reduced Total harmonic distortion (T.H.D) in output voltage waveform without using filter. The topologies mainly designed for 9-level (line to line) and further can be extended for N level using $(3N-3)/2$ switches and $(N-1)/4$ dc sources with voltage multiplier. The proposed topology with voltage multiplier for 9-level is simulated for various modulation index using different multicarrier SPWM and additional techniques like trapezoidal, multi-reference, staircase PWM techniques. The results obtained are evaluated using MATLAB/SIMULINK.

KEYWORDS: Multilevel inverter, Voltage multiplier, Multicarrier SPWM, T.H.D.

I. INTRODUCTION

In the last few decades, multilevel inverter has become interest of study in the several industrial sectors. Due to the capability of adapting advantageous features it is more feasible for high voltage high power applications [1]. The main consideration taken in to account while formulating multilevel inverter is the undesirable harmonics and number of switches to be reduced. Plentiful topologies [2][3] so far suggested must cope with following fulfilments,

- a) It should be capable of enduring minimum number of dc input voltage sources and
- b) It should have less switching devices.

In general the performance of an inverter with any switching strategies depends upon the harmonic contents at its output voltage. In multilevel technology there are several PWM modulation strategies, among them multicarrier SPWM technique [4] dominated other techniques due to its feasible characteristics in suppressing harmonic distortion.

In this paper, several cascaded H-bridge topologies [5] with symmetrical dc input source is studied. The comparative study of various topologies is carried out using various different level shifting SPWM techniques. The conventional H-bridge with 9 level using 16 switches [6], 9 level using 11 switches [7], 9 level using 10 switches [8] requires more number of switching devices is depicted in Fig.1(a)-(c). Acquiring high number of switches decreases the efficiency and performance due to switching and conduction losses. Although as depicted in Fig.1 (d), 9 level using 8 switches [9] requires less number of switching devices provided there is unbalance in voltage across each switch. With the sharp contrast to these topologies the disadvantages can be overcome by proposed topology with voltage multiplier [10]. In many drive related applications separate dc sources precludes the use of an inverter, to minimize the number of dc sources voltage multiplier is included [11]. The comparison of various topologies based on number of devices and maximum number of switches ON is shown in table.1.

International Journal of Innovative Research in Science, Engineering and Technology

(A High Impact Factor, Monthly Peer Reviewed Journal)

Vol. 5, Issue 2, February 2016

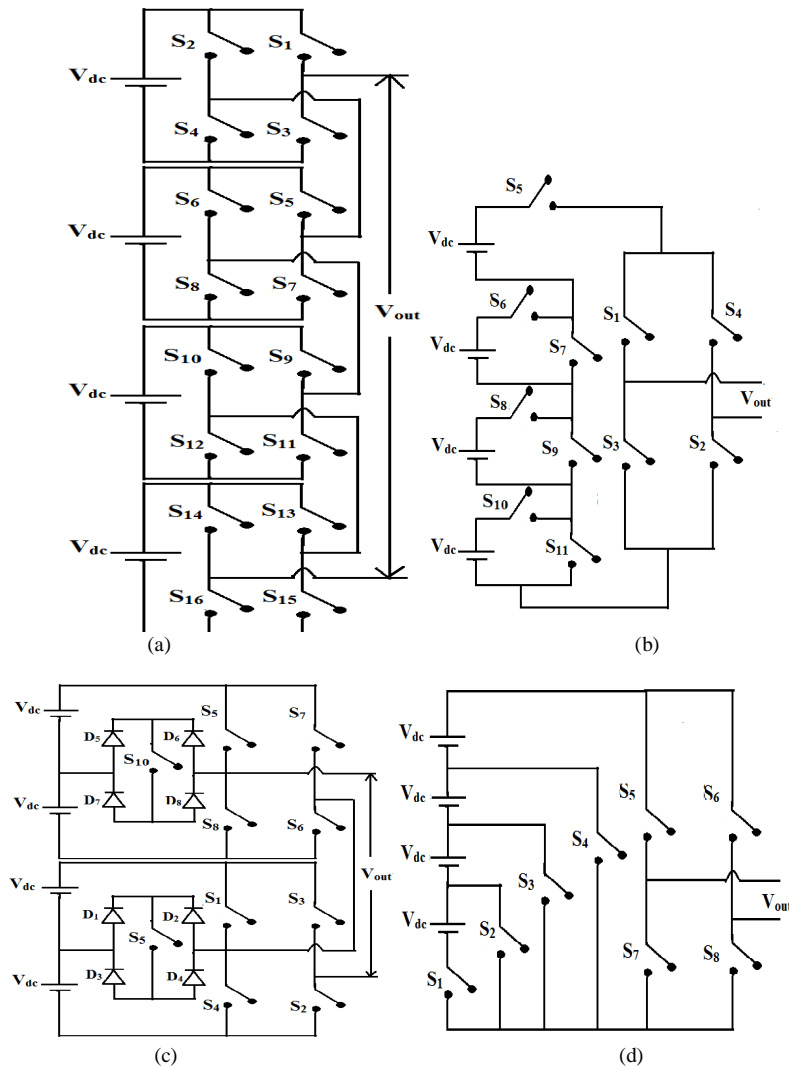


Fig.1 Different Multilevel topologies for 9 level (a) Topology-1 using 16 switch (b) Topology-2 using 10 switch (c) Topology-3 using 10 switch (d) Topology-4 using 8 switch

TABLE-I Comparison of various topologies for 9-level

Topologies	Number of devices				Maximum number of switches ON
	Diodes	Capacitor	Switches	DC sources	
Topology-1	0	0	16	4	8
Topology-2	0	0	11	4	6
Topology-3	8	0	10	4	4
Topology-4	0	0	8	4	3
Proposed topology(without multiplier)	0	0	12	4	6
Proposed topology(with multiplier)	6	6	16	2	6

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II. OPERATION OF PROPOSED CASCADED BRIDGE

The single phase proposed cascaded H-bridge multilevel inverter can be designed for N-levels (line to line) with voltage multiplier as a dc input source. The power circuit for N-level proposed topology is presented in Fig.2 (a)-(b). It requires $(3N-3)/2$ switches and $(N-1)/4$ dc voltage source with voltage multiplier. In this work, the proposed topology is designed for 9-level using level shifting SPWM techniques. The voltage switching pattern for switch S_1 - S_{12} is shown in table.2. Here logic 1 indicates the switch is in 'ON' mode and logic 0 indicates the switch is in 'OFF' mode. Here voltage multiplier acts as voltage source to MLI. Input to bridge 1 (bridge 2) of MLI is provided through voltage multiplier 1 (voltage multiplier 2). For bridge 1 (bridge 2) the voltage source V_1 (V_3) is connected to the multiplied voltage and V_2 (V_4) is connected across the supply of voltage multiplier. The voltage multiplier 1 and 2 consist of complementary switches SW_1 , SW_1^1 and SW_2 , SW_2^1 . It is assumed that at initially even capacitors C_{12} and C_{22} is charged and odd capacitors C_{11} , C_{13} , C_{21} , C_{23} is discharged. Modes of operation for voltage multiplier 1 input to bridge 1 is illustrated below-

Mode1- When switch SW_1 is made 'ON' the capacitor C_{12} is charged through capacitor C_{11} diode D_{12} .

Mode2- When switch SW_1 is made 'OFF' the capacitor C_{12} and C_{13} is charged through diode D_{11} and D_{13} from input supply and capacitor C_{12} .

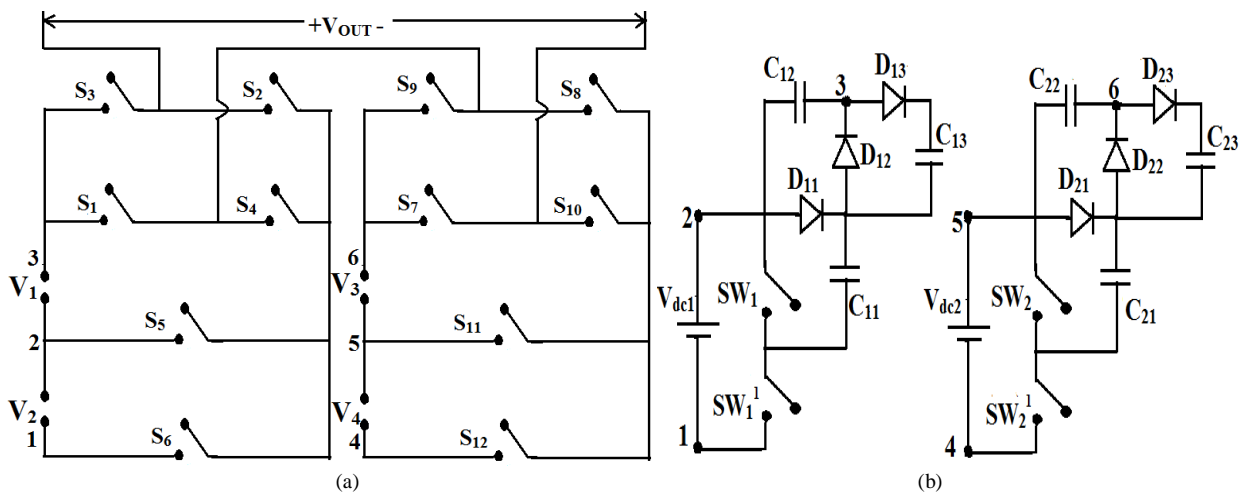


Fig.2 Proposed topology with voltage multiplier (a) Proposed MLI (b) Voltage multiplier 1 and Voltage multiplier 2

TABLE-II Switching table

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}	VOLTAGE LEVELS
0	0	1	1	0	1	0	0	1	1	0	1	$(V_1+V_2+V_3+V_4)$
0	0	1	1	0	1	0	0	1	1	1	0	$(V_1+V_2+V_3)$
0	0	1	1	0	1	1	0	1	0	0	0	(V_1+V_2)
0	0	1	1	1	0	1	0	1	0	0	0	(V_1)
0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	0	1	0	1	0	1	0	0	0	$-(V_1)$
1	1	0	0	0	1	1	0	1	0	0	0	$-(V_1+V_2)$
1	1	0	0	0	1	1	1	0	0	1	0	$-(V_1+V_2+V_3)$
1	1	0	0	0	1	1	1	0	0	0	1	$-(V_1+V_2+V_3+V_4)$

International Journal of Innovative Research in Science, Engineering and Technology

(A High Impact Factor, Monthly Peer Reviewed Journal)

Vol. 5, Issue 2, February 2016

The gate pulse is provided to switches through gate driver circuitry using multicarrier or level shifting SPWM techniques. Moreover the level shifting SPWM comprises of three main strategies which includes-

- 1] Phase disposition pulse width modulation (PDPWM)
- 2] Phase opposition disposition pulse width modulation (PODPWM)
- 3] Alternate phase opposition disposition pulse width modulation (APODPWM)

Additionally, the another PWM technique includes-

- 1] Trapezoidal pulse width modulation (TPWM)
- 2] Multi-reference pulse width modulation (MRPWM)
- 3] Staircase pulse width modulation (STPWM)

In this SPWM techniques the power inverter switches is made ON and OFF state by continuously comparing high frequency f_c triangular wave (carrier) with low frequency f_r sinusoidal wave (reference).

The modulation index for SPWM Technique is the ratio of Amplitude of reference wave (A_R) to the product of number of positive and negative level with amplitude of carrier wave (A_C).

$$\text{Modulation Index} = \frac{A_R}{\frac{(N-1)}{2} \times A_C} \quad (1)$$

In terms of frequency,

$$\text{Modulation Index} = \frac{f_R}{f_c} \quad (2)$$

The output voltage obtained from MLI is periodic waveform superposition of fundamental and harmonic components. The frequency of each harmonic component is integral multiples of fundamental component. To indicate odd and even harmonic total harmonic distortion (T.H.D) is introduced. The percentage T.H.D can be calculated as-

$$\% \text{ T.H.D} = \frac{\sqrt{\sum_{n=2,3,\dots}^{\infty} V_n^2}}{V_1} \quad (3)$$

The comparative study of total harmonic distortion is carried out using various SPWM techniques for different modulation index. The comparison of percentage T.H.D and modulation index are shown in table.3 based on the result obtained using SIMULINK. The percentage T.H.D is minimum for PDSPWM (14.03%) and maximum for STPWM (16.54%) with modulation index 1. Also the variation of T.H.D and modulation index is plotted in graph.1.

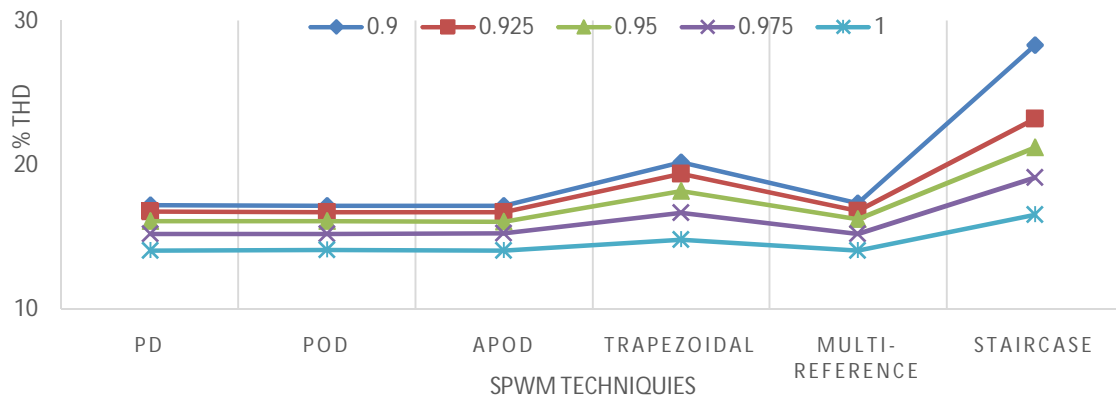
TABLE-III Comparison in terms of total harmonic distortion percentage

Modulation Index	% of Total Harmonic Distortion					
	PDSPWM	PODSPWM	APODSPWM	TPWM	MRPWM	STPWM
1	14.03	14.09	14.04	14.80	14.03	16.54
0.975	15.19	15.21	15.25	16.65	15.20	19.09
0.950	16.10	16.07	16.05	18.15	16.21	21.18
0.925	16.75	16.76	16.71	19.35	16.81	23.17
0.9	17.19	17.16	17.15	20.16	17.33	28.28

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Graph.1 Variation T.H.D and modulation index

III.SIMULATION RESULT

The proposed topology with voltage multiplier is designed for 9 level (line to line) having symmetrical voltage source $V_1=V_2=V_3=V_4=12V$. The electrical parameter values for proposed topology are depicted in table.3 and simulated using MATLAB/SIMULINK. The output voltage and current waveform for 9 level with voltage multiplier for R-load is shown in Fig.3. Voltage across switches S_1-S_6 and switches S_7-S_{12} is shown in Fig.4(a)-(b). It is noted that maximum voltage appears across switches S_1-S_4, S_7-S_{10} , switches S_5, S_{11} has minimum voltage and switch S_6, S_{12} has negative voltage value. The percentage T.H.D is measured using Fast Fourier Transform (FFT) and simulated for various SPWM techniques (viz. PDPWM, PODPWM, APODPWM, TPWM, MRPWM, STPWM) for modulation index 1. The percentage T.H.D is reduced for PDPWM technique depicted in Fig.5.

TABLE-III Parameter values

Parameters	Values
Input Voltage	12V
Output Voltage	48V
Output Power	250W
Switching frequency (Sinusoidal Wave)	50Hz
Switching frequency (Triangular wave)	5KHz

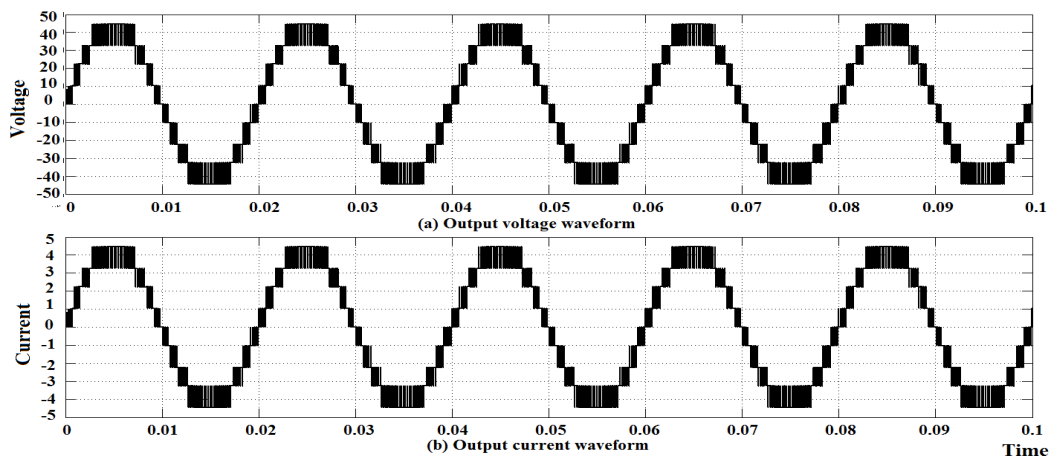


Fig.3 Output voltage and current waveform

International Journal of Innovative Research in Science, Engineering and Technology

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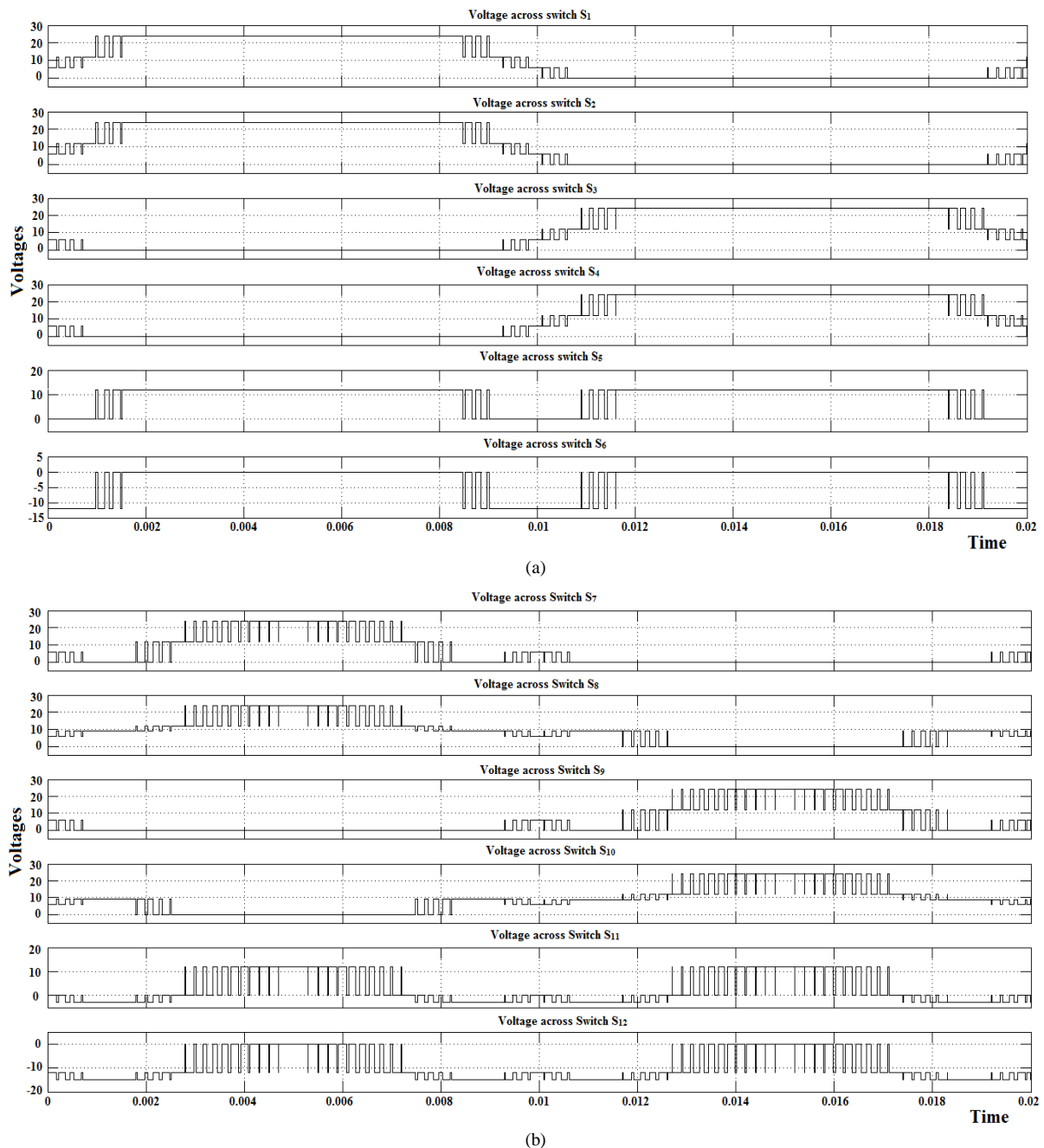


Fig.4 Voltage across switches (a) Switches S₁-S₆ (b) Switches S₇-S₁₂

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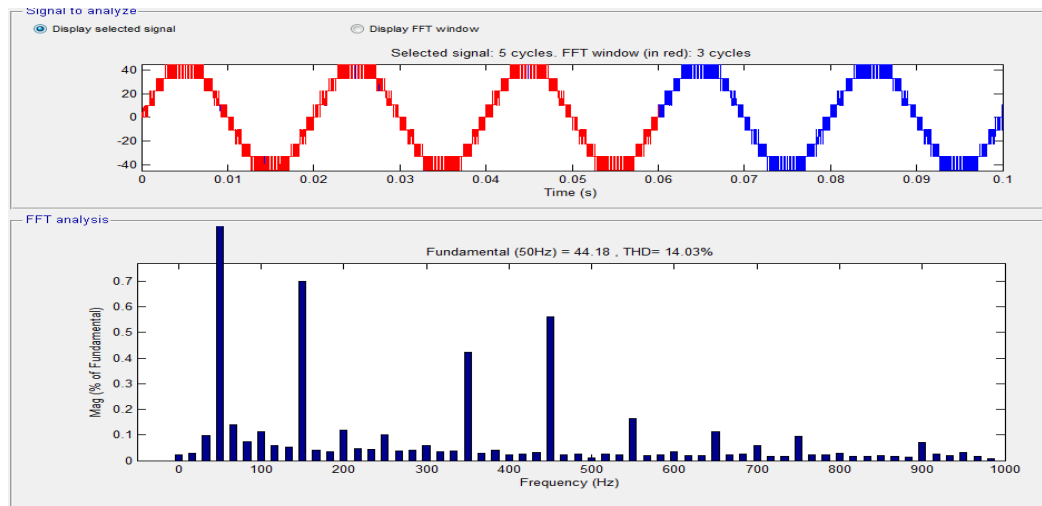


Fig.5 THD response using PDSPWM

IV. CONCLUSION

This paper presents 9level proposed cascaded H-bridge multilevel inverter with voltage multiplier having reduced number of voltage sources than other topologies. The T.H.D (performance factor) is studied and verified by using different PWM techniques. It is found that for resistive load PDSPWM provides appreciable reduced T.H.D of 14.03% for modulation index 1 without filter. Due to balanced distribution of voltage across switches, the efficiency of device is improved with minimum switching and conduction losses.

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