

# International Journal of Innovative Research in Science, Engineering and Technology

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## Multi Valued Logic Based Design of Quaternary Adders in VHDL

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**ABSTRACT:** Small Silicon Area, Higher speed and low power consumption are the desired feature of any circuit, due to the increasing need of portability in devices. Adders form an inevitable part of any system because they are the most basic units. Design of logic circuits using binary logic is limited by the number of interconnections. Multi Valued logic gives us an extension to the binary logic where any position can have more than two values. This paper reviews the need of Multi valued logic and the implementation of the half and full adders using quaternary logic and simulated on Xilinx ISE Design Studio 13.1

**KEYWORDS:** Multi Valued Logic, Quaternary Adders, VHDL, Xilinx

### I. INTRODUCTION

In the world of computers where the dealings are with strings of 0's and 1's, simply because it dictates the two-valued nature of switching primitives of which the machines are made up of. Considerable advancements have made higher radix systems possible even if Decimal schemes are currently out of reach. In many computers and other kinds of processors, adders are used not only in the arithmetic logic units, but also in other parts of the processor, where they are used to calculate addresses, table indices, increment and decrement operators, and similar operations.

Since the speed of the digital processor depends heavily on the speed of the adders used in the system. In the past, one of the major challenges for the VLSI Designer was to reduce silicon chip area, and then in the next step the speed was targeted to achieve faster calculations. Speed of operation is one of the major constraints in designing DSP processors. From the various adders available the speed of the adder depends on how fast the carry is propagated. Using multivalued logic the times carry is generated and propagated is reduced to one half because of the no of states being increased from binary to quaternary.

#### A. Basic Analysis for performance

Three major source of power consumption exists in CMOS circuits:

- 1) Switching Power/ Dynamic Power: Power consumed by the circuit node capacitances during transistor switching
- 2) Short Circuit Power: Power consumed because of the current flowing from power supply to ground during transistor switching.
- 3) Static Power: Static power is power consumed while there is no circuit activity maybe due to leakages and reversed biased PN Junction

The time delay depends on size of transistors, number of transistors used, logic depth, parasitic capacitance and capacitance due to intercell and intracell routing and also on number of inversion levels. Power dissipation depends on switching activity, the number and size of transistors, node capacitance, wiring complexity etc.

$$P_{avg} = P_{static} + P_{dynamic} + P_{short-circuit}$$

The power delay product is a measure of efficiency in an adder circuit. There is a trade-off between power dissipation and speed and is very important when low power operations are needed and is given by

$$PDP = Power * DELAY$$

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## Multi Valued Logic

Multi-value logic is defined as a non-binary logic and involves the switching between more than two states. Multi-valued logic means instead of assuming one of the two states as per in binary logic, signal may assume one of more than two states, for instant 4 states. There are many ways in which quaternary adders using multivalve logic can be designed. In voltage mode multi valued logic, current mode multi valued logic. The advantage of multi valued logic is the injection of more than two levels of signal into a single wire leads to lower number wires in data bus for the same range of data. Voltage mode circuits are preferred because of benefits of the power consumption. A large majority of the power is consumed only during the logic level switching

## II. RELATED WORK

Quaternary full adders based on output generator sharing are proposed by Hirokatsu with reduction in delay and power [1] Design of Some Useful Logic Blocks Using Quaternary Algebra [2] form the basis of this paper.

### A. Implementation of Quaternary Half Adders (QHA)

Addition can be performed in a number of ways in quaternary logic, direct addition can be done or addition by conversion i.e. first a conversion of the quaternary value is done to binary logic and addition is done in Binary Logic and the output is converted back to quaternary logic.

Table 1: Truth Table of Quaternary Half Adder

INPUTS		OUTPUTS	
X	Y	Sum	Carry
0	0	0	0
0	1	1	0
0	2	2	0
0	3	3	0
1	0	1	0
1	1	2	0
1	2	3	0
1	3	0	1
2	0	2	0
2	1	3	0
2	2	0	1
2	3	1	1
3	0	3	0
3	1	0	1
3	2	1	1
3	3	2	1

### B. Idea of working of a Quaternary Half Adder

The adder is like counting of digits in a circular approach. In this the number to be added is the number of times a change in level happens to the number which it was added to. Also the number of times the levels cross the '0' mark a carry is generated.

For Eg: 2 is the number to be added (y) to 3 (x). At 3 the jump of 2 levels i.e 3 to 0 and 0 to 1 happens. So the level reached is 1 and because it crossed 0 once the carry generated is 1.

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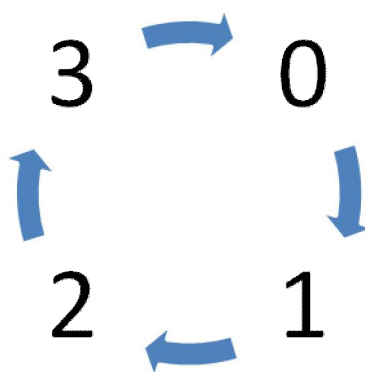


Figure 1: Circular Approach for Quaternary Adders

## C. Quaternary Full Adder

The proposed quaternary full adder is constructed using quaternary half adder. The block diagram of quaternary full adder is shown

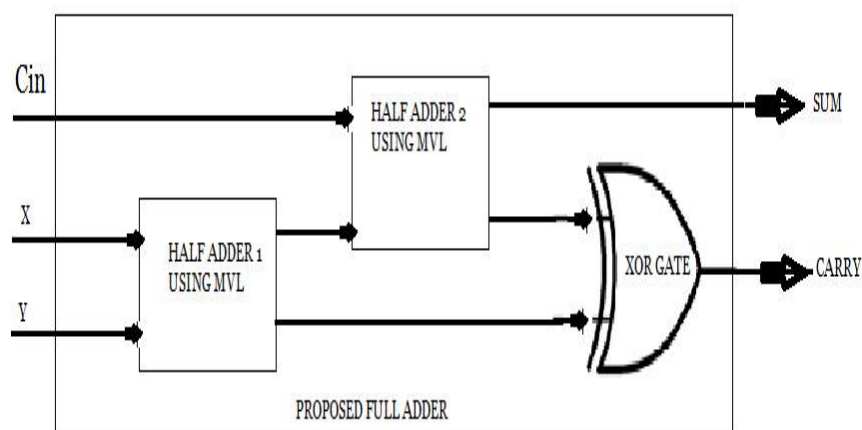


Figure 2: Concept of a Full Adder

The Quaternary Full adder is constructed by using two half adders and one XOR gate in a similar way as a conventional full adder. The first quaternary half adder is given with the two quaternary inputs X and Y. The second quaternary half adder is given one input as Cin and the other is the sum output of the first half adder. The sum output of the second half adder gives the sum of QFA. The carry output of the first half adder is given as one input to the XOR gate and the carry output of the second half adder is the second input to the XOR gate to get the carry output of the proposed full adder. The truth table of a Quaternary Full Adder for carry = 0 and carry = 1 is given in table 2 and 3 respectively.

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Table 2: Truth table of QFA with Carry = 0

INPUTS			OUTPUTS	
Cin	X	Y	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	0	2	2	0
0	0	3	3	0
0	1	0	1	0
0	1	1	2	0
0	1	2	3	0
0	1	3	0	1
0	2	0	2	0
0	2	1	3	0
0	2	2	0	1
0	2	3	1	1
0	3	0	3	0
0	3	1	0	1
0	3	2	1	1
0	3	3	2	1

Table 3: Truth table of QFA with Carry = 1

INPUTS			OUTPUTS	
Cin	X	Y	Sum	Carry
1	0	0	1	0
1	0	1	2	0
1	0	2	3	1
1	0	3	0	0
1	1	0	2	0
1	1	1	3	0
1	1	2	0	1
1	1	3	1	1
1	2	0	3	0
1	2	1	0	1
1	2	2	1	1
1	2	3	2	1
1	3	0	0	1
1	3	1	1	1
1	3	2	2	1
1	3	3	3	1

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## III. SIMULATION RESULTS

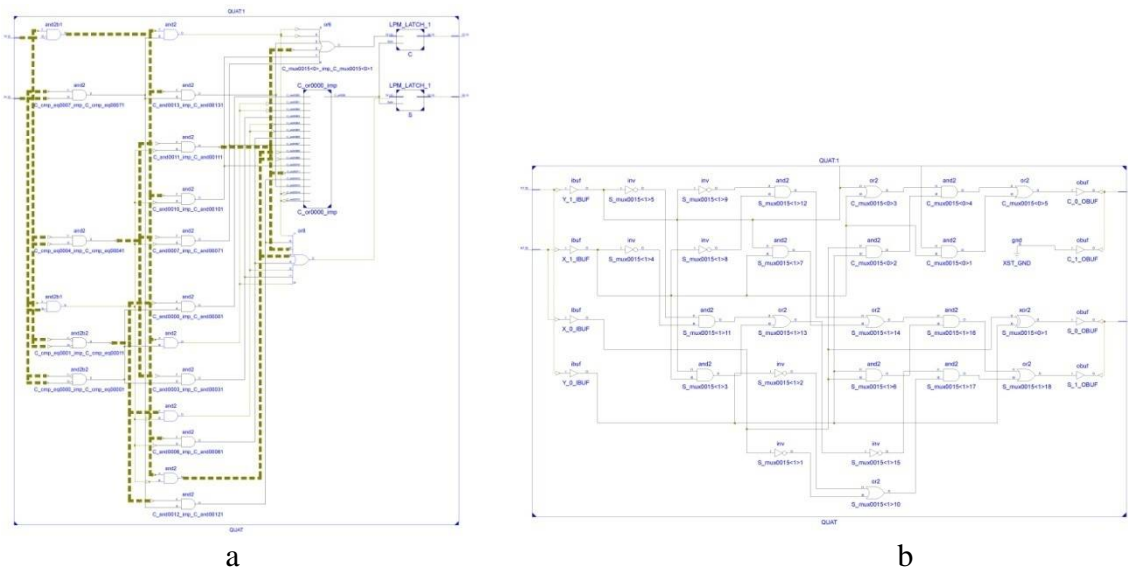


Figure 3: (a) Schematic Symbol of Quaternary Half Adder created in Xilinx.  
(b) Technology Schematic Symbol of Quaternary Half Adder created in Xilinx.

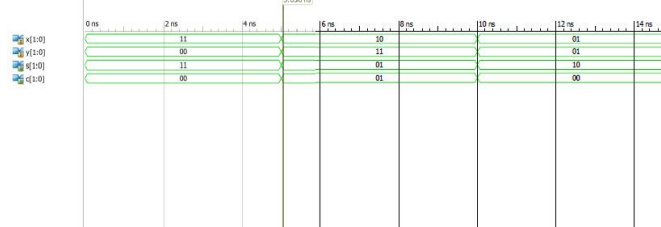


Figure 4: Output Waveform of Quaternary Half Adder in Xilinx

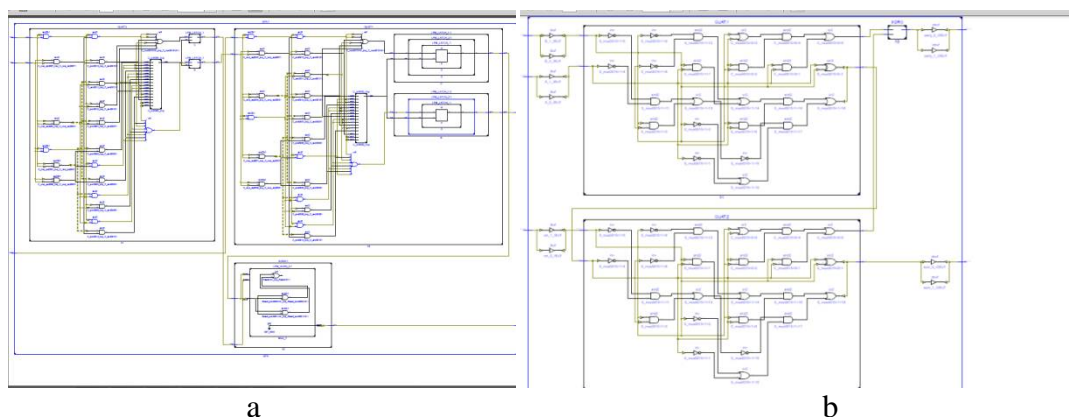


Figure 5: (a) Schematic Symbol of Quaternary Full Adder created in Xilinx.  
(b) Technology Schematic Symbol of Quaternary Full Adder created in Xilinx.

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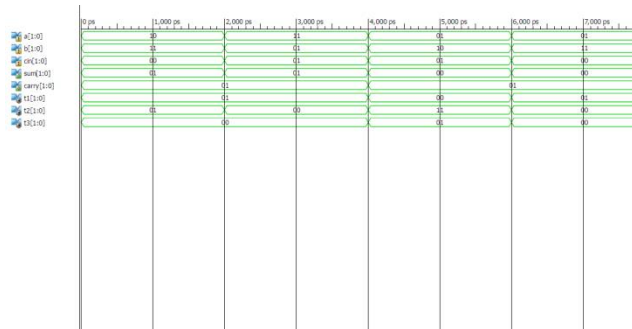


Figure 6: Output Waveform of Quaternary Full Adder in Xilinx

## IV. CONCLUSION

The QFA using QHA's is capable of transmitting more information than the binary system. The simulated output waveform results of the Quaternary adders are obtained and verified from the truth tables. There are several advantages of Quaternary Full Adders using MVL like less wiring complexity, more computational ability in the areas like DSP, Communication and Memory Elements.

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