

Implementation of Frequency and Phasor Measurement of Input AC Signal on FPGA

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ABSTRACT: Frequency and phasor measurement of input ac signal helps in monitoring and analysing the power system dynamics. This paper discusses the implementation of a system to measure frequency, input voltage and phase of input ac signal. Quadrature sampling technique is used to measure the magnitude and phase of input signal. Frequency is measured using zero crossing detection. Modules to measure the Root Mean Square (RMS) value, phase and frequency of the input voltage are developed in Verilog HDL and implemented on Field Programmable Gate Array (FPGA). Measured values of frequency, phase and RMS voltage are displayed on Liquid Crystal Display (LCD).

KEYWORDS: PMU, FPGA, RMS, ADC, ZCD, LCD.

I. INTRODUCTION

Frequency of a signal is a rate at which that signal repeats itself. Electrical and electronic devices are designed to operate at particular frequency. Change in the input frequency can damage these device. Thus measurement of frequency is helpful to improve the efficiency and performance of these devices.

Phasor of a sinusoidal wave is defined as a complex equivalent with complex modulus and complex phase angle representing the amplitude and phase angle of the cosine wave respectively. Sinusoidal signal $x(t)$ and its phasor can be expressed as equation (1) and (2) respectively.

$$x(t) = X_m \cos(\omega t + \phi) \quad (1)$$

$$X = \frac{X_m}{\sqrt{2}} e^{j\phi} \quad (2)$$

$$X = \frac{X_m}{\sqrt{2}} (\cos\phi + j\sin\phi) \quad (3)$$

where X_m is amplitude of the wave, ω is angular frequency, t is time and ϕ is phase angle.

Synchrophasor or synchronized phasor is a phasor estimated with respect to common time reference. Synchrophasor representation of equation (1) is given by X in equations (2) and (3), where ϕ is the instantaneous phase at the nominal frequency of system synchronized to Coordinated Universal Time (UTC).

IEEE Std C37.118.1TM-2011 is a standard for synchrophasor measurement in power systems and describes various requirements for synchronized measurement. Phasor Measurement Unit (PMU) is a device that estimates synchrophasor, frequency and rate of change of frequency the input voltage [1]. Synchronized measurement of phase angle, at different locations within the power systems, helps in real-time monitoring and analysis of power system dynamics.

This paper discusses the development and initial testing results of a PMU. The results obtained for the measurement of RMS voltage, frequency and phase of the input ac signal is presented here. Quadrature sampling technique is used to measure RMS and phase value and zero crossing detection is used for frequency measurement.

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II. RELATED WORK

Several approaches for measurement of frequency and phasor of input signal by the PMU are discussed in various literatures. ARM microcontroller based phasor measurement technique is explained in [2], in which sine wave signal is considered as input and sampled. Average of the sampled data gives the RMS value and total number of samples before the positive zero crossing corresponds to the phase of the signal. Discrete Fourier Transform (DFT) based magnitude and phase measurement and its simulation performed in LabVIEW is explained in [3]. MATLAB/Simulink model for PMU is explained in [4].

III. PROPOSED PMU DESIGN

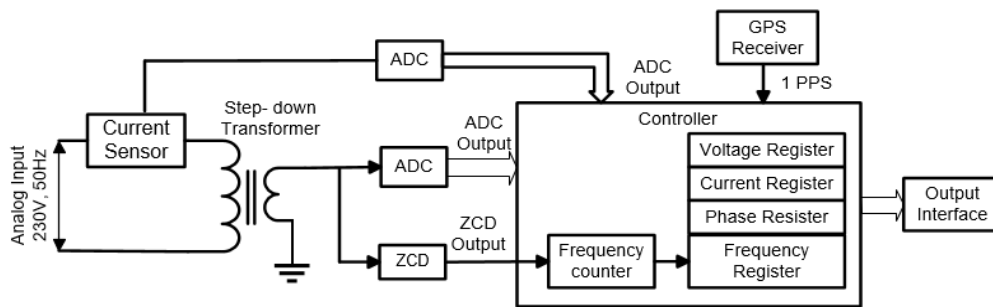


Figure 1: Block diagram of proposed PMU design

Block diagram of proposed design of PMU is shown in Figure 1. In the proposed design, Field Programmable Gate Array (FPGA) is used as a controller. Global Positioning System (GPS) receiver is used to detect 1 Pulse per Second (PPS) signal from the GPS source for synchronized measurement and also time and date information. Step-down transformer is used to reduce the input AC voltage to $3.3V_{pp}$. Hall based sensor is used to sense the input AC current. ADS7253 ADC is used to provide the digital equivalent of input signal. ADS7253 is a dual channel ADC supporting simultaneous sampling. Input signal through the step-down transformer is applied to one channel and Hall sensor output is applied to other channel of ADC. Then frequency RMS value and phase of the input signal is measured and displayed on output interface.

IV. METHODOLOGY

Frequency Measurement

Frequency of input signal is measured using zero crossing detection. Input signal is applied to a Zero Crossing Detector (ZCD) and converted to square wave [2]. ZCD output and its time delayed signal is logically XOR'ed to produce narrow square pulses (XOR'ed output) as shown in Figure 2. These narrow square pulses are then counted over period of half a second, which corresponds to frequency of input signal.

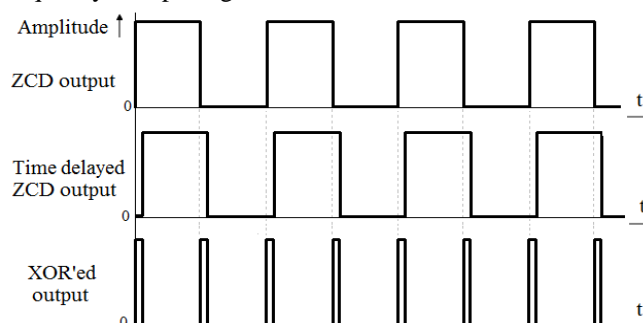


Figure 2: Frequency measurement using ZCD

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Figure 3 shows the flowchart for frequency measurement. If the control signal “Reset” is logically high, “Frequency” value is reset to zero. When “Reset” is at logic low level, “ZCD_output” signal is loaded to “Td_ZCD” signal to produce time delayed signal. “ZCD_output” and “Td_ZCD” is logically XOR’ed to generate “XOR’ed_output”. Logic high period of “XOR’ed_output” is counted over a period of half a second, which corresponds to the “Frequency” value.

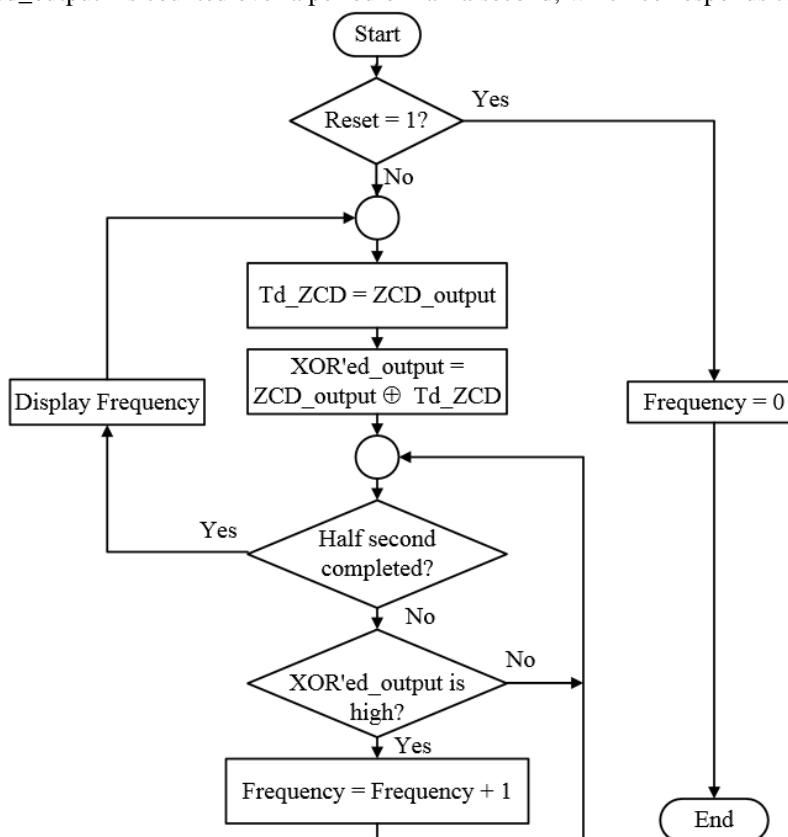


Figure 3: Flowchart for frequency measurement

Voltage and Phase Measurement

Voltage and phase of the input signal is measured using quadrature sampling technique. In this method, input signal is sampled four times per cycle with 90° phase difference between two consecutive samples. The DC offset is obtained by averaging the measurements which are 180° apart. To measure peak value, the offset nulled measurements which are in quadrature to each other (0° and 90° or 180° and 270°) referred as I and Q are considered and peak value, RMS value and phase are calculated as given in equations (4), (5) and (6) respectively [3].

$$\text{Peak value} = \sqrt{I^2 + Q^2} \quad (4)$$

$$\text{RMS value} = \frac{\text{Peak value}}{\sqrt{2}} \quad (5)$$

$$\text{Phase} = \tan^{-1} \frac{I}{Q} \quad (6)$$

Figure 4 shows the flowchart for Phasor measurement. Once the “Enable” signal is set, the conversion process is started and ADC output is stored in the memory register. Conversion process restarts at every 5ms (considering 50Hz input) and once four consecutive measurements are done, RMS and phase value of the input is calculated and displayed on Liquid Crystal Display (LCD).

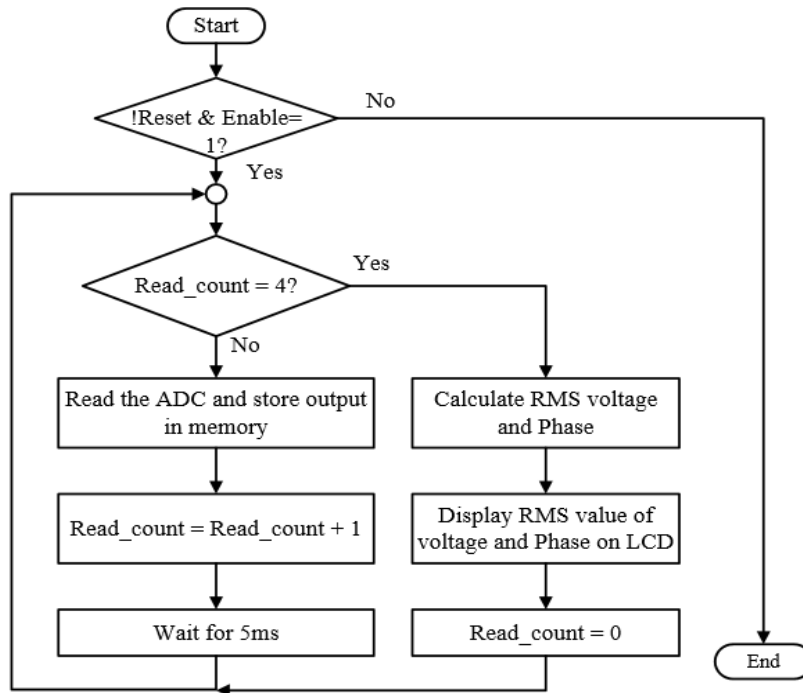


Figure 4: Flowchart for phasor measurement

V. SIMULATION AND RESULTS

Figure 5 shows the simulation result for frequency measurement. The simulation is carried out using Quartus design tool assuming that ZCD output of frequency 50Hz, “ZCD_output” is externally available and “Td_ZCD” is the time delayed signal of ZCD output. “Pulse_1s” is a signal of period one second. Logical XOR of “ZCD_output” and “Td_ZCD” generates a signal “XOR’ed_output”. During the logical low level of “Pulse_1s” signal, “Frequency_reg” value is incremented by one, when “XOR’ed_output” is high. During the rising edge of “Pulse_1s” signal, “Frequency_reg” value is stored in “Frequency” and “Frequency_reg” value is initialized to zero. Since “ZCD_output” is a signal of frequency 50Hz, “Frequency” value is set to 50 at the rising edge of “Pulse_1s” signal.

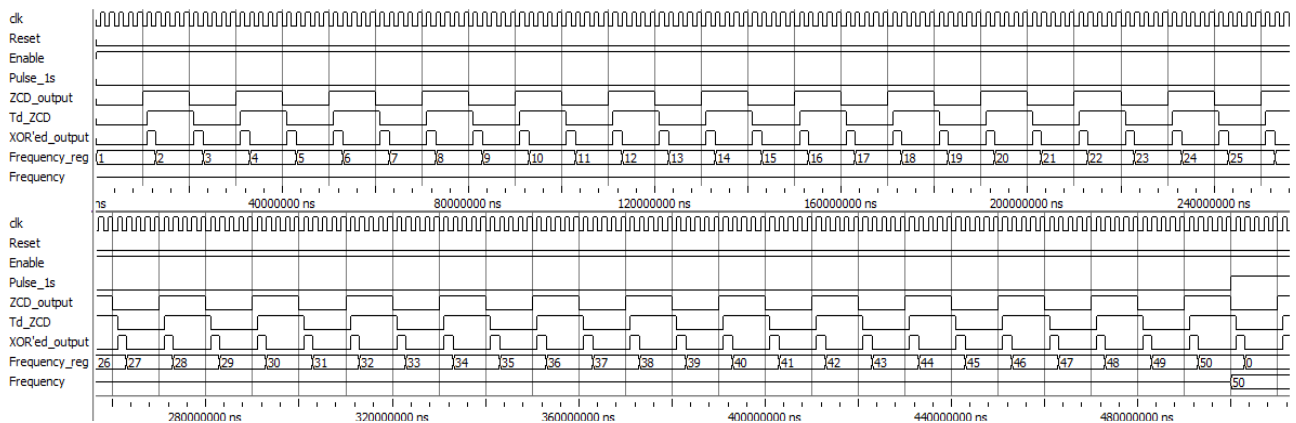


Figure 5: Simulation result for frequency measurement

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For hardware implementation of frequency and phasor measurement, Altera Cyclone-V FPGA is used as a controller. For the initial testing of designed module, input voltage signal of magnitude 3.2Vpp and frequency 50Hz is applied from the audio frequency oscillator considering that the input voltage is applied from step-down transformer. This input signal is applied to ZCD circuit to generate square wave for frequency measurement. Since the ADC supports unipolar input, clamper circuit is used to shift the input signal to the required level and applied to ADC. After performing the necessary operation, RMS value of 224.27V is obtained for this signal, which is approximately equal to the estimated value of 223.03V and measured frequency value is 50Hz. Figure 6 shows the displaying of RMS, frequency and phase of the input voltage signal on LCD.

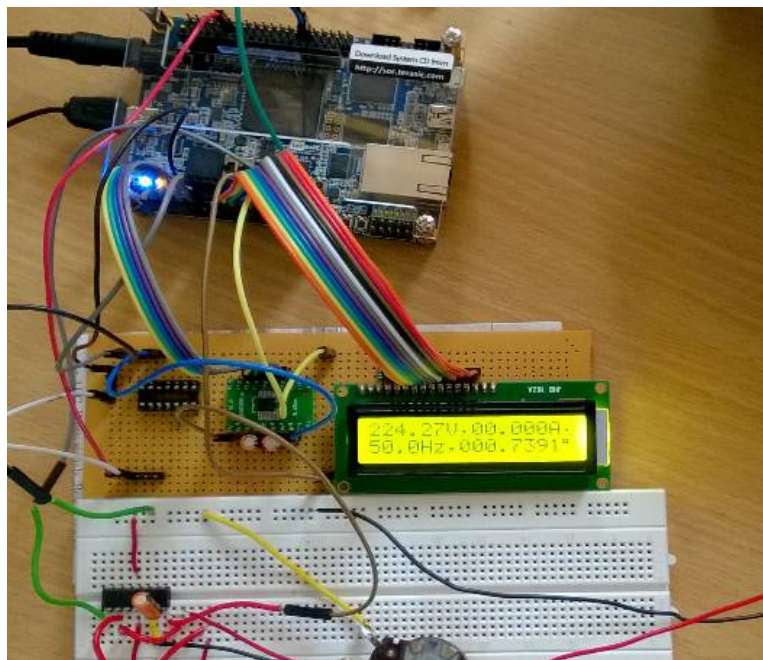


Figure 6: Displaying RMS, frequency and phase of input voltage on LCD

Table 1 shows the resource usage for the implemented design.

Table 1: Resource usage for the implemented design

| | |
|-------------------------|-------|
| Total registers | 9885 |
| Total input/output pins | 24 |
| Total block memory bits | 10386 |
| Total DSP blocks | 38 |
| Total PLLs | 1 |

VI. CONCLUSION

Modules to measure the RMS, frequency and phase of the input voltage signal is developed in Verilog HDL and implemented on FPGA. Functional testing for the measurement of peak, RMS value, frequency and phase of input signal is done. Interface for the measurement of current and GPS receiver are currently being done. Further testing is to be done to validate the measured values.

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