

# Application of Vedic Mathematics for Computation of Basic DSP Operations

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**ABSTRACT:** In most of the Digital Signal Processing (DSP), critical operations are multiplication and accumulation. Convolution plays a major role in various DSP applications. Multiplication is the essential component in designing DSP operations. In this regard, a study is carried out on the Urdhva-Tiryagbhyam sutra of Vedic mathematics and a multiplier is designed. DSP operations namely linear convolution, circular convolution and Multiply and Accumulate (MAC) are implemented using Vedic multiplier. The coding is developed in Verilog and it is synthesized and simulated using Xilinx ISE 13.2. The results are analysed with array multiplier in terms of computation time.

**KEYWORDS:** Urdhva-Tiryagbhyam, Vedic mathematics.

## I. INTRODUCTION

With the advancement of VLSI technology, digital signal processing plays a crucial role in many areas of electrical engineering. The accuracy of the mathematical calculations improves by analyzing outputs of DSP operations. To perform multiplication operation in the processor it requires time to compute and the system performance is determined by the performance of the multiplier with respect to computation time.

The execution time in most DSP algorithms mainly depends upon the time required for multiplication, so there is a need of multiplier which consumes less computation time. Vedic mathematics provides the unique solution for decreasing computation time. Vedic mathematics are reproduced from Vedas by Swami Bharathi Krishna Thirtha after his eight years of research [2]. Many application areas in engineering use Vedic mathematics especially in signal processing. Vedic mathematics is primarily based on sixteen sutras. Urdhva-Tiryagbhyam sutra is one of the sixteen sutras which is used to design Vedic multiplier. The DSP operations are implemented using Vedic multiplier.

## II. RELATED WORKS

Most of the multiplication algorithms for high speed implementation are based on conventional multiplier and its modifications. The main disadvantage of the add and shift multiplication method is that it consumes more time to compute. The Vedic mathematics approach for multiplication is useful for fast computation when compared to array multiplier [1].

A method for calculating convolution sum of finite length sequences is explained in [3]. The linear convolution is implemented using Vedic multiplication based on Paravartya Yojayet (Transpose & Adjust) sutra [4].

## III. VEDIC MULTIPLIER

Vedic multiplier is designed based on Urdhva-Tiryagbhyam sutra. This sutra has been used for the multiplication of two decimal numbers. The similar technique is applicable to binary number system to build the proposed algorithm suitable with digital domain. Urdhva-Tiryagbhyam means "vertical and crosswise". It is based on concept through which partial products and additions are done concurrently leading to short computation time.

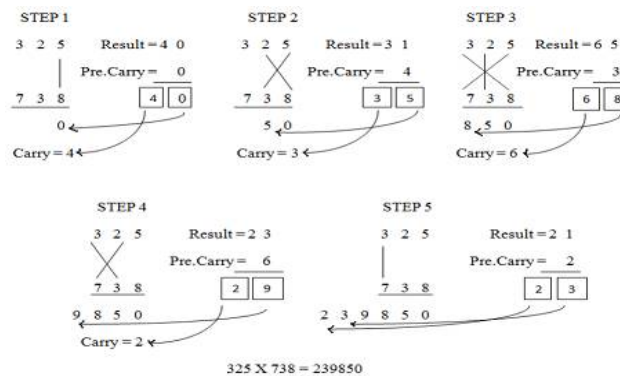
Figure 1 shows the illustration of multiplication of two decimal numbers by Urdhva-Tiryagbhyam method. The multiplication is done by multiplying least significant digits on both sides of line and it is added with previous carry.

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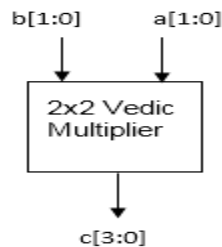
The result is one bit and carry is generated. The carry generated is added in next step. All results of previous carry are added, if there are more than one line present in one step. Least significant bit act as result bit in each step and rest of the bits act as carry in previous step. At the initial step carry is zero.



**Figure 1: Multiplication of Two Decimal Numbers**

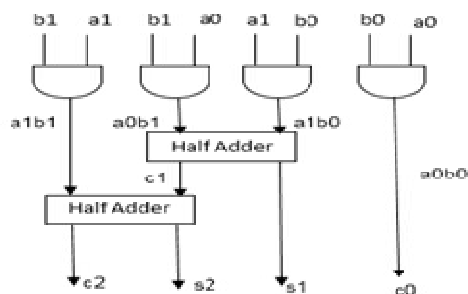
### A. 2x2 Vedic Multiplier

Figure 2 shows the block diagram of 2x2 Vedic multiplier module.



**Figure 2: Block Diagram of 2x2 Vedic Multiplier Module**

Figure 3 shows the structure of 2x2 Vedic multiplier designed using four AND gates and two half-adders. The total delay is two half-adder delays, once the product bits are generated.



**Figure 3: Structure of 2x2 Vedic Multiplier**

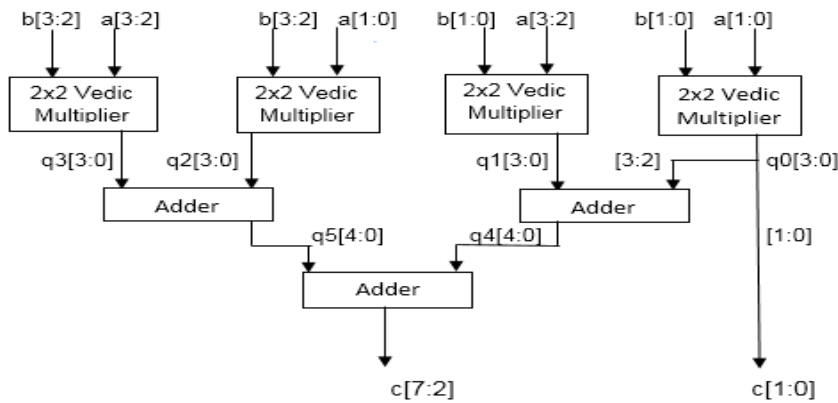
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### B. 4x4 Vedic Multiplier

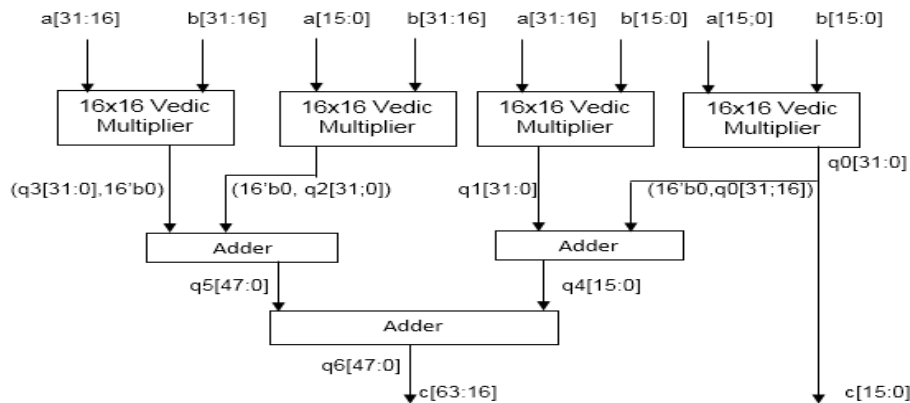
Figure 4 shows the structure of 4x4 Vedic multiplier using 2x2 Vedic multiplier as building block. Adders are used to add partial products [3].



**Figure 4: Structure of 4x4 Vedic Multiplier**

### C. 32x32 Vedic Multiplier

8x8 Vedic multiplier have been designed using 4x4 Vedic multiplier as building block. 16x16 Vedic multiplier have been designed using 8x8 Vedic multiplier as building block. Following the same method, 32x32 Vedic multiplier is designed using the 16x16 Vedic multiplier as building block. Figure 5 shows the structure of 32x32 Vedic multiplier.



**Figure 5: Structure of 32x32 Vedic Multiplier**

## IV. DSP OPERATIONS

### A. Linear Convolution

Convolution is one of the DSP operations which is the mathematical way of combining two signals  $x$  and  $h$ , to obtain a third signal  $y$  [4]. Linear Convolution of two discrete sequences is given by the equation (1).

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$$y(n) = \sum_{k=-\infty}^{k=\infty} x(k)h(n-k) \quad (1)$$

Linear convolution is implemented using 4x4 bit Vedic multiplier which improves its efficiency in terms of speed.

### B. Circular Convolution

Circular convolution of two equal length sequences  $x(n)$  and  $h(n)$  is given by the equation (2). Circular convolution is computed using linear convolution technique.

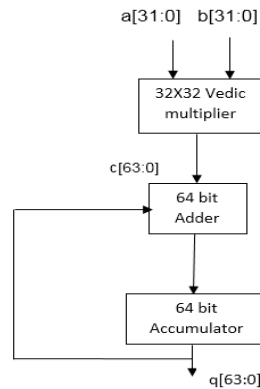
$$y(n) = \sum_{k=0}^{k=N-1} [x(k)h(n-k)] \bmod N \quad (2)$$

Circular convolution is implemented using 4 bit linear convolution based on Vedic multiplier.

### C. Multiply and Accumulate(MAC)

Multiply and Accumulate is one of the normally used operation in various DSP applications. Speed of multiplier determines the speed of MAC. The performance of MAC can be increased by using efficient multiplier in terms of speed. Thus MAC is designed using Vedic multiplier.

Figure 6 shows the architecture of 32 bit MAC. The MAC unit comprises of a multiplier followed by an adder and an accumulator register which stores the result. The two 32 bit operand  $a[31:0]$  and  $b[31:0]$  are inputs to the MAC unit. The output from 32 bit MAC is  $q[63:0]$ . 32x32 bit Vedic multiplier is used to design 32 bit MAC.



**Figure 6: Architecture of 32 bit MAC**

## V. RESULTS

Verilog code is developed for 4x4 bit and 32x32 bit Vedic multiplier and synthesized using Xilinx ISE 13.2. Synthesis is done for FPGA (Field Programmable Gate Array) Spartan3 XC3S400-TQ144. Test waveforms are generated using Xilinx software. Using Vedic multiplier, Verilog code is developed for linear convolution, circular convolution and MAC unit. Synthesis and simulation is done for the same.

Figure 7 shows the simulation result of 32x32 bit Vedic multiplier. From Figure 7, for multiplication of inputs  $a = \text{FFFFFFFF(H)}$ ,  $b = \text{FFFFFFFF(H)}$ , product  $c = \text{FFFFFFFFE00000001(H)}$ .



**Figure 7: Simulation Result of 32x32 bit Vedic Multiplier**

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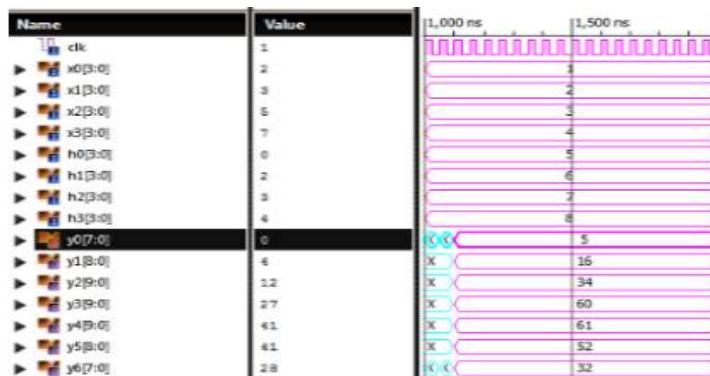
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Table 1 shows the timing summary of Vedic multiplier and array multiplier. It is found that time delay for Vedic multiplier is relatively shorter than array multiplier.

**Table 1: Timing Summary of Multiplier**

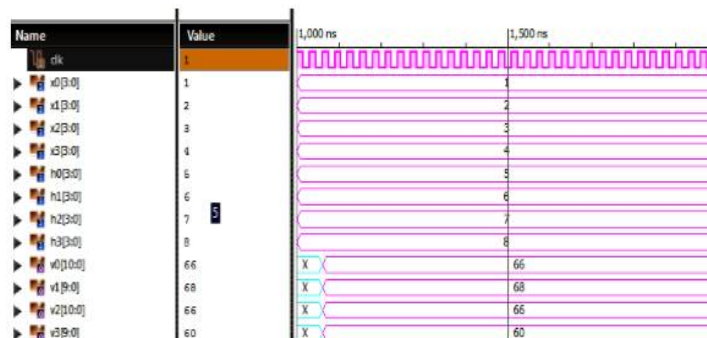
Multiplier	Time delay in nanoseconds(ns)	
	Array multiplier	Vedic multiplier
4x4 bit	17.59	14.18
32x32 bit	41.91	39.53

Figure 8 shows the simulation result of linear convolution using Vedic multiplier. From Figure 8,  $x(n) = (x_0, x_1, x_2, x_3) [1\ 2\ 3\ 4]$ ,  $h(n) = (h_0, h_1, h_2, h_3) = [5\ 6\ 7\ 8]$ ; Output  $y(n) = (y_0, y_1, y_2, y_3, y_4, y_5, y_6) = [5\ 16\ 34\ 60\ 61\ 52\ 32]$ .



**Figure 8: Simulation Result of Linear Convolution**

Figure 9 shows the simulation result of circular convolution using Vedic multiplier. From Figure 9,  $x(n)=(x_0,x_1,x_2,x_3) [1\ 2\ 3\ 4], h(n)=(h_0,h_1,h_2,h_3)=[5\ 6\ 7\ 8]$ ; Circular convolution Output  $v(n)=(v_0,v_1,v_2,v_3)=[66\ 68\ 66\ 60]$ .



**Figure 9: Simulation Result of Circular Convolution**

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Figure 10 shows the simulation result of 32 bit MAC.

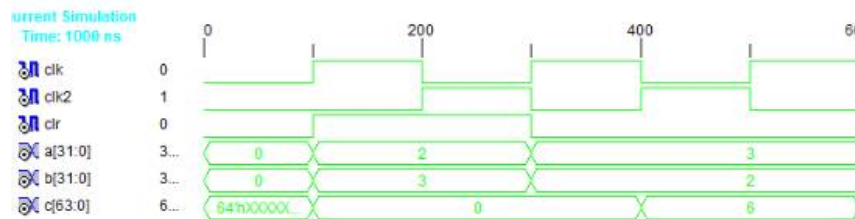


Figure 10: Simulation Result of 32 bit MAC

Table 2 shows timing summary of DSP operations using different multiplier techniques. With reference to Table 2, it is found that DSP operations using Vedic multiplier leads to short computation time.

Table 2: Timing Summary of DSP Operations

DSP Operations	Time delay in nanoseconds(ns)	
	Array Multiplier	Vedic Multiplier
32 bit MAC	35.91	32.63
Linear Convolution	23.75	21.27
Circular Convolution	23.71	21.04

## VI. CONCLUSION

Multiplier is one of the vital functions in digital signal processing. It is desired to have area efficient, high speed, power efficient multiplier. In this regard, Vedic multiplication based on Urdhva-Tiryagbyham is studied and simulated. The simulations are carried out for 4x4 bit to 32x32 bit Vedic multiplier. In this technique, partial products and additions are done concurrently leading to short computation time.

DSP operations namely linear convolution and circular convolution are implemented using Vedic multiplier and simulated. 32 bit MAC unit is designed using 32x32 bit Vedic multiplier and simulated. The results are compared with array multiplier. It is found that Vedic multiplier is efficient than array multiplier with respect to computation time.

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