

# Design of Low Power Energy Efficient CMOS Circuits with Adiabatic Logic

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**ABSTRACT:** The increase in demand for low power devices led to research of solutions for the reduction of energy and power consumption. The switching events during charging-discharging of load capacitor cause increase in power consumption/dissipation. Adiabatic logic is an alternative approach for reducing the power consumption/dissipation. It offers a way to utilise the stored energy from the load capacitor by recycling to the power supply. In spite of the complexity of circuits, the logic provides good power saving. The simulation results of adiabatic logic circuits are compared to logic of CMOS circuits indicating the former is more advantageous.

**KEYWORDS:** switching events, power consumption/dissipation, adiabatic logic, recycling

## I. INTRODUCTION

The performance in computer systems is enhanced in several magnitudes due to increase in rapid switching and increase in the integrated transistors on a chip. These improvements are accompanied by greater energy and power consumption/dissipation. Hence it requires cooling packages increasing the cost and reducing the dependability on the system. The battery life is affected due to the application of low power. To overcome this VLSI designing helps to make compatible circuits for low power. Charging-discharging cycle leads to power dissipation. In order to reduce this, an alternative approach adiabatic logic is obtained. Yong Bin Kim et al. [1], discussed the results obtained by investigating the adiabatic logic on the basic gates such as NAND, NOR and XNOR, and more complicated circuits like a 4 and 8 bit adder. Maurya et al. [6], implemented NAND and NOR gates in Positive Feedback Adiabatic Logic (PFAL), that is methods of quasi adiabatic logic in spice tools using 180 nm technology to show the significant power saving compared to the conventional method. Dhaka et al. [7], proposed NOR logic gate using 2 Phase Adiabatic Static Clocked Logic (2PASCL) and Pass transistor Adiabatic Logic (PAL) which is simulated on 180 nm and 90 nm technology to obtain the comparison of significant power saving. Bharathi et al. [8], investigates the less power dissipation of the adiabatic techniques like Energy efficient Charge Recovery Logic (ECRL), PFAL, 2PASCL and PAL. It shows the working principle of energy efficient techniques. The performance shows that it is energy efficient compared to conventional CMOS design.

In adiabatic circuits, the dissipated energy is equal to the injected energy. Adiabatic technique is used to increase energy efficiency of logic circuit. For energy recovery, a capacitance  $C_L$  is charged or discharged through a circuit of resistance  $R$ , when the switching time  $T$  is increased, the power dissipation reduces. So during the simulation, by integrating the product of current and voltage and dividing it by the period  $T$ , then the power consumption can be given as follows:

$$P = \frac{1}{T} \int_0^T (\sum_{i=1}^n (VI)) dt \quad (1)$$

where,  $V$  and  $I$  are power supply voltage and current respectively and number of power supplies is given by  $n$ . The implementation and simulation of the circuits are designed in Cadence Virtuoso Spectre using a 45 nm CMOS technology with appropriate power supplies. Comparative analysis between the conventional CMOS, 2PASCL, ECRL, 2n-2n2p, PAL and PAL-2n is done based on the power dissipation/consumption.

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## II. CONVENTIONAL SWITCHING

CMOS is a combination of nMOS and pMOS in pull down and pull up section respectively. The source of pull up network is connected to power supply and source of pull down network is connected to ground. The switching due to charging-discharging of the load capacitors causes more power consumption. The Figure 1 shows the switching in conventional CMOS logic. The rise in the logic level causes the charging during the positive rail, which is given by,

$$Q = C_L V_{dd} \tag{2}$$

$C_L$  is the load capacitance. Hence, the power supply energy is given by,

$$QV_{dd} = C_L V_{dd}^2 \tag{3}$$

The energy withdrawn from the voltage supply is equal to the energy consumed in the circuit. Hence half of the energy stored during the charge cycle is

$$E_{\text{charge}} = \frac{1}{2} C_L V_{dd}^2 \tag{4}$$

The other half energy is dissipated as heat.

$$E_{\text{charge}} + E_{\text{discharge}} = C_L V_{dd}^2 \tag{5}$$

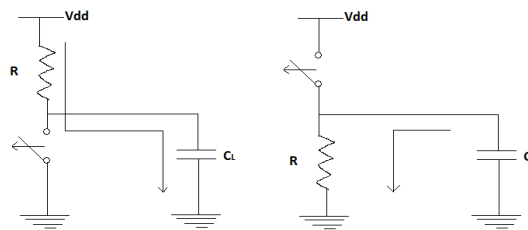


Figure 1: Conventional switching

## CONVENTIONAL CMOS CIRCUIT DESIGN

CMOS is the basic unit of the digital circuits. Within the drain of nMOS and pMOS in pull down and pull up section networks is the output of the circuit obtained. The switching activity in CMOS, charging-discharging of the load capacitance and frequency causes increase in power consumption. The Figure 2 shows the CMOS inverter circuit and the output of the CMOS inverter.

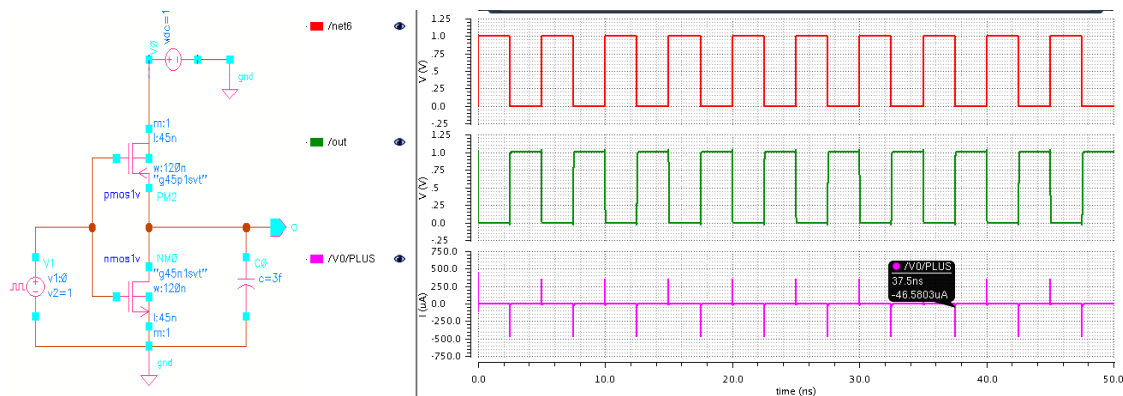


Figure 2: CMOS inverter circuit and the output of the CMOS inverter

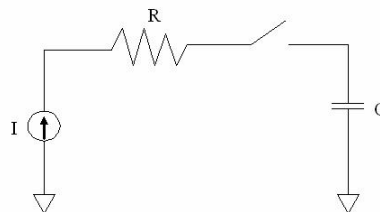
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## III. ADIABATIC SWITCHING

"Adiabatic" is taken from a Greek word and it describes thermodynamic process that shows no energy exchange with the surroundings. In real-time systems such perfect processes cannot be obtained due to some factors which causes dissipation. But dissipation can be decreased by reducing the operational speed and conditional transistor switching. It is also called as "Energy recovery CMOS", since it reuses the stored energies in the load capacitors. The ideal condition of the adiabatic process is achieved when the switching process is retarded. Practically energy dissipation cannot be reduced to be zero because the charge cycle is always associated with an adiabatic and a non-adiabatic component. The conservation of energy is achieved in the circuit rather than dissipation.



**Figure 3: Circuit explaining Adiabatic Switching**

The circuit consists of a constant current source (an AC power supply, a trapezoidal power supply or a linear voltage ramp). The circuit consisting of the Adiabatic Switching is shown in Figure 3. Consider the circuit where R is the resistance of the pMOS section. The capacitor voltage  $V_C$  is considered to be zero initially.

The voltage in the circuit is given by

$$V=IR \tag{6}$$

Then the power is given by

$$P= VI =I^2R \tag{7}$$

The amount of energy during charging,

$$E = R \int_0^T I^2 dt = RI^2T \tag{8}$$

Also

$$I = \frac{CV}{T} \tag{9}$$

Hence

$$E = E_{diss} = \frac{2RC}{T} \frac{CV^2}{2} \tag{10}$$

where, the respective terms are given as:

- E — energy dissipated during charging,
- C — load capacitance,
- R — ON resistance of the MOS switch,
- V — supply voltage,
- T — time period

### ECRL CIRCUIT DESIGN

ECRL consists of two cross-coupled transistors and n functional blocks in the nMOS transistors. Both positive and negative outputs are generated. The circuits suffer loss in the precharge and recover phases. Due to the cross coupling the outputs interfere each other. The propagation from one stage to next stage takes place in only one phase but the values are stored in four phases. Figure 4 shows the circuit and the output of the ECRL inverter.

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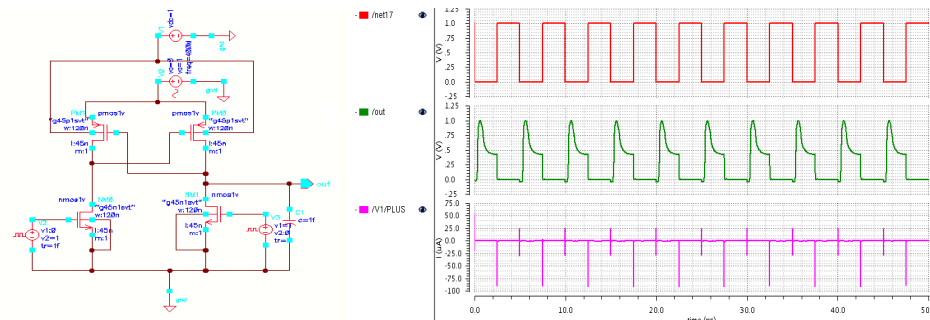


Figure 4: Circuit of ECRL inverter and the output of the ECRL inverter

## 2PASCL CIRCUIT DESIGN

The 2PASCL uses two phase sinusoidal power supply. One clock is in symmetry and other is unsymmetrical. The circuit has two transistors. One transistor is placed between the output and power clock and another placed between one of the terminals of nMOS and power source. Figure 5 shows the circuit and the output of the 2PASCL inverter.

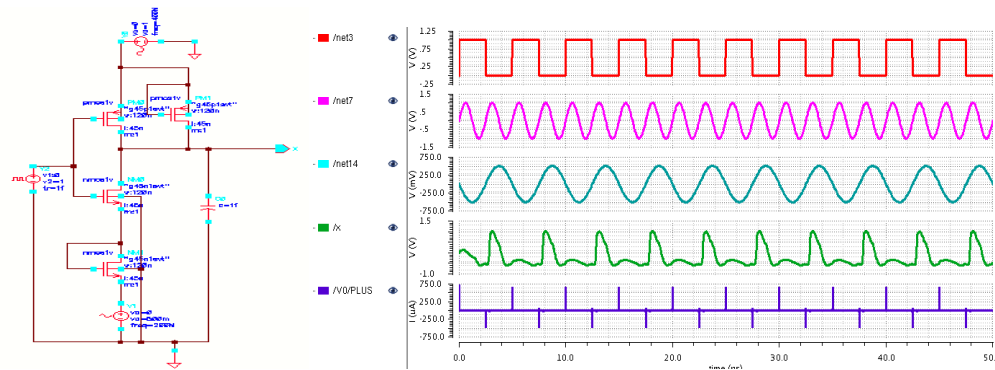


Figure 5: Circuit of 2PASCL inverter and the output of the 2PASCL inverter

## 2n-2n2p CIRCUIT DESIGN

2n-2n2p was introduced in order to overcome the coupling effects as in ECRL. The core of this logic consists of a latch of pMOS and nMOS transistors. The n-functional block is in parallel with nMOS. The cross-coupled nMOS transistors switches larger part results in the non-floating outputs. The cross coupled pMOS are used during precharge phases. Figure 6 shows the circuit and the output of the 2n-2n2p inverter.

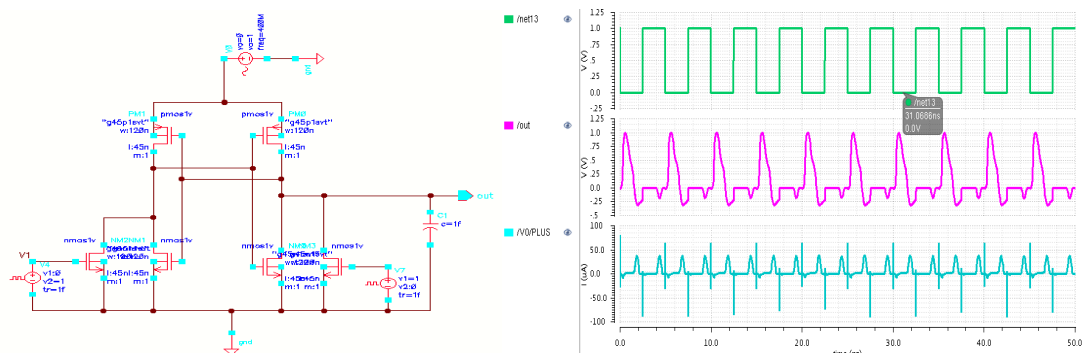


Figure 6: Circuit of 2n-2n2p inverter and the output of the 2n-2n2p inverter

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## PAL CIRCUIT DESIGN

PAL is a dual rail adiabatic logic. The gate complexity is less. It uses two phase clock rising. In the evaluate phase the clock rises from 0 to  $V_{dd}$  and supplies energy to the circuit, then the clock returns to 0 in the recovery phase and the energy is recycled to power clock generator. The two n-trees realize the logic functions. Figure 7 shows the circuit and the output of the PAL inverter.

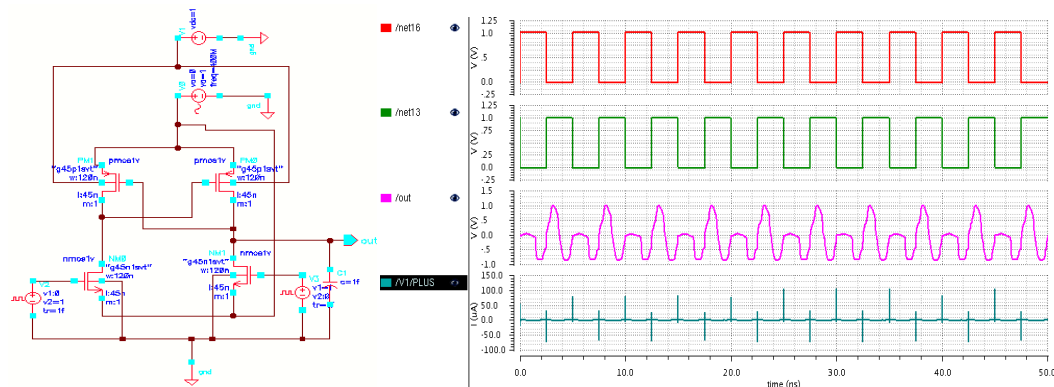


Figure 7: Circuit of PAL inverter and the output of the PAL inverter

## PAL-2n CIRCUIT DESIGN

PAL-2n with nMOS pull-down configuration is a dual-rail circuit. It is a quasi adiabatic logic circuit. The core is a latch made by pMOS and nMOS also called as 'Adiabatic Amplifier'. The pMOS transistor of the latch has parallel n-functional blocks and form a transmission gate. It avoids logic level erosion on the output nodes, but complete recovery of clock signals is not possible. PAL-2n uses a four phase clock rising from 0 to  $V_{dd}$  in the evaluate phase and supplies energy to the circuit, then the clock returns to 0 in the recovery phase. Figure 8 shows the circuit and the output of the PAL-2n inverter.

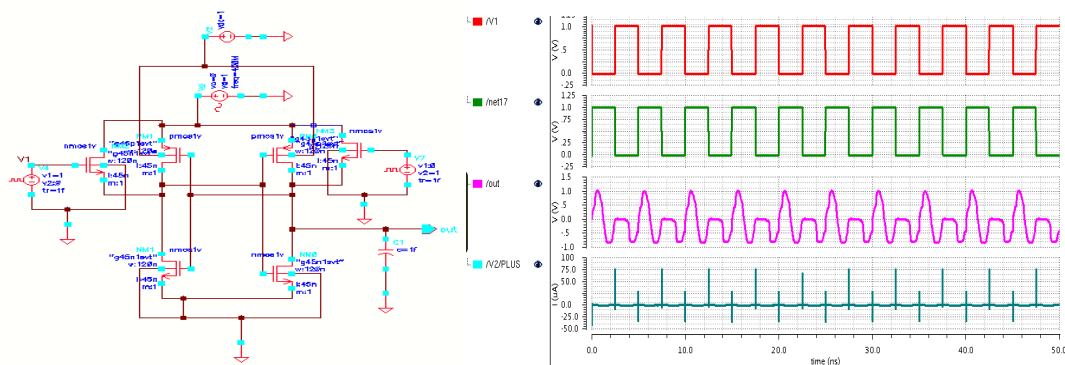


Figure 8: Circuit of PAL-2n inverter and the output of the PAL-2n inverter

## IV. RESULTS AND DISCUSSION

The Table 1 shows the average power consumption of all the logic styles. The comparisons of all logics show that adiabatic logic has less power consumption than conventional CMOS. The implementation of inverter and other basic gates AND, OR and 2:1 multiplexer is simulated and the average power consumption is calculated.

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**Table 1: Average power consumption of logic circuits**

Logic	Average power consumption (watts)			
	Inverter	AND	OR	2:1 multiplexer
CMOS	244 n	25.98 n	34.63 n	142.07 n
2PASCL	7.085 n	17.58 n	17.58 n	63.68 n
ECRL	0.392 n	0.392 n	0.288 n	0.27 n
2n-2n2p	5.38 u	5.38 u	615.4 n	3.651 u
PAL	0.406 n	0.406 n	0.434 n	0.738 n
PAL-2n	0.488 n	0.488 n	1.04 n	1.03 n

## V. CONCLUSION

The simulation of basic gates is analyzed at 45 nm technology at 1 V with clock frequencies of 400 MHz and 200 MHz with a load capacitance of 0.01 pF for conventional CMOS, 2PASCL, ECRL, 2n-2n2p, PAL and PAL-2n. From the comparison of the results obtained, the average power consumption of the circuit calculated is considerably low in adiabatic logic that uses power clock supply.

## REFERENCES

- [1] Yong Bin Kim and Shivakumar Sompur, "An investigation into adiabatic circuits", IEEE Transactions on Circuits and Systems, vol. 1, ISBN :07803-7150-X, pp. 294-297, 2001.
- [2] Kaushik Roy Pandit, Saibal Mukhopadhyay and Hamid Mahmoodi Meimand, "Leakage Current Mechanisms and Leakage Reduction Techniques in Deep Sub-micrometer CMOS Circuits", Proceedings of the IEEE, ISSN: 0018-9219, INPEC Accession Number: 7552870, vol. 91, no. 2, pp. 305-327, 2003.
- [3] Cihun Siyong, Muh Tian Shiue, Ci Tong Hong and Kai Wen Yao, "Analysis and Design of an Efficient Irreversible Energy Recovery Logic in 180nm CMOS", IEEE Transactions on Circuits and Systems, vol. 55, no. 9, pp. 2595-2607, 2008.
- [4] Nazrul Anuar, Yasuhiro Takahashi and Toshikazu Sekine, "Two Phase Clocked Adiabatic Static CMOS Logic", IEEE ICECS, pp. 503-506, 2009.
- [5] Nazrul Anuar, Yasuhiro Takahashi and Toshikazu Sekine, "XOR evaluation of 4X4 BIT array Two Phase Clocked Adiabatic Static CMOS Logic", IEEE MWSCAS, 2010.
- [6] Atul Maurya and Gaganes Kumar, "Adiabatic Logic: Energy Efficient Technique for VLSI Applications", International Conference on Computer & Communication Technology, IEEE, pp. 234-238, 2011.
- [7] Gayatri, Mahendra Singh Dhaka and Pramendra Singh Dhaka, "Adiabatic Logic Gate for Low Power Application", International Journal of Engineering Research and Applications (IJERA), vol. 2, Issue-3, pp. 2474-2478, 2012.
- [8] M. Bharathi, B. Dilli Kumar, "Design of Energy Efficient Arithmetic Circuits Using Charge Recovery Adiabatic Logic", International Journal of Engineering Trends and Technology, vol. 4, Issue-1, pp. 32-40, 2013.
- [9] Arjun Mishra and Neha Singh, "Low Power Circuit Design Using Positive Feedback Adiabatic Logic (PAL-2n)", International Journal of Science and Research, vol. 3, Issue-6, ISSN: 2319-7064, pp. 43-45, 2014.
- [10] Santpal Singh, Gagandeep Singh and Jaspreet Singh, "An Adiabatic Approach to Design Low Power Energy Efficient CMOS Circuits", International Journal of Emerging Research in Management & Technology, ISSN: 2278-9359, vol. 4, Issue-4, pp. 11-14, 2015.
- [11] Kshitij Shinghal, Deepti Shinghal and Amit Saxena, "Design and Implementation of Adiabatic based Low Power Logic Circuits", International Research Journal of Engineering and Technology, vol. 2, Issue-2, ISSN: 2395-0072, pp. 498-504, 2015.