

Design of Two-Stage CMOS Operational Amplifier suitable for Signal Conditioning

Divyashree N V¹, Usha Desai², Asha Kiran³

M.Tech Student, Dept of E&C, NMAMIT, Nitte, Udupi, Karnataka, India¹

Associate Professor, Dept of E&C, NMAMIT, Nitte, Udupi, Karnataka, India²

Deputy Manager, IC Design Centre, BEL, Bengaluru, Karnataka, India³

ABSTRACT: We know that PMOS and NMOS technology have many drawbacks. They have very low speed, circuit complexity is also more, power dissipation is high and noise margin is low. CMOS is a combination of PMOS and NMOS and are fabricated on same chip. So power dissipation is reduced and speed is increased. Designing of high gain CMOS OPAMP is a challenging task for a designer. The bias current decides the input to CMOS two-stage OPAMP. Here the two-stage OPAMP is designed by making use of Miller compensation technique. The designed OPAMP displays frequency of around 5.8MHz, with gain of 74.64dB and 81.25 degree phase margin and load capacitance of 5pF. The slew rate is obtained at 14.54 μ V/Sec, CMRR of 73.66dB and PSRR of 80.49dB.

All the work has been carried out using Cadence 0.6 μ m technology. In the first section we have Introduction, second section includes Related work, third section includes Specification of proposed circuit, fourth section includes Simulations, fifth section presents Conclusion and last section has References.

KEYWORDS: CMOS, gain, phase margin, CMRR, PSRR, and compensation.

I. INTRODUCTION

The electronics industry has exploded in last few years. In analog signal processing systems, OPAMPs form an integral part. In CMOS technology the design of analog circuits like OPAMPs becomes very critical and challenging. OPAMP is a linear device which can be used for many applications like signal conditioning, filtering, and many mathematical operations are carried out like addition, subtraction, differentiation, integration etc. Advantages of OPAMP include they are small size, cost is reduced, reliability is high, less power consumption when compared to discrete circuits.

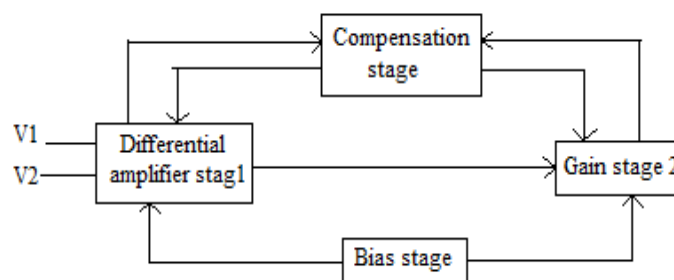


Figure 1: Block diagram of dual-stage CMOS OPAMP

The Block diagram shown above consists of differential input stage which is followed by a Common Source(CS) 2nd stage. The CS stage rises the DC gain and in-turn increases the OPAMP output swing for given voltage supply. Bias

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circuit creates the operative point to each transistor to work in quiescent phase. Miller compensation is provided for getting closed loop performance.

II. RELATED WORK

Anchal Verma [2] presents a design of two-stage CMOS OPAMP, to operate using umc 2µm CMOS technology at ±2.5V power supply. The designed OPAMP is CMOS two-stage OPAMP. The OPAMP designed exhibits a unity gain frequency of around 4.416MHz with a gain of 96dB and 700 phase margin. Design and Simulation have been carried out using LT Spice tools.

Yadav [3] proposed a precise method to design two-stage OPAMP. The OPAMP which is designed is two-stage CMOS OPAMP which is followed by the output buffer and exhibits UGB of around 14 MHz with gain of 77.25 dB with phase margin of about 85.85°.

Palmisano and Palumbo [5] determined design equations for improved compensation approach having current buffer. It allows a high gain-bandwidth product to be achieved in the design. It also avoids the drawbacks that arise with the voltage buffer and nulling resistor methodologies. Due to the RC compensation network with the second gain stage the commonly used two-stage CMOS OPAMP suffers from two elementary performance limitations. First, it offers the stable operation for only restricted range of capacitive loads, secondly, above the open-loop pole frequency, power supply rejection shows severe degradation.

Gray and Meyer [10] presented a summary of current design methods for the OPAMP implemented in CMOS and NMOS knowledge at the tutorial level. Factors affecting the performance of OPAMP like voltage gain and input noise, offsets and common mode and power supply rejection, transient response and power dissipations are considered.

III. SPECIFICATIONS OF PROPOSED CIRCUIT

The OPAMP circuit is designed to meet the following specifications as shown in Table 1. Theoretical values are validated and two-stage OPAMP is implemented using the specifications mentioned below.

Table 1: Specifications of the OPAMP

Process Specifications	Theoretical values	Practical values
Supply Voltage	±5 V	±5 V
Bias Current	30 µA	26 µA
Gain	80dB	72.06 dB
Gain Bandwidth	10 MHz	7.457 MHz
Phase Margin	91.22°	81.39°
K_n	126.65 µA/V ²	126.65 µA/V ²
K_p	76.9 µA/V ²	76.9 µA/V ²
Slew rate	20 µV/sec	19.94 µV/sec

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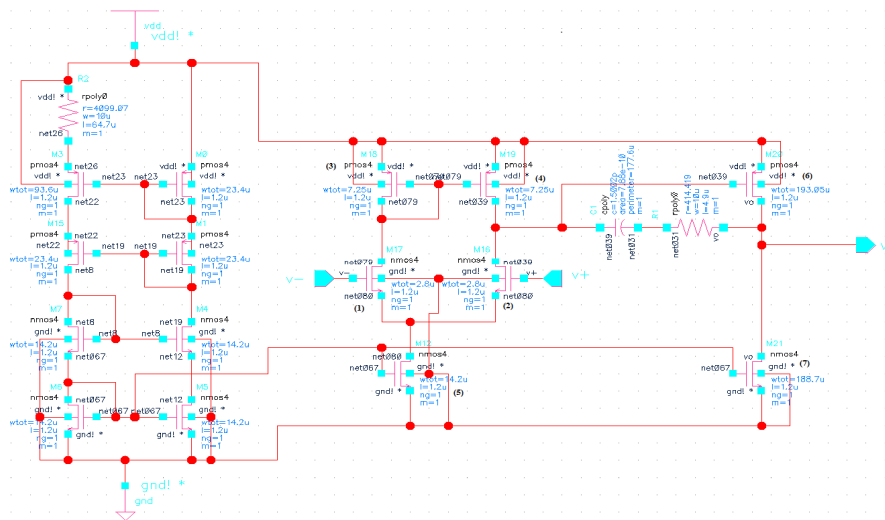


Figure 2: Schematic of two-stage CMOS OPAMP

The schematic (Figure 2) consists of three sub parts: differential amplifier stage, second gain stage and biasing circuit stage. Bias stage consists of 8 transistors, differential stage consists of 5 transistors and second gain stage has 2 transistors. To provide high gain and high output swing two-stage OPAMP is chosen. To minimise the temperature and open loop variations OPAMPs are biased and compensated. The aspect ratios of all the transistors used in the schematic are presented in Table 2.

Table 2: MOSFET sizing specifications

MOSFET	W/L RATIO
M1	2.3374
M2	2.3374
M3	6.056
M4	6.056
M5	11.84
M6	160.865
M7	157.27

IV. SIMULATIONS

All the simulations are done on cadence virtuoso with 0.6 μ m technology with V_{DD} of 5V. The load capacitance is 5pF for all simulations. By doing AC analysis we decide gain, phase margin and unity gain bandwidth of OPAMP. The gain is obtained to be 72.06 dB with a phase margin of 81.39 $^\circ$ and unity gain bandwidth of around 7.457 MHz.

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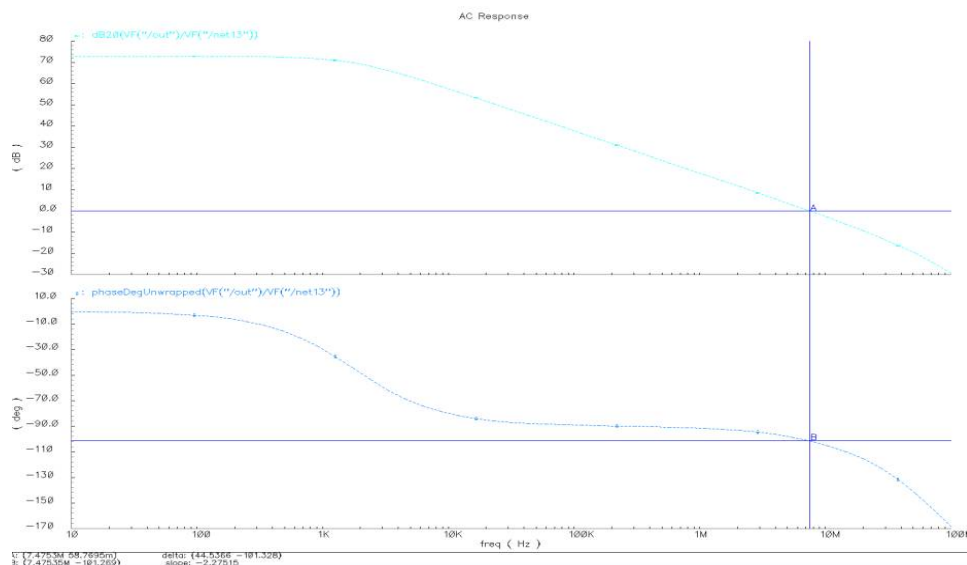


Figure 3: Gain and Phase response curves

V. CONCLUSION

The objective of the presented work was to implement a full custom design of two-stage CMOS OPAMP plus analyse its behaviour. The miller compensation technique is active in the design. The designed OPAMP is very much suitable for signal conditioning and ADC applications. The basic two-stage OPAMP is designed using CMOS 0.6 μ m technology. XFAB foundry is used for the whole process. The outcomes indicate the designed amplifier has efficiently fulfilled wholly the design specifications.

REFERENCES

- [1] Hamed Aminzadeh and Reza Lotfi, "Design guidelines for high-speed two stage CMOS Operational Amplifiers", The Arabian Journal for Science and Engineering, Vol.32, pp.75-87, 2007.
- [2] Anchal Verma, Deepak Sharma, Rajesh Kumar Singh, Mukul Kumar Yadav, "Design of Two-Stage CMOS Operational Amplifier", International Journal of Emerging Technology and Advanced Engineering, Vol. 3, Issue 12, pp.102-106, 2013.
- [3] Amana Yadav, "Design of Two-Stage CMOS Op-Amp and Analyze the Effect of Scaling", International Journal of Engineering Research and Applications, Vol. 2, Issue 5, pp.647-654, 2012.
- [4] Priyanka Kakoty, "Design of a high frequency low voltage CMOS Operational amplifier", International Journal of VLSI design & communication System, Vol.2, pp. 73-85, 2011.
- [5] G. Palmisano and G. Palumbo, "A Compensation Strategy for Two Stage CMOS OPAMPs Based on Current Buffer", IEEE Transaction Circuits and System-I: Fund Theory and Applications, Vol. 44, pp. 879-440, 1997.
- [6] Savn Bandyopadhyay, Deep Mukherjee, Rajdeep Chatterjee, "Design Of Two Stage CMOS Operational Amplifier in 180nm Technology With Low Power and High CMRR", International Journal Of Recent Trends in Engineering & Technology, Vol. 11, pp.239-247, 2014.
- [7] Amana Yadav, "A Review Paper on Design and Synthesis of two stage CMOS op-amp" International Journal of Advances in Engineering & Technology, Vol.2, Issue 1, pp.677-688, 2012.
- [8] B. Razavi, "Design of Analog CMOS Integrated Circuits", New York: Mc-Graw Hill, 2001.
- [9] P. Allen and D. Holmberg "CMOS Analog Circuit Design", 2nd Edition. Saunders college publishing/HRW, Philadelphia, PA, 1998.
- [10] P. R. Gray, P.J. Hurst, S.H. Lewis and R.G. Meyer, "Analysis and Design of Analog Integrated circuits", Forth Edition. John Wiley & Sons, Inc., 2001.