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Design of Controller Board and DC-DC Interface for Remote Sensing Satellites

Basavaraj¹, SK Najeer ahemmad², Dr. Veena Devi Shasthrimath³

M.Tech Student, Dept. of Electronics and Communication, NMAM Institute of Technology, Nitte, Udupi District,
Karnataka, India¹

Sci/Eng, 'SE', DHSG ISAC, ISRO, Bengaluru, Karnataka, India²

Professor, Dept. of Electronics and Communication, NMAM Institute of Technology, Nitte, Udupi District, Karnataka,
India³

ABSTRACT: Future sub meter resolution Cartographic Satellites carry advanced high resolution cameras capable of producing resolution of the images as small as 0.3m. The data rates from these satellites are as high as several Gbps. The transmission band within which the data has to be sent to the ground stations is limited. Hence the data needs to be compressed suitably with a certain loss compression algorithms which minimize the distortions. These satellites need to be designed with modular compression units to cater to high data rate requirements. For higher swath requirements there may be multiple units operating simultaneously, each unit has to be controlled by a controller unit which initializes the compression units before it starts processing the image data. The controller unit has the functionalities like providing the secondary voltage, providing the power reset, configuring and initializing the compression units, loading the NUC(Non Uniformity Correction) parameters, providing the commands and receiving the health of the compression units.

KEYWORDS: MIL-STD 1553B, POL, OVP, SPI, Controller, NUC, Relay, DC-DC.

I. INTRODUCTION

The Base band Data Handling System (BDH) of Remote sensing satellites acquires image data from high resolution payloads formats and transmits to ground through RF interface or stores in Solid Stare Recorder during non-visibility. The data rate from these payloads is very high to be transmitted to ground in limited band width channel. Hence the payload data is compressed in BDH system using efficient compression algorithm. The BDH system comprises of compression boards which can compress the data with less distortion at higher compression ratios. BDH system also incorporates the play back unit with performs channels coding, randomization and formatting of the payload data before transmitting to ground. The current paper discusses about the controller board which configures, commands, provides the secondary voltages and collects the health parameters of compression as well as playback boards. This controller board also acts as a slave to the 1553 bus control unit of the space craft. Controller board receives commands from the 1553 interface to perform the above said functions. The controller board is also used to receive the raw bus from space craft power systems and converts to secondary voltages required for digital logic using DCDC converters, POL and LDOs.

II. CONTROLLER BOARD ARCHITECTURE

The block schematic of the As these satellites collects data from high resolution payloads The Master Controller memory devices such as Static RAM (SRAM), Programmable RAM (PRAM), and Magneto resistive RAM (MRAM) are used for storing elements. The Magneto resistive property gives a small but sufficient signal to distinguish between a "1" and "0". The 160 and 24MHz oscillator is used to generate the clock depending upon the type of frequency band used. Power on Reset (POR) is an electronic device incorporated into the integrated circuit that detects the power

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applied to the chip and generates reset impulses is given to the FPGA circuit. MIL-STD-1553 bus is used for communication between storing elements and buffers. For remote sensing satellites the controller and DC-DC interface is designed. The controller unit is designed for both main and redundant controller. The RAW bus voltage received by the controller is converted into secondary voltages with the help of DC-DC converter. And the over voltage in the circuit is handled by the OVP (Over Voltage Protection). The EL215 relay driver is used to select the secondary voltages using commands given from FPGA. The MIL-STD-1553 bus communication is used as normal bus communication is complex.

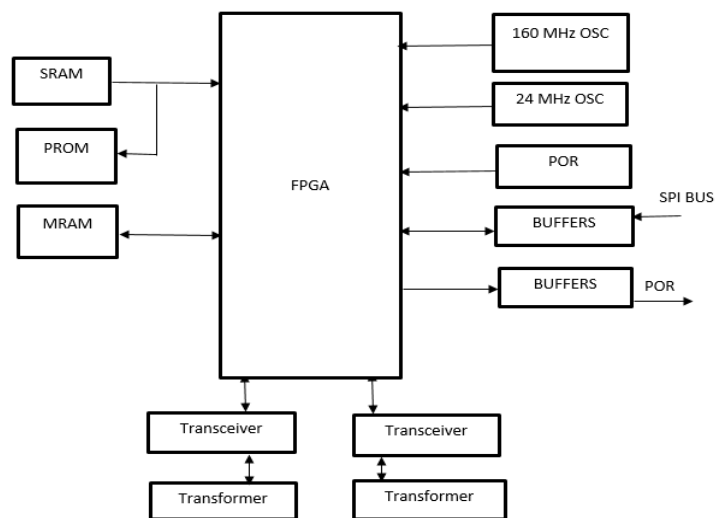


Figure 1: Controller Board Architecture

MEMORY DEVICES: MRAM, PROM, SRAM

MRAM is a non-volatile random access memory which uses magnetic storage and Magneto Resistance (MR) to read the stored data. Magneto Resistive material is a resistor made of common ferromagnetic material which will change in resistance in the presence of a magnetic field. The magneto resistive property gives a small but sufficient signal to distinguish between a "1" and "0". MRAM results from combining MR storage elements with standard semiconductor fabrication processes. The magnetic devices are integrated with support circuits on a single silicon chip to duplicate the function of a static semiconductor RAM chip. **SRAM** is the memory circuit is said to be static if the stored data can be retained indefinitely, as long as the power supply is on, without any need for periodic refresh operation. The data storage cell i.e., the one-bit memory cell in the static RAM arrays. The data being held in the memory cell will be interpreted either as logic '0' or as logic '1'. To access the data contained in the memory cell via a bit line, requires at least one switch, which is controlled by the corresponding word line.

COMPONENT USED: Point of Load, POR, Transceiver

Point of Load: The TPS50601-SP [6] is a 6.3V, 6A synchronous step-down is optimized for small designs through high efficiency and integrating the high-side and low-side MOSFETs. Further space savings are package achieved through current mode control, which reduces component count, and a high switching. Cycle-by-cycle current limiting on the high-side FET protects the device in overload situations and is enhanced by a low-side sourcing current limit which prevents current runaway. There is also a low-side sinking current limit which turns off the low-side MOSFET to prevent excessive reverse current. Thermal shutdown disables the part when die temperature exceeds thermal shutdown temperature. **POR (Power On Reset)** The power-on reset (POR) is an electronic device incorporated into the integrated circuit that detects the power applied to the chip and generates a reset impulses is given to the FPGA. **Transceiver** through MIL-STD-1553 interface, Tele-command reception and Telemetry transfer is carried out.

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Remote terminal is implemented at Baseband Data Handling (BDH) end. Bus communication media is twisted shielded pair. Using this bus standard bus communication is done as shown in Figure 2.

III. BUS COMMUNICATION

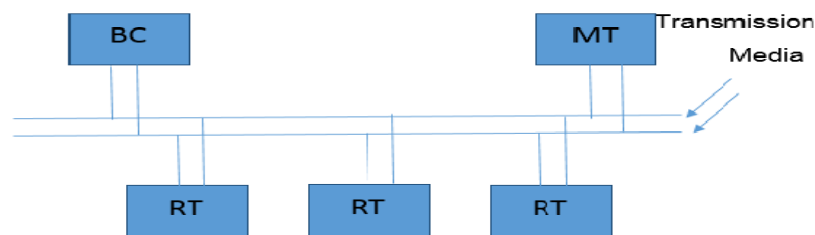


Figure 2: Bus Communication

2.1 The Standard defines four hardware elements

1. Transmission media (or Data Bus)
2. Bus Controller (BC)
3. Remote Terminal (RT)
4. Monitor Terminal (MT)

Bus Controller Provides data flow control for all transmissions on the Bus. Initiates data transfer on the bus Uses Command/response method. Only one Bus Controller may be active at a time. Remote Terminal capable of transmitting or receiving data on receiving the command from Bus controller. With the use of remote sense signals it will receives the signal and transmits the signals it will be controlled by command from the bus controller. RT uses command word information for processing messages. Total number of available sub address = 60 (30 transmit, 30 receive). Two sub addresses 00000 & 11111 are used to designate mode codes. Total number of data words stored in each sub address = 32. Two types of Remote Terminal Embedded RT Sensor or Subsystem that provides its own internal 1553 interface. Stand Alone RT Used to interface and monitor transmissions in and out of non-1553 subsystems. Monitor Terminal that listens to the exchange of information on the data bus and Collects data from data bus. Providing information to backup Bus Controller to take over as the Bus Controller. The standard specifies two methods for a terminal to be connected to the main bus:

1. Direct coupled to main bus
2. Transformer coupled to main bus

The primary difference between the two beings that the transformer coupled method uses an isolation transformer for connecting the stub cable to the main bus cable. In both methods, two isolation resistors are placed in series with the bus. In the direct-coupled method as shown in Figure 3 the resistors are typically located within the terminal, whereas in the transformer-coupled method as shown in Figure 4 the resistors are typically located with the coupling transformer in boxes called data bus couplers.

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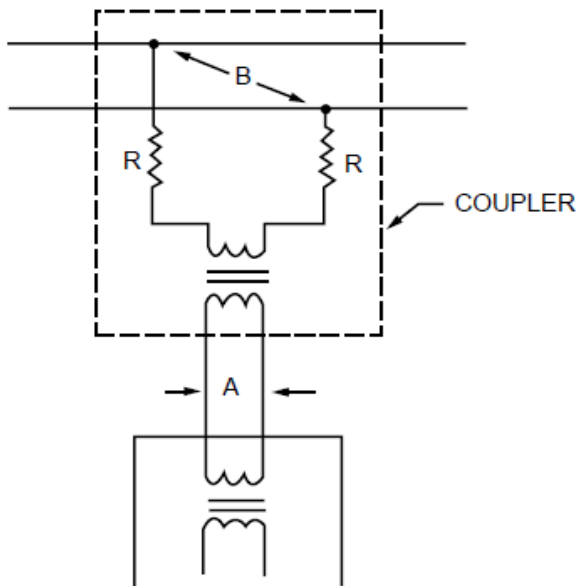


Figure 3: Direct Coupled to main bus [5]

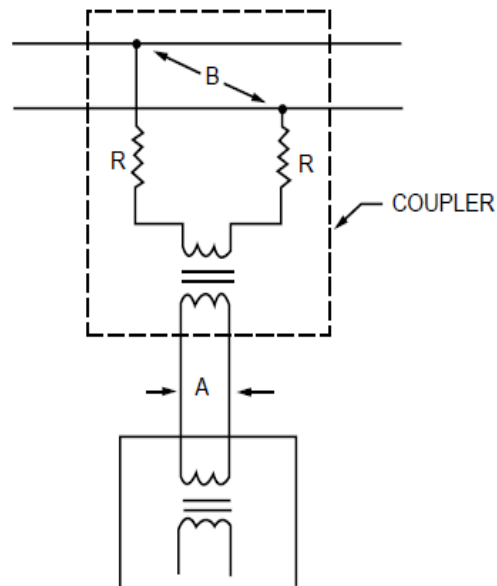


Figure 4:Transformer Coupled to main bus [5]

IV. VOLTAGE SELECTION

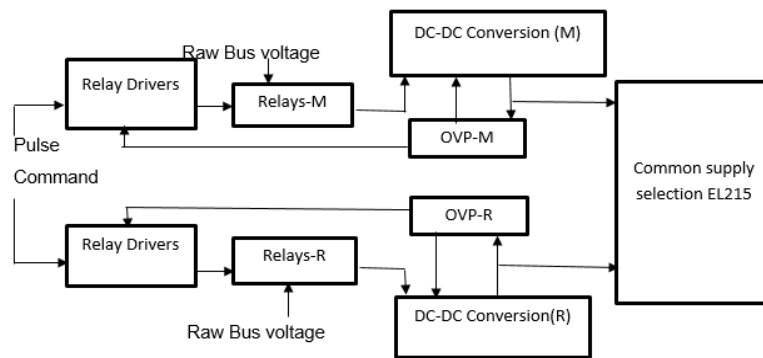


Figure 5: Voltage Selection using EL215

The DC-DC converters which provide power supply to controller and compression boards are turned on using SEL/DESEL and ON/OFF commands. DC-DC converters generated 5V and 3.3V secondary voltages required for FPGA, MRAM, SRAM and other logic devices from RAW bus supply which can vary from 28V to 42V. Two sets of converters are used to take care of single point failure. Supply selection is done using EL215 relay as shown in Figure 5.

V. CONCLUSION

For remote sensing satellites the controller and DC-DC interface is designed. The controller unit is designed for both main and redundant controller. The RAW bus voltage received by the controller is converted into secondary voltages with the help of DC-DC converter. And the over voltage in the circuit is handled by the OVP (Over Voltage Protection). The EL215 relay driver is used to select the secondary voltages.



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