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Low Power CSLA using CMOS Technology

Indushree B¹, Dileep Kumar M. J²

M.Tech, Dept. of E&C, NMAMIT, Nitte, Udupi, Karnataka, India¹

Assistant Professor, Dept. of E&C, NMAMIT, Nitte, Udupi, Karnataka, India²

ABSTRACT: Adders are the basic units to create any data path application or any processor. Carry generation forms the critical path in adders design. Carry Select Adder (CSLA) lists in one of the fastest adders and plenty of data processing processor utilizes this adder to execute arithmetic function. CSLA gives clarity that efficacious and simple gate level attention helps to diminish the consumption of power and area. In this paper modified version of 16-bit CSLA using BEC, D-latch and combinational circuit is compared with 16-bit regular CSLA in terms of power and area.

KEYWORDS: CSLA, RCA, BEC, D-Latch, Combinational, Low power, Area.

I. INTRODUCTION

In Very Large Scale Integrated (VLSI) design, adders have a unique significance and it is used in computer and other processors. In the electronic applications adders are utilized in large area. For instance in microprocessors, there are millions of commands per second are executed. Owing to the like in the probability of the gadgets namely laptops, cell phones etc, need much battery backup [1]. Basically systems and high performance processor demand for area efficient and low power multiplication and addition. For researchers designing of adders is not easier to implement in the VLSI design [4].

CSLA is one of the fast adders. CSLA structure has a chance to decrease area, power and delay [3]. The CSLA contains more area in Carry Look-Ahead Adder (CLA) and small area in Ripple Carry Adder (RCA). CSLA uses pair of RCA to generate partial output by seeing carry input $C_{in}=0$ and $C_{in}=1$, then last terminal outputs are elected by Mux [2-3]. 16-bit CSLA using Binary Excess-1 Converter (BEC), D-latch and combinational circuit has shrunken area and low power consumption. The primary thought of this work is to utilize less transistor level modified structure of 16-bit CSLA (using BEC, D-latch and combinational circuit) instead using regular structure of CSLA with $C_{in}=0$ and $C_{in}=1$ to achieve low power consumption and area [5].

II. REGULAR 16-BIT CSLA

Regular CSLA includes many RCAs of different bit size which are isolated into groups. Group 0 comprises two-bit RCA which adds the input bits and carry; it gives the output as sum [0:1] and the carry out [1]. Group 0 is given to the selection input to Mux present in Group 1, chooses the sum and carry from the respective RCA ($C_{in}=1$) or RCA ($C_{in}=0$). Likewise the rest of the groups will be opted depending on the Cout from the preceding groups. Either of the two RCAs is selected by actual C_{in} from the preceding sector. The output of the upper RCA is opted when $C_{in}=0$ as shown in the Figure 1, and the output of the lower RCA is opted when $C_{in}=1$.

III. 16-BIT CSLA USING BEC

The structure of 16 bit CSLA using BEC is utilized in place of RCA ($C_{in}=1$) to optimize the area and power. Figure 2 shows 16-bit CSLA using BEC. The structure is classified into five groups of various sizes RCA and BEC. RCA ($C_{in}=0$) gives one input to the Mux and one more input from the BEC. The important benefit of this

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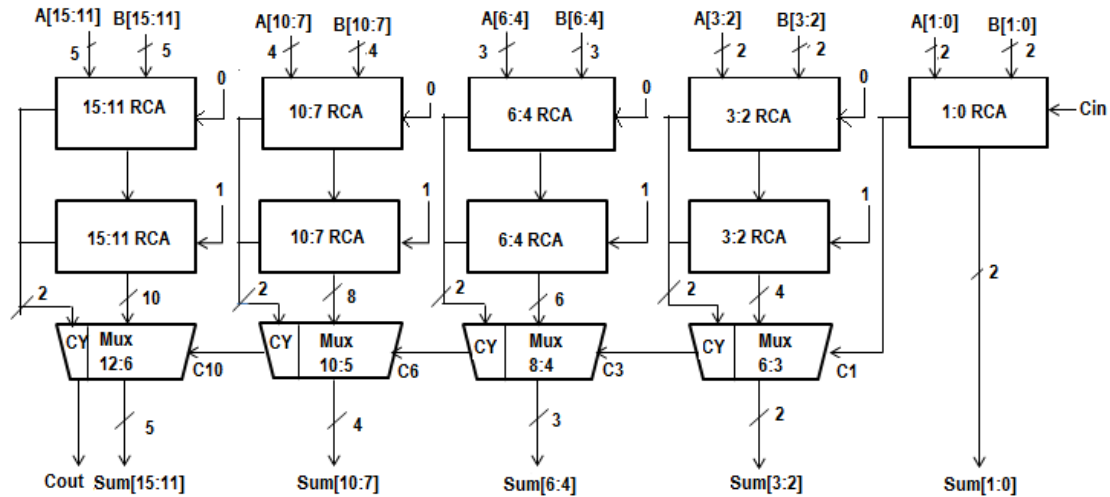


Figure 1: Regular 16-bit CSLA [2]

BEC logic arrives from the lesser number of logic gates over the n-bit Full Adder (FA) structure. It is clearly understood BEC structure cut down the area and power [6].

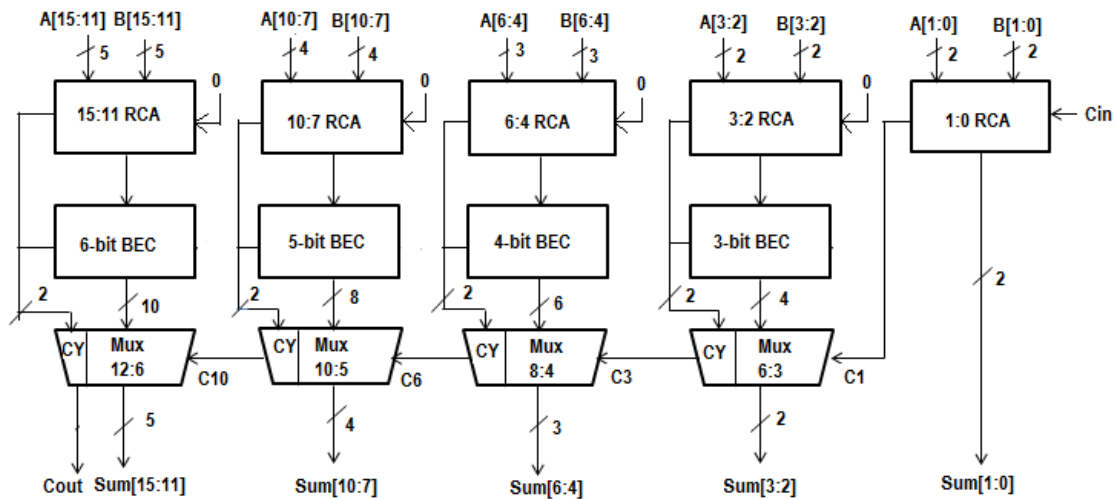


Figure 2: 16-bit CSLA using BEC [3]

IV. 16-BIT CSLA USING D-LATCH

In this 16-bit CSLA using D-latch single RCA is used inspite of utilizing two distinct RCAs in regular CSLA to deplete power consumption and area. At any times when clock is one addition for carry input $C_{in}=1$ is executed. At any times when clock is zero then zero is assumed to be carry input C_{in} and sum is stacked in adder itself. It can infer that latch is used to store the output for $C_{in}=1$. Least Significant Bit (LSB) i.e. (Carry out from the preceding stage) adder is utilized as control signal for Mux to pick terminal output of 16-bit adder. Final output of the latch is elected if $C_{in}=1$ and sum and carry of RCA is elected if $C_{in}=0$.

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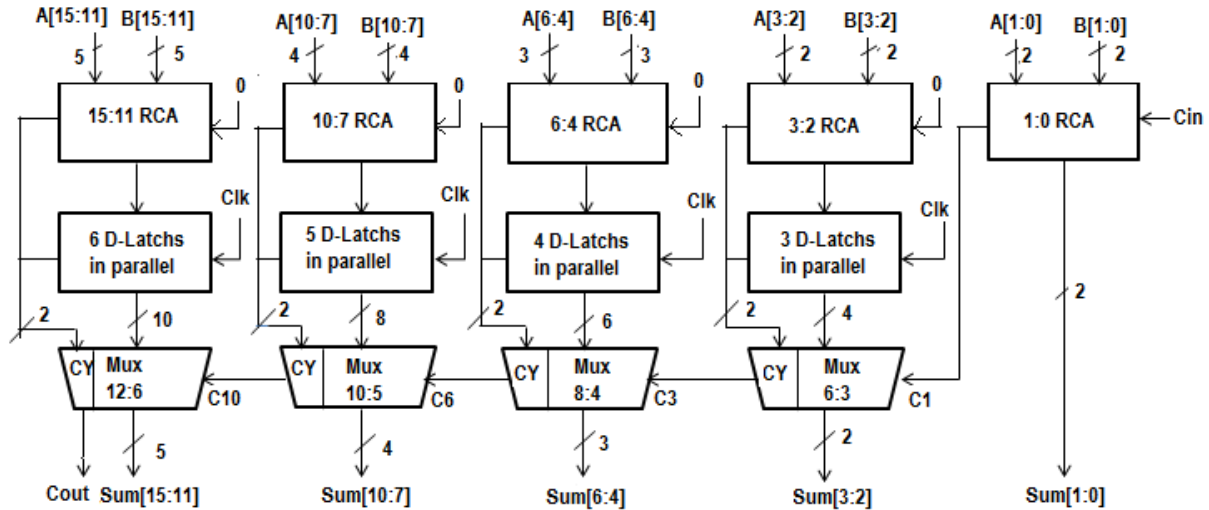


Figure 3: 16-bit CSLA using D-Latch [6]

V. 16-BIT CSLA USING COMBINATIONAL CIRCUIT

In this method Combinational Circuit comprises AND and XOR gates replaces RCA ($C_{in}=1$) and Mux. Comparatively to the regular CSLA, this method decreases the power and area.

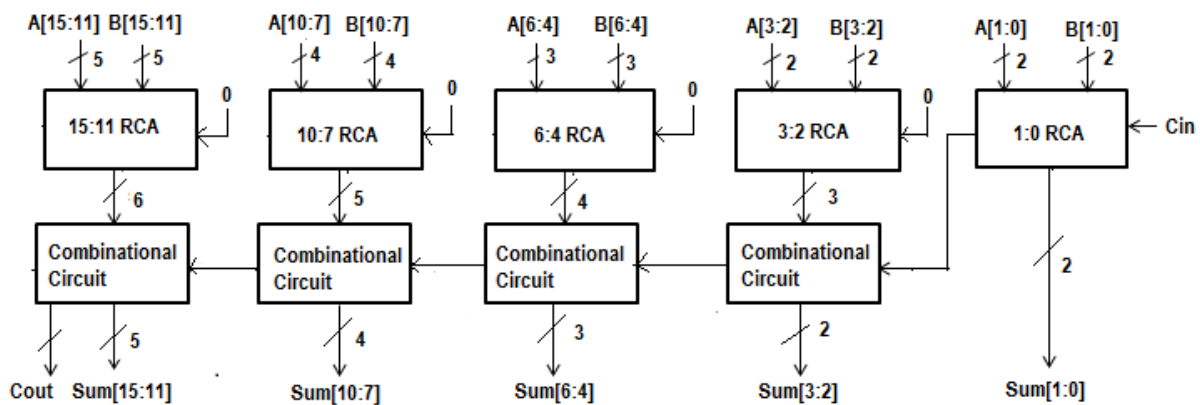


Figure 4: 16-bit CSLA using Combinational Circuit [5]

The structure is classified into groups and variable size of RCA and Combinational Circuit. Initially RCA structure performed operation with $C_{in}=0$ the carry out of RCA is provided to the Combinational Circuit and preceding stage carry out is the input of Combinational Circuit.

VI. SIMULATION RESULTS

The design of 16-bit CSLA using BEC, D-latch and combinational circuit has been analyzed and implemented using Cadence Virtuoso with 180 nm and 45 nm technology. The schematic diagram of 16-bit CSLA using Regular, BEC, D-

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latch and Combinational Circuit is illustrated in Figure 1, Figure 2, Figure 3 and Figure 4 respectively. Table 1 shows the overall comparison of 16-bit CSLA using Regular and modified XOR gate with 180 nm and 45 nm Technology.

Table 1: Overall Comparison of Regular and Modified 16-bit CSLA Structures with 180 nm and 45 nm Technology

| Technology | 180nm | | 45nm | |
|--|------------------|------------|------------------|------------|
| | Transistor count | Power (nW) | Transistor Count | Power (nW) |
| Regular XOR 16-bit CSLA | 2452 | 23.99 | 2452 | 8.98 |
| Modified XOR 16-bit CSLA | 2324 | 23.60 | 2324 | 7.80 |
| Regular XOR 16-bit CSLA using BEC | 1836 | 22.59 | 1836 | 7.13 |
| Modified XOR 16-bit CSLA using BEC | 1744 | 22.30 | 1744 | 6.72 |
| Regular XOR 16-bit CSLA using D-latch | 1472 | 22.13 | 1472 | 6.73 |
| Modified XOR 16-bit CSLA using D-latch | 1372 | 22.00 | 1372 | 6.37 |
| Regular XOR 16-bit CSLA Using Combinational Circuit | 1568 | 21.12 | 1568 | 5.36 |
| Modified XOR 16-bit CSLA Using Combinational Circuit | 1504 | 20.80 | 1504 | 4.93 |

By counting the overall number of AND-OR-INVERTER (AOI) gates area is calculated for individual logic block. General XOR gate consists of two NOT gate, two AND gate and one OR gate whereas modified XOR gate consists of one NOT gate, two AND gate and one OR gate. Hence in modified XOR gate one gate is reduced which helps to reduce the area and power.

VII. CONCLUSION

In order to perform operation of any circuit, power consumption and area are the major areas of the VLSI design process. XOR gate has more transistor count to decrease modified XOR gate is used. Based on gate level implementation it is concluded that the CSLA with RCA is not area efficient so CSLA using BEC, D-Latch and Combinational Circuit had been implemented which consumes less power and area. This CSLA architecture has less power and area, simple and efficient for VLSI applications. The simulation of these adders is carried out in 180nm and 45nm technology Cadence Virtuoso.

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