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Scalable Power and Bandwidth Manipulations with SAR ADC

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ABSTRACT: A successive approximation register analog to digital converter (ADC) with a fixed anti aliasing frequency that allows tradeoffs between power consumption and signal bandwidth is presented. The ADC, without increasing hardware complexity, can reduce power consumption significantly by skipping MSB conversions when they are unnecessary. By sampling and converting only the difference between two successive input samples, DAC capacitor switching power reduces as oversampling ratio (OSR) increases. For OSR = 1, a 1.2 V 10 b 30 MS/s ADC fabricated in 0.18 μm CMOS process consumes 980 μW and achieves signal to noise plus distortion ratio (SNDR) and spurious free dynamic range (SFDR) of 56.2 and 68.6 dB, respectively, resulting in a figure of merit (FOM) of 67 fJ/conversion step for a 14.1 MHz full scale input. For OSR = 16, the ADC dissipating 231 μW from a 1.2 V supply, achieves a FOM of 42.7fJ/conversion-step for a 1.125 MHz full scale input.

I. INTRODUCTION

The first semiconductor chips held two transistors each. Subsequent advances added more transistors, and as a consequence, more individual functions or systems were integrated over time. The first integrated circuits held only afewdevices,perhapsasmanyasten diodes, transistors, resistors and capacitors, making it possible to fabricate one or more logic gates on a single device. Now known retrospectively as small scale integration(SSI), improvements in technique led to devices with hundreds of logic gates, known as medium-scale integration (MSI). At one time, there was an effort to name and calibrate various levels of large-scale integration above VLSI. Terms like ultra-large-scale integration (ULSI) were used. But the huge number of gates and transistors available on common devices has rendered such fine distinctions moot. Terms suggesting greater than VLSI levels of integration are no longer in widespread use.
Structured VLSI design is a modular methodology originated by Carver Mead and Lynn Conway for saving microchip area by minimizing the interconnect fabrics area. This is obtained by repetitive arrangement of rectangular macro blocks which can be interconnected using wiring by abutment. An example is partitioning the layout of an adder into a row of equal bit slices cells. In complex designs this structuring may be achieved by hierarchical nesting.

1.2 DESIGN

A state of art of VLSI IC will have tens of millions of transistors. One human mind cannot assimilate all the information that is required to design and implement such complex chip. A design team comprising hundreds of engineers, scientists and technicians has to work on a modern VLSI project. It is important that each member of the team has clear understanding of his or her part of the contribution for the design. This is accomplished by means of the design hierarchy. Any complex digital system may be broken down into gates and memory elements by successively subdividing the system in a hierarchical manner. Highly automated and sophisticated CAD tools are commercially available to achieve this decomposition. They take very high-level descriptions of system behaviour and convert them into a form that ultimately be used to specify how a chip is manufactured. A specific set of abstractions will help in describing the digital system, which is targeted for a VLSI chip. The behavioural domain specifies what a particular system does.
The structural domain specifies how entities are connected together to effect the prescribed behaviour or function. The physical domain finally specifies how to actually build a structure that has the required connectivity to implement the

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required functionality. The Y-chart each design domain may be specified at a various levels of abstraction such as circuit, logic and architectural. Concentric circles around the centre indicate these levels of abstraction.
Top design Initial Concept level System design and Verification Logic design and Verification CMOS design and Verification Bottom Layout, Placement Design level Routing Mass production, Testing, packaging Marketing. The starting point of a VLSI design of a chip is the system specifications. The specifications will provide design targets such as functions, speed, size, power dissipation, cost etc. This is the top level of the design hierarchy. These specifications are used to create an abstract, high-level model. The modelling is System specifications High-level model VHDL/VERILOG Logic synthesis Circuit design Physical design Manufacturing Finished VLSI chip usually done using a high-level hardware description language (HDL), such as VHDL or VERILOG. Therefore this aspect of modelling a system will not deal here. Using a HDL compiler the functional simulation is done.
The next step in the flow is 'SYNTHESIS'. Synthesiser is a CAD tool software, which generates a gate level net list net list is the description of the logic gates and their interconnections using the VHDL code as an input. This forms the basis for transferring the design to the electronic circuit level. In this level of design, the MOS transistors are used as switches, and Boolean variables are treated as varying voltage signals '0' or '1' for digital in the circuit. Transistors cannot be decomposed further and these are the components, which have to be siliconised. To make a transistor on silicon, one should know the layout details of the same at various integration layer levels. This corresponds to 'physical design'. The physical design level constitutes the bottom of the design hierarchy. After the design process, the VLSI design project moves on to the manufacturing line. The final result is a finished electronic VLSI chip.

II.LITERATURE REVIEW

2.1 A 69-MW 10-BIT 80-M SAMPLES PIPELINED CMOS ADC

Byung-Moo Min, Peter Kim, Frederick W. Bowman, David M. Boisvertand Arlo J. Aude (December 2003)
A 10-bit 80-MS/s analog-to-digital converter (ADC)with an area- and power-efficient architecture is described. Bysharing an amplifier between two successive pipeline stages,a 10-bit pipeline is realized using just four amplifiers with aseparate sample-and-hold block. The proposed feedback signalpolarity inverting (FSPI) technique addresses the drawbackof the conventional amplifier sharing technique. A wide-swingwide-bandwidth telescopic amplifier and an early comparisontechnique with a constant delay circuit have been developed tofurther reduce power consumption. The ADC is implemented in a0.18- m dual gate oxidation CMOS process technology, achieves72.8 dBc spurious free dynamic range, 57.92dBc signal to noiseratio, 9.29 effective numbers of bits (ENOB) for a 99MHz input atfull sampling rate, and consumes 69 mW from a 3V supply. TheADC occupies 1.85 mm.

2.2 A 14-BIT ADC WITH 8 OSR AND 4-MHZ CONVERSION BANDWIDTH IN A 0.18-M CMOS PROCESS

Ruoxin Jiangand Terri S. Fiez (january 2004)
A 14-bit 8 oversampling delta-sigma analog to digital converter (ADC) for wide band communication applications has been developed. By using a novel architecture, a high maximum out of band quantization noise gain (Qmax) is realized, which greatly improves the SNR and tonal behavior. The ADC employs a fifth order single stage structure with a 4 bit quantizer. It achieves 82 dB SNDR and 103 dB SFDR at 4 MHz conversion bandwidth with a single 1.8 V power supply.Delta sigma analog to digital (A/D) converters can achieve high resolution and linearity for low to medium bandwidth applications, such as audio signal processing.

2.3 A 6-BIT 600-MS/S 5.3-MW ASYNCHRONOUS ADC IN 0.13-M CMOS

Shuo-Wei Michael Chenand Robert W. Brodersen, Fellow (December 2006)
An asynchronous analog to digital converter (ADC) based on successive approximation is used to provide a high speed 600 MS/s and medium resolution 6 bit conversion. A high input bandwidth 4 GHz was achieved which allows its use in RF subsampling applications. By using asynchronous processing techniques, it avoids clocks at higher than the sample rate and speeds up a nonbinary successive approximation algorithm utilizing a series nonbinary capacitive ladder with digital radix calibration. The sample rate of 600 MS/s was achieved by time interleaving two single ADCs, which were fabricated in a 0.13 m standard digital CMOS process. The ADC achieves a peak SNDR of 34 dB, while only consuming an active area of 0.12 mm2 and having power consumption of 5.3 mW.

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2.4 AN ULTRA LOW ENERGY 12-BIT RATE-RESOLUTION SCALABLE SAR ADC FOR WIRELESS SENSOR NODES

Naveen Vermaand Anantha P. Chandrakasan, Fellow (June 2007)

A resolution-rate scalable ADC for micro-sensor networks is described. Based on the successive approximation register (SAR) architecture, this ADC has two resolution modes: 12 bit and 8 bit, and its sampling rate is scalable, at a constant figure of merit, from 0–100 kS/s and 0–200 kS/s, respectively. At the highest performance point (i.e., 12 bit, 100 kS/s), the entire ADC including digital, analog, and reference power consumes 25 W from a 1V supply. The ADC's CMRR is enhanced by common-mode independent sampling and passive auto zero reference generation. The efficiency of the comparator is improved by an analog offset calibrating latch, and the preamplifier settling time is relaxed by selftiming the bit-decisions. Prototyped in a 0.18- m, 5M2P CMOS process, the ADC, at 12 bit, 100 kS/s, achieves a Nyquist SNDR of 65 dB 10.55 ENOB and an SFDR of 71 dB. Its INL and DNL are 0.68 LSB and 0.66 LSB, respectively.

2.5 A 10-BIT 50-MS/S SAR ADC WITH A MONOTONIC CAPACITOR SWITCHING PROCEDURE

Chun-Cheng Liu,Soon-Jyh Chang, Guan-Ying Huangand Ying-Zu Lin (April 2010)

This paper presents a low-power 10-bit 50-MS/s successive approximation register (SAR) analog to digital converter (ADC) that uses a monotonic capacitor switching procedure. Compared to converters that use the conventional procedure, the average switching energy and total capacitance are reduced by about 81% and 50%, respectively. In the switching procedure, the input common-mode voltage gradually converges to ground. An improved comparator diminishes the signal-dependent offset caused by the input common-mode voltage variation. The prototype was fabricated using 0.13m 1P8M CMOS technology. At a 1.2V supply and 50 MS/s, the ADC achieves an SNDR of 57.0 Db and consumes 0.826 mW, resulting in a figure of merit (FOM) of 29 fJ conversionstep. The ADC core occupies an active area of only 195265m.

2.6 A 10-BIT 100-MS/S REFERENCE-FREE SAR ADC IN 90 NM CMOS

Yan Zhu,Chi-Hang Chan, U-Fat Chio, Sai-Weng Sin, Seng-Pan U, Rui Paulo Martins and Franco Maloberti (June 2010)

A 1.2 V 10 bit 100 MS/s Successive Approximation (SA) ADC is presented. The scheme achieves high speed and low power operation thanks to the reference-free technique that avoids the static power dissipation of an on chip reference generator. Moreover, the use of a common-mode based charge recovery switching method reduces the switching energy and improves the conversion linearity. A variable selftimed loop optimizes the reset time of the preamplifier to improve the conversion speed. Measurement results on a 90 nm CMOS prototype operated at 1.2 V supply show 3 mW total power consumption with a peak SNDR of 56.6 dB and a FOM of 77 fJ/conv step.

2.7ARESOLUTIONRECONFIGURABLE 5-TO-10-BIT 0.4-TO-1 V POWER SCALABLE SAR ADC FOR SENSOR APPLICATIONS

Marcus Yip and Anantha P. Chandrakasan (june 2013)

A power-scalable SAR ADC for sensor applications is presented. The ADC features a reconfigurable 5 to 10 bit DAC whose power scales exponentially with resolution. At low resolutions where noise and linearity requirements are reduced, supply voltage scaling is leveraged to further reduce the energy per conversion. The ADC operates up to 2 MS/s at 1 V and 5 kS/s at 0.4 V, and its power scales linearly with sample rate down to leakage levels of 53 nW at 1 V and 4 nW at 0.4 V Leakage power gating during a sleepmode in between conversions reduces total power by up to 14% at sample rates below 1 kS/s. Prototyped in a lowpower 65 nm CMOS process, the ADC in 10-bit mode achieves an INL and DNL of 0.57 LSB and 0.58 LSB respectively at 0.6 V, and the Nyquist SNDR and SFDR are 55 dB and 69 dB respectively at 0.55 V and 20 kS/s. The ADC achieves an optimal FOM of 22.4 fJ/conversion step at 0.55 V in 10-bit mode. The combined techniques of DAC resolution and voltage scaling maximize efficiency at low resolutions, resulting in an FOM that increases by only 7x over the 5-bit scaling range, improving upon a 32x degradation that would otherwise arise from truncation of bits from an ADC of fixed resolution and voltage. This is highly suited for proto typing of systems. As there is no fabrication step, this design cycle time is shortest among all the approaches. Only drawback is that the designer may not be able to use the resources on the chip to the full extent.

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2.8 A 0.5 V 1.1 MS/SEC 6.3 FJ/CONVERSION-STEP SAR-ADC WITH TRI-LEVEL COMPARATOR IN 40 NM CMOS

Akira Shikat, Ryota Sekimoto, Tadahiro Kurodaand Hiroki Ishikuro April 2012

This paper presents an extremely low voltage operation and power efficient successive approximation register (SAR) analog to digital converter (ADC). Tri level comparator is proposed to relax the speed requirement of the comparator and decrease the resolution of internal Digital to Analog Converter (DAC) by 1 bit. The internal charge redistribution DAC employs unit capacitance of 0.5 fF and ADC operates at nearly thermal noise limitation. To deal with the problem of capacitor mismatch, reconfigurable capacitor array and calibration procedure were developed. The prototype ADC fabricated using 40 nm CMOS process achieves 46.8 dB SNDR and 58.2 dB SFDR with 1.1MS/se cat 0.5 V power supply. The FoM is 6.3 fJ/conversion step and the chip die area is only 160µm ×70µm.

III. PROPOSED SYSTEM

3.1 INTRODUCTION

ANALOG-TO-DIGITAL converter (ADC) can be divided into two categories: 1) Nyquist-rate; and 2) oversampling, based on the relationship between input signal bandwidth and sampling frequency (*fS)*. Nyquist-rate ADCs, as is well known, process signals whose frequency ranges from dc to Nyquist (*fS*/2). However, in some baseband applications, due to the tradeoff between system level anti aliasing requirements and ADCs sampling rate or input signal bandwidth, Nyquist rate ADCs are clocked at a rate well above the minimum Nyquist requirement, having an oversampling ratio (OSR) >2. Furthermore, digital systems employing oversampling ADCs often have options to change OSR to take advantage of the signal bandwidth and signal-to-noise ratio (SNR) tradeoff.

3.2 BLOCK DIAGRAM

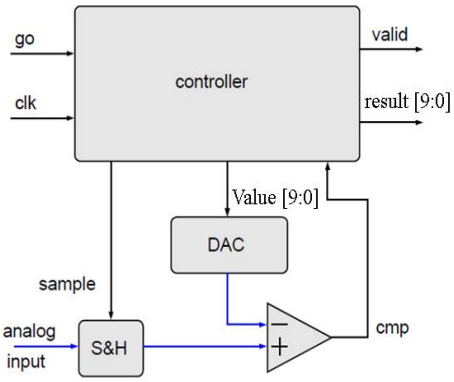

Fig 3.1: block diagram of SAR ADC

3.3 CONTROLLER

In control theory, a controller is a device, historically using mechanical, hydraulic, pneumatic or electronic techniques often in combination, but more recently in the form of a microprocessor or computer, which monitors and physically alters the operating conditions of a given dynamicalsystem. Typical applications of controllers are to hold settings for temperature, pressure, flow or speed

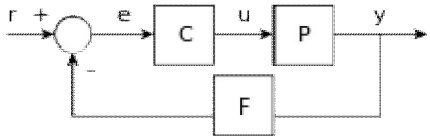

Fig 3.2: linearised model of the ADC

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A simple feedback control loop illustrates that the error signal is received by controller C, which then either attenuate or amplify the input signal to the plant. This signal describes the magnitude by which the output value deviates from the set point. The signal is subsequently sent to the controller C which then interprets and adjusts for the discrepancy.

3.3.1 FEEDBACK

The input to a feedback controller is the same as what it is trying to control - the controlled variable is "fed back" into the controller. The thermostat of a house is an example of a feedback controller. This controller relies on measuring the controlled variable, in this case the temperature of the house, and then adjusting the output, whether or not the heater is on. However, feedback control usually results in intermediate periods where the controlled variable is not at the desired set-point. With the thermostat example, if the door of the house were opened on a cold day, the house would cool down. After it fell below the desired temperature set point, the heater would kick on, but there would be a period when the house was colder than desired.

3.3.2 FEED FORWARD

Feed forward control can avoid the slowness of feedback control. With feed-forward control, the disturbances are measured and accounted for before they have time to affect the system. In the house example, a feed forward system may measure the fact that the door is opened and automatically turn on the heater before the house can get too cold. The difficulty with feed forward control is that the effect of the disturbances on the system must be accurately predicted, and there must not be any unmeasured disturbances

3.4 COMPARATOR

In electronics a comparator is a device that compares two voltages or currents and outputs a digital signal indicating which is larger. It has two analog input terminals V_+ and V_- and one binary digital output V_o. The output is ideally

$$V_o = \begin{cases} 1, & \text{if } V_+ > V_- \\ 0, & \text{if } V_+ < V_- \end{cases}$$

A comparator consists of a specialized high-gain differential amplifier. They are commonly used in devices that measure and digitize analog signals, such as analog to digital converters (ADCs), as well as relaxation oscillators. The differential voltages must stay within the limits specified by the manufacturer. Early integrated comparators, like the LM111 family, and certain high-speed comparators like the LM119 family, require differential voltage ranges substantially lower than the power supply voltages (±15 V vs 36 V). Rail to rail comparators allow any differential voltages within the power supply range. When powered from a bipolar dual rail supply,

$$V_{S-} \leq V_+, V_- \leq V_{S+}$$

or, when powered from a unipolar TTL/CMOS power supply:

$$0 \leq V_+, V_- \leq V_{cc}$$

3.4.1 OP-AMP COMPARATOR

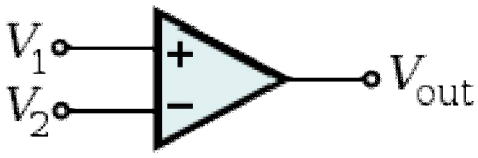

Fig 3.3: A simple op-amp comparator

An operational amplifier (op-amp) has a well balanced difference input and a very high gain. This parallels the characteristics of comparators and can be substituted in applications with low performance requirements. In theory, a standard op-amp operating in open loop configuration without negative feedback may be used as a low performance comparator. When the non inverting input (V+) is at a higher voltage than the inverting input (V-), the high gain of the op-amp causes the output to saturate at the highest positive voltage it can output. When the non-inverting input (V+)

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drops below the inverting input (V-), the output saturates at the most negative voltage it can output. The op-amp's output voltage is limited by the supply voltage. An op-amp operating in a linear mode with negative feedback, using a balanced, split voltage power supply, powered by ± V_S has its transfer function typically written as: $V_{out} = A_o(V_1 - V_2)$. However, this equation may not be applicable to a comparator circuit which is non-linear and operates open loop no negative feedback. In practice, using an operational amplifier as a comparator presents several disadvantages as compared to using a dedicated comparator.

3.5 DAC

DACs and their inverse, ADCs, are part of an enabling technology that has contributed greatly to the digital revolution. To illustrate, consider a typical long-distance telephone call. The caller's voice is converted into an analog electrical signal by a microphone, then the analog signal is converted to a digital stream by an ADC. The digital voice data is then extracted from the packets and assembled into a digital data stream. A DAC converts this into an analog electrical signal, which drives an audio amplifier, which in turn drives a loudspeaker, which finally produces sound.

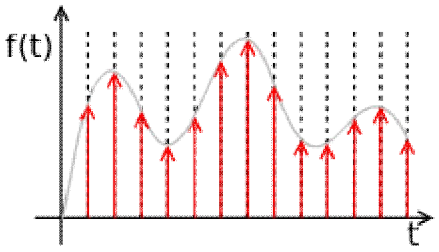

Fig 3.4: Ideally sampled signal

The fact that DACs output a sequence of piecewise constant values known as zero-order hold in sample data textbooks or rectangular pulses causes multiple harmonics above the Nyquist frequency. Usually, these are removed with a low pass filter acting as a reconstruction filter in applications that require it.

3.6 SAMPLE AND HOLD CIRCUIT

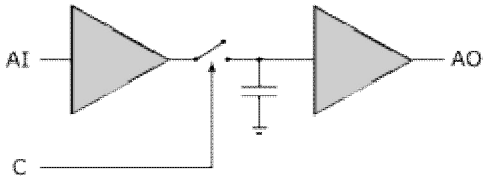

Fig 3.5: A simplified sample and hold circuit diagram.

AI is an analog input, AO an analog output, C a control signal. Sample and hold circuits are used in linear systems. In some kinds of analog-to-digital converters, the input is compared to a voltage generated internally from a digital-to-analog converter (DAC). The circuit tries a series of values and stops converting once the voltages are equal, within some defined error margin. If the input value was permitted to change during this comparison process, the resulting conversion would be inaccurate and possibly unrelated to the true input value. Such successive approximation converters will often incorporate internal sample and hold circuitry

.

IV. RESULT AND DISCUSSION

The ADC, implemented in 0.18-μm CMOS technology, occupies a die area of 0.42 mm^2. The die micrograph. The ADC performances are measured for various OSRs. For OSR = 1, the measured differential nonlinearity (DNL) and integral nonlinearity (INL), shown in Fig. 10, are less than 0.56/−0.44 and 0.82/−0.79 LSB, respectively. The dynamic performances of a full-scale sinusoidal input at 0.5 and 14.1 MHz . The measured signal-to-noise-plus-distortion ratio

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(SNDR) and spurios-free dynamic range (SFDR) are 56.3 and 71.1 dB, respectively. dynamic performance versus input and sampling frequencies. Dynamic performance is well maintained for sampling frequencies up to 30 MS/s. The total power consumption is 980 μW from a 1.2 V supply. Analog circuits including the reference buffer consume 870 μW.

V.CONCLUSION

A power and bandwidth scalable SAR ADC running with various OSRs has been proposed and implemented in 0.18-μm CMOS process. While the ADC works like Nyquist rate ADCs for an OSR of 1, it skips unnecessary MSB capacitor switching by sampling and processing only the difference between two successive samples as OSR increases, resulting in a considerable amount of power saving and linearity improvement. The ADC running at 30 MS/s draws 980 μW from a 1.2 V supply and achieves SNDR of 56.3 dB for a 14.1-MHz input, resulting in a FOM of 67-fJ/conversion step.

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