

A New Three-Stage Buck in Buck, Boost in Boost Grid-Tied Inverter

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ABSTRACT: A new kind of buck in buck, boost in boost grid tied inverter is analysed in this paper. In this family of inverters only a single power stage works at high frequency at a time. This reduces the losses due to switching and hence improves efficiency. There is only minimum filtering inductance in the power loop and over filtering does not take place. The analysis of the operating modes of the inverter is done through the equivalent circuits of various stages in a half-bridge configuration of the inverter. The closed-loop simulation of a 230V/50 Hz, 2kW is included.

KEYWORDS: Grid-tied inverter, buck in buck, boost in boost

I. INTRODUCTION

The use of renewable sources of energy such as solar, wind, hydel etc. is becoming increasingly popular and inevitable due to the depletion of the non-renewable sources such as coal. The new developments in utility grid are being incorporated by many utilities one such development being the smart grid. The journey toward a more intelligent grid structure is expected for all electric utilities. The effect on the grid of large-scale distributed energy resources like wind and solar will force the grid to evolve from a one-way source of power distribution to an intelligent, multi-directional source. Both the society as well as the utility will have benefits from this in the long term. But these welfares can only be achieved if several obstacles regarding the integration of renewable resources and grid are overcome. Hence integration of renewable energy sources and grid is important in the scenario and grid-tied inverter is a method of achieving this integration. The energy scenario in India gives a clear picture of the need for integration of renewable energy sources and grid [1]. At current levels of consumption the reserves of coal may last for 80 years and if all the inferred reserves also materialize it can hold out for over 140 years. India has total reserves of 1201 million metric tonnes of crude oil. Demand for crude oil is anticipated to rise to more than 240 million metric tonnes by 2021-22, and to 465 million metric tonnes by 2031-32.

The grid-tied inverter as the name suggests is a dc to ac inverter which is connected to the grid i.e., the output voltage and frequency are synchronised with the grid along with other parameters. The main application of grid-tied inverters is to convert the DC from solar panels to AC and connect it with the grid. In many countries the enterprise with grid-tied system is allowed to sell the energy to the utility. Two methods of compensation are net metering and feed-in tariff. The method of compensation where the enterprise with a renewable energy source is given a compensation for the net outflow of power is called the net metering method. The method of compensation where the enterprise is paid for every electrical unit (kWh) based on a contract existing between the utility and the enterprise is called the feed-in tariff policy. If a system is connected to the grid, then the generated power has to comply with specific standards, which are regulated by the utility in each country. The main norms that grid connected inverters have to comply with are given in [2].

The grid-tied inverters for the renewable energy sources are becoming widely used today because of acute energy shortage [3], [4]. The pertinent work in this direction starts with locating the proper inverter between the modern grid with all its sophisticated capabilities and the renewable energy resources, again highly modernised. One of the classifications in grid-tied inverters is based on the number of power stages in the inverters:

1. Single Stage Inverters:

The conventional converters are generally of two types voltage-source (or voltage-fed) and current-source (or current-fed) inverters. They can be converters or inverters according to power flow directions. The voltage source converter is widely used. The VSI has certain limitations such as the ac output voltage cannot surpass the dc-bus voltage or in other words the dc-bus voltage has to be more than the ac input voltage. Hence, the VSI performs a bucking action for dc-to-ac power conversion and a boosting action for the power conversion from ac to dc. The devices of a same phase leg cannot be turned on simultaneously. There is a possibility of shoot through which could destroy the devices. Dead time has to be set to both upper and lower devices in the V-source converter. The CSI has certain restrictions like the output ac voltage has to be greater than the dc-bus voltage or the dc output voltage is always less than the ac input voltage. Therefore, the CSI performs a boosting action for dc-to-ac power conversion and bucking action for ac-to-dc power conversion. It is mandatory to maintain any one of the upper or lower devices on at a time. If not maintained on an open circuit of the dc inductor will be produced which may cause damage to the devices. To overcome the problems associated with VSI and CSI, F. Peng put forward a Z-source inverter in [5] or impedance-source (impedance fed) inverter. In the CSI only boost operation is possible [6] and in VSI only bucking operation is possible but in Z-source inverters both buck and boost operation is possible. But there are extra inductors in the ZSI. The control of the ZSI is difficult.

2. Two Stage Inverters:

Here a dc/dc converter is used to convert dc voltage into a suitable value and then converted to ac. There are two stages in these inverters the dc - dc conversion and inverting stage. A traditional two-stage dual mode time sharing inverter is shown in Fig.1 (a). In this topology only a single power stage works at high frequency at a time. This has the advantage that the switching power losses can be reduced. The main drawback of this inverter is that during boost stage over-filtering takes place. The filter used in this is the CL-CL filter.

3. Three stage inverter:

As the name suggests there are three power stages in this type of grid-tied inverter. A boost stage, buck stage and inverting stage are the three stages. The Fig.1 (b) shows a three stage “boost in boost, buck in buck” inverter with LCL filter. The full bridge converter converts dc to ac and is preceded by a boost and buck stage. Here also similar to the two stage inverter over filtering takes place due to CL-CL filter during boost stage.

The converter analysed in the paper is a modification of the inverter above. The boost and buck stages are interchanged to obtain this topology. By doing so one inductor can be saved and associated losses can be avoided. The converter is a buck in buck, boost in boost inverter where only either the boost or the buck stage works at high frequency at a time thereby reducing the switching losses. The topology ensures that there is minimum inductance in the power loop.

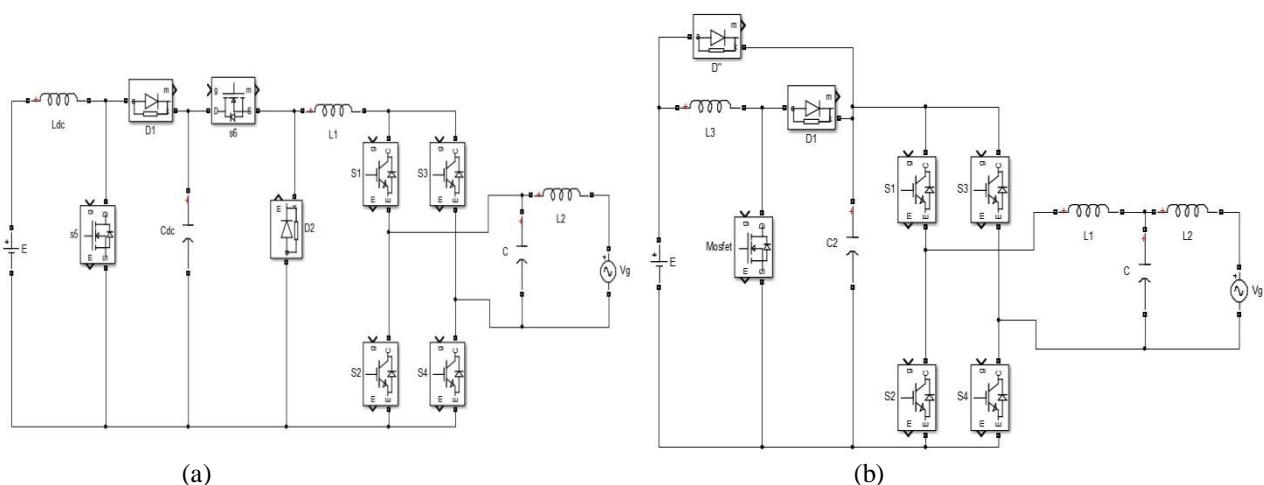


Fig 1: Grid-tied inverters (a) Two stage dual mode time-sharing inverter with CL-CL filter [7] (b) three stage “boost in boost, buck in buck” inverter with LCL filter. [8]

II. BUCK IN BUCK, BOOST IN BOOST CONVERTER

The full bridge configuration is shown in Fig. 2 and half bridge topology in Fig. 3. The converter is a buck in buck, boost in boost converter in which only a single power stage works at high frequency at a time. This reduces the switching losses and minimizes filter inductance thereby avoiding the problem of over filtering. The full bridge topology uses switches S_5 and S_6 at high frequency during boost and buck modes respectively and S_1, S_2, S_3 and S_4 forms the full bridge inverter. In half-bridge topology switches S_1 and S_2 are the switches working at high frequency during buck and boost operations respectively in positive half cycle and S_4 and S_5 are the switches working at high frequency during buck and boost operations respectively in negative half cycle. The switches S_3 and S_6 form the half bridge inverter.

The entire operation is analysed based on the half bridge configuration of the inverter shown in Fig 3. There can be two possible cases:

1. When $|E_1|$ or $|E_2| > V_g$
2. When $|E_1|$ or $|E_2| < V_g$

When $|E_1|$ or $|E_2| > V_g$:

The waveform in Fig.4 (a) clearly illustrates this mode. When $|E_1|$ or $|E_2| > V_g$ only buck operation takes place. During positive half cycle the S_1 is switched at high frequency, S_3 is on throughout the positive half cycle and S_2 is off. The equivalent circuit corresponding to positive half cycle is shown in Fig. 5 (a). During negative half cycle S_4 is switched at high frequency, S_6 is on throughout the negative half cycle and S_5 is off. The equivalent circuit corresponding to negative half cycle is shown in Fig.5 (b).

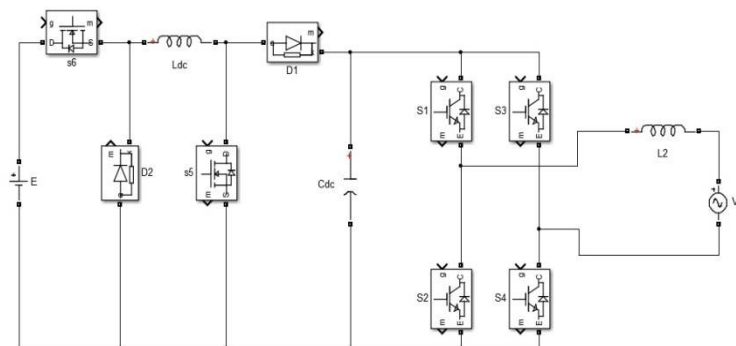


Fig 2: The buck in buck, boost in boost converter in full bridge configuration.

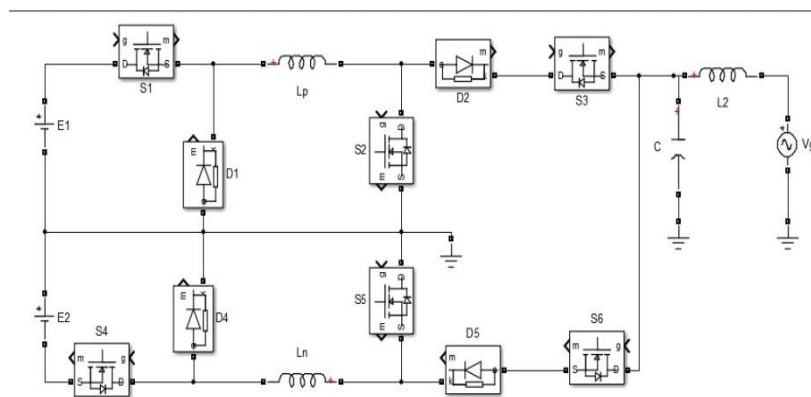


Fig 3: The buck in buck, boost in boost converter in half bridge configuration.

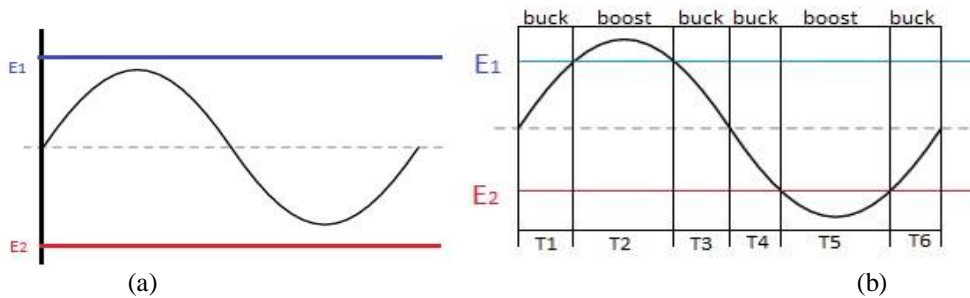


Fig 4: Basic operation principle: (a) When $|E_1|$ or $|E_2| > V_g$ (b) When $|E_1|$ or $|E_2| < V_g$

When $|E_1|$ or $|E_2| < V_g$

During this mode both buck as well as boost operation is required. The whole operation can be split into six intervals as shown in Fig.4 (b). During T_1 buck operation is required. S_1 is switched at high frequency, S_3 is on throughout the positive half cycle and S_2 is off. The equivalent circuit corresponding to positive half cycle is shown in Fig. 5(a). During T_2 boost operation is required so S_1 is kept on while S_2 is switched at high frequency. The equivalent circuit is shown in Fig.5(c). During T_3 again buck operation is required and it is same as the operation during T_1 . During T_4 buck operation is required. S_4 is switched at high frequency, S_6 is on throughout the negative half cycle and S_5 is off. The equivalent circuit corresponding to negative half cycle is shown in Fig. 5(b). During T_5 boost operation is required so S_4 is kept on while S_5 is switched at high frequency. The equivalent circuit is shown in Fig.5 (d). During T_6 again buck operation is required and it is same as the operation during T_4 .

The operation of full bridge configuration is also similar to that of half bridge configuration. The control strategy block diagram in fig. 6(b) clearly illustrates the working of full bridge configuration shown in fig.2.

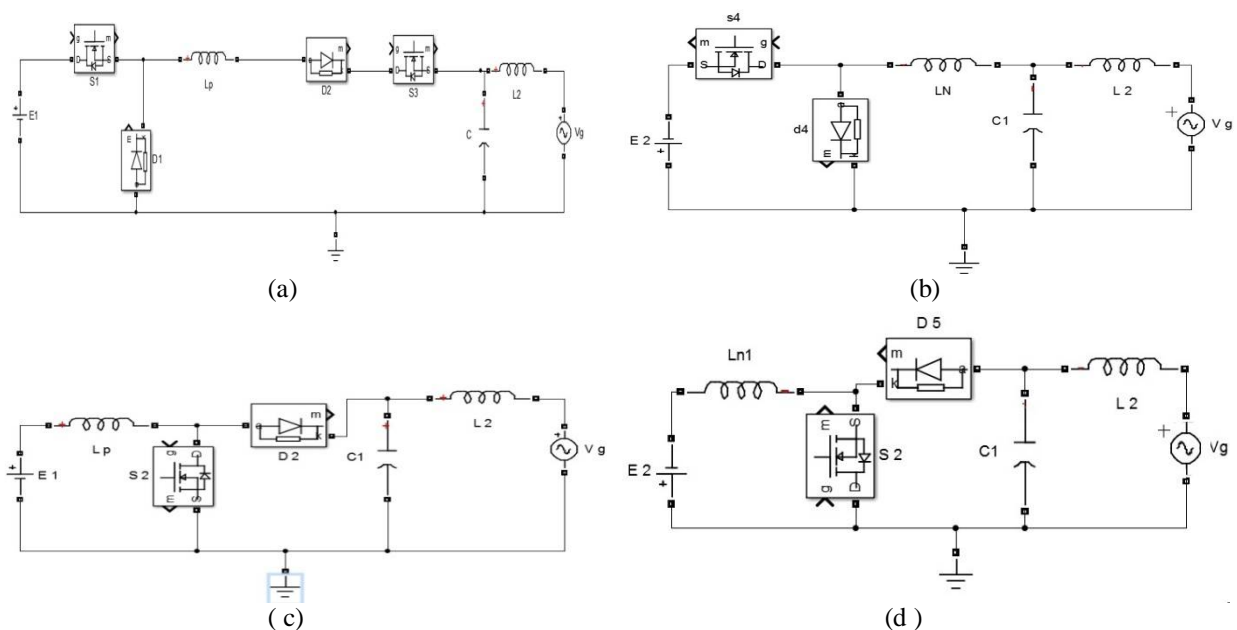


Fig 5: Equivalent circuits: (a) Buck operation in the positive half cycle (b) buck operation in the negative half cycle (c)Boost operation in the positive half cycle (d) boost operation in the negative half cycle

III. CONTROL ANALYSIS

If the instantaneous input power is equal to instantaneous output power the following equation stands true:

$$E(t)i_1(t) = V_g(t)i_g(t) \quad (7)$$

During the boost stage indirect current control is used which means the grid current $i_g(t)$ is controlled by controlling the input current $i_1(t)$. Hence it is named so. In case of half bridge configuration, the switching frequency is 40 kHz for switches $S_1, S_2, S_4,$ and S_5 . The half bridge inverter switches are switched at 50Hz. The parameter design is similar to [9], [10]. When E_1 or E_2 is greater than $V_g(t)$ buck mode is activated and corresponding switches are turned on. When the E_1 or E_2 is less than $V_g(t)$ boost mode is activated and corresponding switches are turned on. In case of the full bridge configuration the switching frequency for S_6 and S_5 is 40 kHz. The full bridge inverter switches are switched at 50Hz. The control strategy block diagrams for the half bridge and full bridge configurations are shown in fig.6(a) and 6(b) respectively. The reference current in buck loop is calculated from eqn. (7) as

$$i_{ref-buck} = \frac{|V_g|}{R_f} \quad (8)$$

Where R_f is the equivalent resistor for obtaining the output power. The reference current in the boost mode can be calculated from (7) as:

$$i_{ref-boost} = \frac{|V_g^2|}{R_f E} \quad (9)$$

Where E may represent E_1 or E_2 in case of half-bridge configuration.

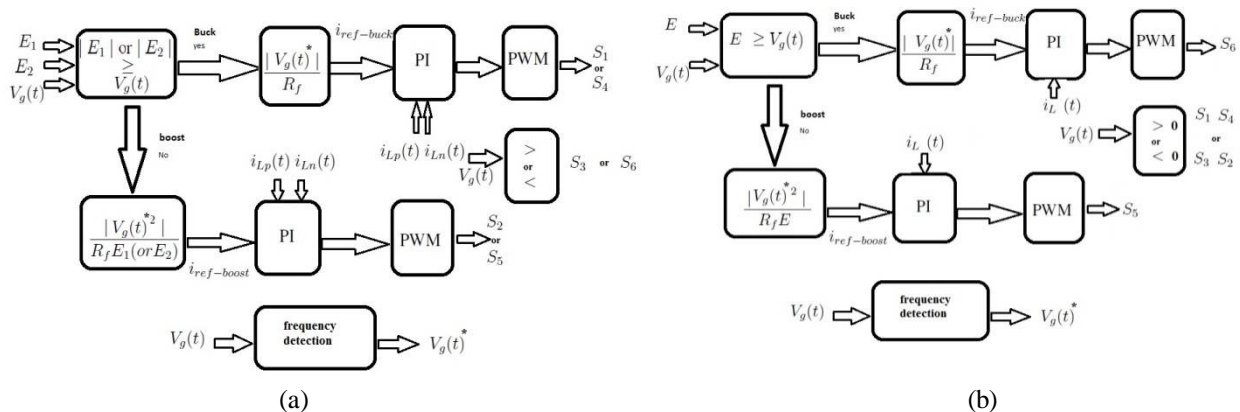


Fig 6: The control strategy block diagram: (a) Control strategy for half-bridge configuration (b) Control strategy for full bridge configuration

IV. SIMULATION RESULTS

The simulation for a 230 V, 50 Hz, 2kW half bridge system was done using Matlab. The design parameters are shown in the table 1:

Table 1: Design values of the components used

Components	Value
L_2	600 μ H
C	2 μ F
L_p, L_n	600 μ H
f_s	40kHz

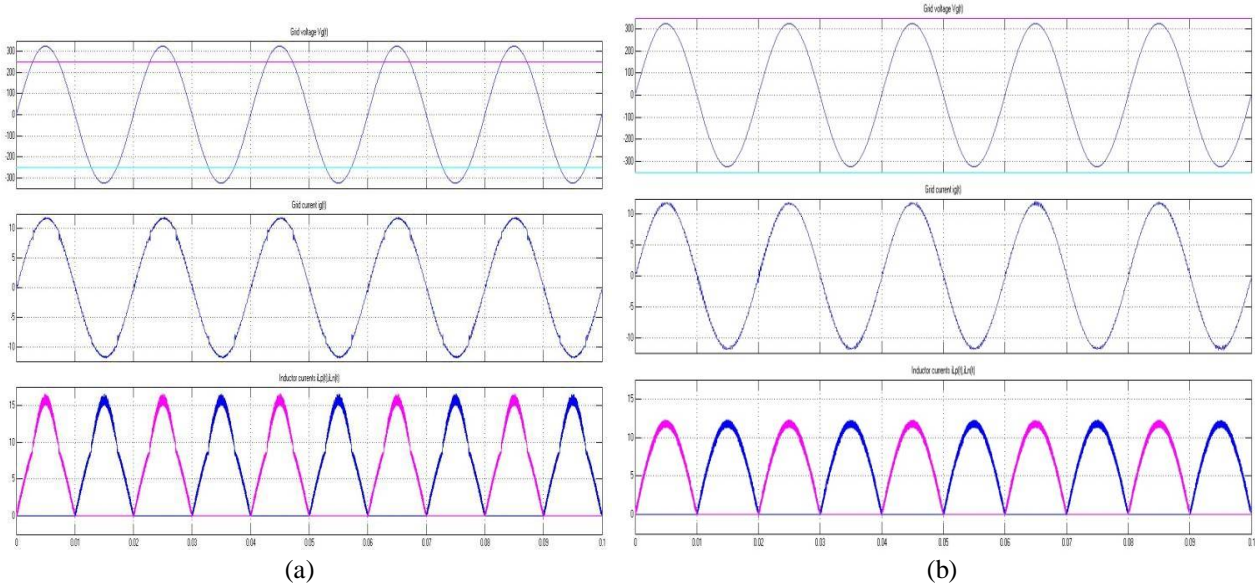


Fig 7: The simulation results: (a) Grid voltage $V_g(t)$, grid current $i_g(t)$ and inductor currents $i_{Lp}(t)$, $i_{Ln}(t)$ when $E_1=E_2=250V$ (b) Grid voltage $V_g(t)$, grid current $i_g(t)$ and inductor currents $i_{Lp}(t)$, $i_{Ln}(t)$ when $E_1=E_2=350V$

The variation of grid voltage $V_g(t)$, grid current $i_g(t)$ and inductor currents $i_{Lp}(t)$, $i_{Ln}(t)$ when $E_1=E_2=250V$, where both buck and boost operations are required is shown in Fig 7(a) and $V_g(t)$, grid current $i_g(t)$ and inductor currents $i_{Lp}(t)$, $i_{Ln}(t)$ when $E_1=E_2=350V$, where only buck operation is required, is shown in Fig 7(b). The variation of $V_g(t)$, $i_g(t)$, $i_{Lp}(t)$ and $i_{Ln}(t)$ when the load changes from full load, 2kW, to half load, 1kW, and back is shown in Fig. 8. The behaviour of the system when there is voltage sag is shown in Fig. 9.

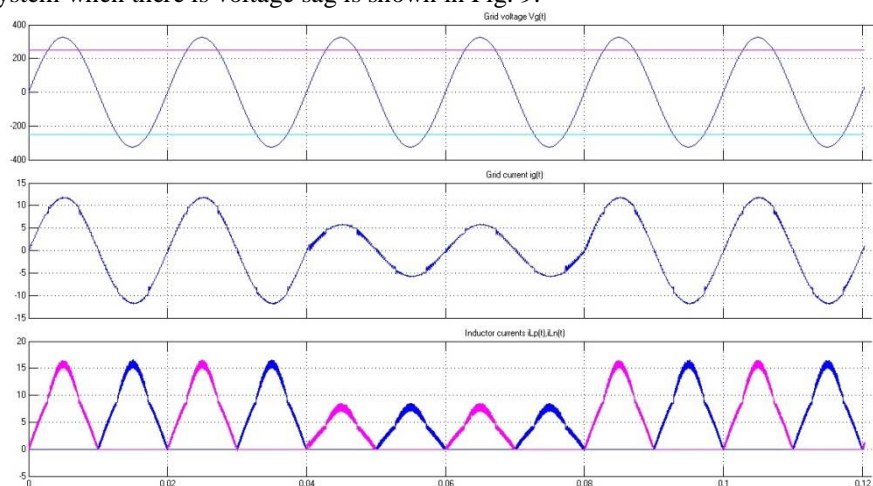


Fig 8: Variation in $i_g(t)$, $i_{Lp}(t)$ and $i_{Ln}(t)$ when the load changes from 2000W to 1000W and back to 2000W.

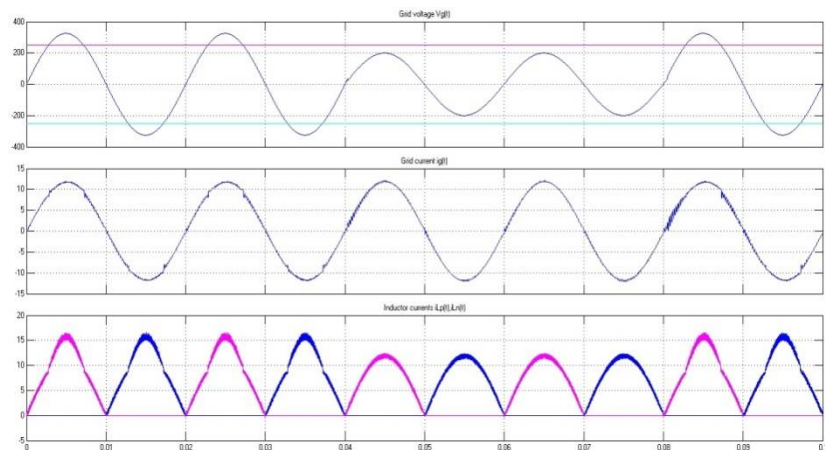


Fig 9: Variation in $i_g(t)$, $i_{Lp}(t)$ and $i_{Ln}(t)$ when there is a voltage sag in the grid voltage from 0.04s to 0.08s

V. CONCLUSION

The principle of operation of a new type of buck in buck, boost in boost grid-tied inverter was discussed using the half bridge topology. The term buck in buck, boost in boost is indicative of the fact that only the buck stage or the boost stage works at a time at high frequency. There is only minimum filtering inductance in the power loop. The closed loop simulation was done for a 230V, 50 Hz, 2kW system.

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