

A New Binary Hybrid Cascaded H-Bridge Multi Level Converter for Electric Vehicle Application

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ABSTRACT: Over the years the concept of multilevel inverters has been widely accepted in the zone of high power industrial and commercial applications. The low level inverters create harmonic distortions in the output voltage and high dv/dt stresses leading to electromagnetic compatibility (EMC) issues and higher harmonic distortion results in malfunction of the device or other extra heating losses. A new approach to voltage source multilevel converter has been proposed here which creates a smoother sinusoidal output waveform reducing the THD (Total Harmonic Distortion). As the number of levels increases the number of power semiconducting devices also increased. In this paper, a new inverter is proposed with lower number of switches and sources in order to acquire maximum level. A 15 level inverter which employs three sources and 10 switches has been developed. The new topology is framed out by cascading three half bridge and a single 'H-bridge configuration. Three isolated dc sources are realized by connecting the battery cells. The voltage level of each source is selected such that it has a binary weighted voltage level. In addition with the reduction of switches, a binary combination of the dc sources is selected for each level to reduce the THD. The performance of proposed converter is evaluated using MATLAB with its Simulink and Simpowersystems. The results verified the performance of the proposed converter.

KEYWORDS: Binary hybrid multi level converter, Cascaded H-bridge converter, 15 level inverter, minimum switch multi level converter.

I. INTRODUCTION

The energy storage system is currently possible with dc power only which is transformed into ac for the high power and low power applications. Most of the commercial and industrial equipment's are made to operate with an alternating current supplies in order to match with the ac supply system. But due to the unavailability of ac power storing devices there arise the need for dc power storage devices for backup, remote power utilization, some lighting, and it reaches the most modern electric vehicle applications. In order to meet the present requirement of electric devices it is necessary to change the zero frequency power to standard frequency, hence emerged the various inverter topologies and control techniques [1-2].

Inversion of direct current into alternating current is an established idea, but the quality of inverted power is the main concern behind every technique [3] focus on the power quality issues at the inverter output. Inverters can be voltage source and current source type. The power quality of the inverter output is entirely depends upon the inverter design and control techniques. The ultimate aim is to match the inverter output more smoother sinusoidal and hence to decrease the harmonic contents of the output. There are different methods available for design and control of the inverter to obtain nearly sinusoidal output by decrease the THD. The harmonic content present in the electrical device input or the output of the inverter produce unwanted switching losses and circulating harmonic current produce unnecessary heating of the machine and results derating of the machine and results aging of the electrical machines [4-6].

Designers are now paying more attention to save electric energy by reducing the harmonics. By increasing the number of levels, the THD is reduced considerably but this result in increase in number of switches and the corresponding

switching losses. Obviously the control and gate driver circuit for the inverter get complex and bulky which results high cost and heavy size of the overall system. It is difficult to change the square wave output into sinusoidal but possible with high valued filters, results losses and reduction in the rms output voltage. Multilevel inverters are introduced to solve most of the above mentioned problems [7-12].

The number of levels can be obtained by changing the design and control of the switches. Basic two level inverter is first proposed and it is famous for its simplicity and small size. The two level inverter is used for induction motor drives [13], for the active filters [14-16]. For the electric vehicle application using high power dc storage, a multilevel inverter is reported [17]. This inverter has low weight and size and therefore compromising the THD. The dynamic voltage restorer (DVR) with neutral point clamped Multilevel Inverter has been reported [18]. DVR based on the flying capacitor multilevel inverter is also presented [19]. However, these structures have a greater number of switches and require additional components such as diodes and capacitors. The cascaded H-bridge converters are used for the voltage balance of the battery cells [20-21]. Each H-bridge cell is here used to control one battery cell then the voltage balance can be realized by the separate control of charging and discharging of the cells. One major advantage of using multilevel inverter is to reduce the filter inductance. Voltage balance control of the battery cells used in STATCOM can be realized by the adjustment of the modulation ratio of each H-bridge [22]. A hybrid cascaded multilevel converter is reported [23] and the ac output of the converter is multilevel voltage, while the number of voltage levels is the number of cascaded battery cells therefore for a greater number of levels that much battery units and corresponding switching devices are necessary.

A new binary hybrid cascaded H-bridge multilevel inverter (BHCMLI) is proposed in this paper which can combine the source selection according to the binary weighted pattern and inversion of the dc link voltage with the help of an H-bridge converter. The application of the multilevel inverter is retained and the proposed system is simulated in the MATLAB SIMULINK software.

II. PROPOSED CONVERTER

A desired ac voltage can be taken from the H-bridge sides of the proposed new binary hybrid cascaded H bridge multilevel converter for ac power applications such as motor drive, using in active filters, or to connect to the power grid. The ac output of the converter is multilevel voltage as the name implies and an efficient energy management algorithm is developed for switching battery units according to the binary pattern, hence the number of voltage levels are greater than the total number of battery units. It will reduce total harmonic content of the converter output. By appropriate switching of the dc sources, it can get different steps in the output voltage waveform creating smoother output. Each source is associated with two switches and one for switching ON the source (1, 2&3) and another for switching OFF the source (1', 2'&3'). These switches will determine the number, duration and the delay of the multilevel output. Figure 1 shows the total circuit configuration of the proposed circuit where the dc link voltage is taken from the terminals a and b and the output ac is taken from the Vout terminal. All the sources are not same in potential level and the crucial selection of these sources are according to the binary pattern.

Generalizing,

$$V_n = 2^{(n-1)} \times 12 \text{ Volt} \quad (1)$$

Where V_n is the n^{th} source voltage capacity.

$$V_1 = 12 \text{ V}, V_2 = 24 \text{ V}, V_3 = 48 \text{ V} \dots \dots \text{ so on.}$$

The total number of levels available in the output waveform

$$k = 2^{n+1} - 1 \quad (2)$$

Maximum Output voltage,

$$V_{max} = (2^n - 1)12 \text{ Volt} \quad (3)$$

From the Figure 1 it is clear that using a three sources of 12 V, 24V and 48 V are selected in order to get the multilevel output. The maximum number of levels = $2^{3+1}-1=15$ levels.

$$V_{max} = 84 \text{ Volt}$$

The circuit operates with an eight modes and each mode describe each voltage level. The function of the serially connected half bridges is to create a stepped dc link voltage. For an ideal sine wave, it is necessary to create a multi-

level dc link voltage input to the H-bridge converter. Every mode shows different levels of output and it starts from 0 volt to 84 volt. As the total eight modes complete, the circuit will create a 90 degree output voltage and overall the 180 degree time period is obtained. In order to keep the output frequency as desired grid frequency, it is required to create a control signal with the same frequency for the H-bridge will decrease the switching complexity. The upper switches in the half bridge circuit are numbered numerically and the lower switches are numbered as compliment of the upper switch of the same arm. From the naming itself it is clear that the upper and lower switches in the same leg of the half bridge are complimentary switches. All the three half bridge legs are connected in series and cascaded with an H-bridge.

Dividing the each output stages as modes and each mode corresponds to each voltage. It will generate up to 84 volt as number of steps of size 12 volt therefore maximum eight steps and corresponding eight modes of operations and during each mode, voltage is referred in between the terminals a and b. Mode 1 gives the total short circuiting of load or zero voltage across the load. The first mode can be generated by turning on the switches 1', 2' 3' or else turning off all the switches. Both will give same output voltage but the first trial will give a freewheeling path to the load current. Therefore choose a conducting zero voltage output as shown in figure 2.

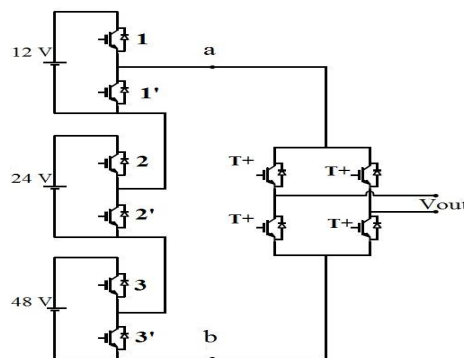


Figure 1. Proposed converter circuit

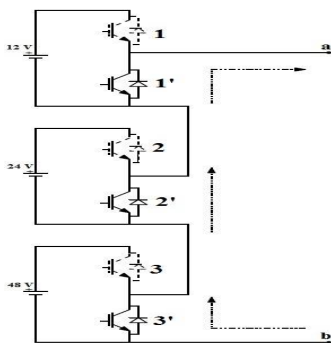


Figure 2. Mode I- 0 Volt

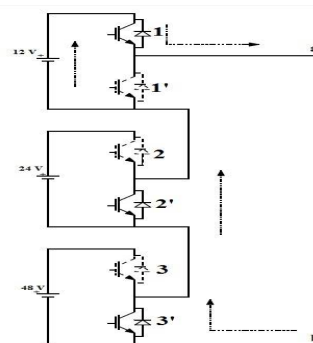


Figure 3. Mode II- 12 Volt

The 12 volt can be created by turning on the switch 1 and remaining all are as before. At this time, only one switch in the upper side is turned on and the first source will selected as 12 volt and produce 12 volt output. It can generalize the switches into upper half switches and lower half switches. The transition from one mode to another is achieved by controlling the half bridge switches. Similarly, next level of voltage is 24 volt and it can achieve by turning ON the second source only and turning OFF the 12 and 48 Volt sources. Similarly it is easy to analyze the modes of operations. The figures 4 and 5 show output voltage levels of 24 volt as the third mode and 84 Volt as mode VIII. When the circuit operates at the VIIIth mode, output reaches 90 degrees and a maximum voltage of 84 volt. All the upper switches of the half bridges are turned ON and all lower ones are turned OFF. Figures 4-5 shows the selection and bypassing of the sources for the desired levels of output. The intermediate modes of operations are present for generating desired output levels and they are self-explanatory.

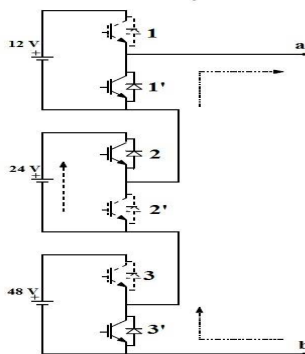


Figure 4. Mode III- 24 volt

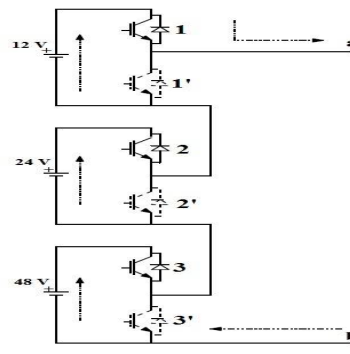


Figure 5. Mode VIII- 84 volt

III. CONTROL SIGNAL GENERATION

First step of control signal generation is by coding the each step of the expected output wave form by binary digits. For that, design the required output waveform with desired dc levels. Positive and negative regions are distinguished by finding the repeating sequence. The period is set for normal grid frequency and each step duration is calculated according to this time period. Now assign the binary coded decimal values for each step as shown in figure 6. B0, B1, B2 decimal values are determined and the repeating sequence and its period, delay, duration all can be found. The total control of the switches will obtain from the binary coding of the expected output is shown in Figure 6.

A. Switching Logic

Considering total three sources and six switches, two switch per source. Appropriate switching gives required DC voltage levels across the terminal a-b. Table 1 shows the switch position and the voltage available corresponding to the binary bit positions. According to the binary rule, bit is 0 means the corresponding switch is OFF, and 1 for the ON position of the switch.

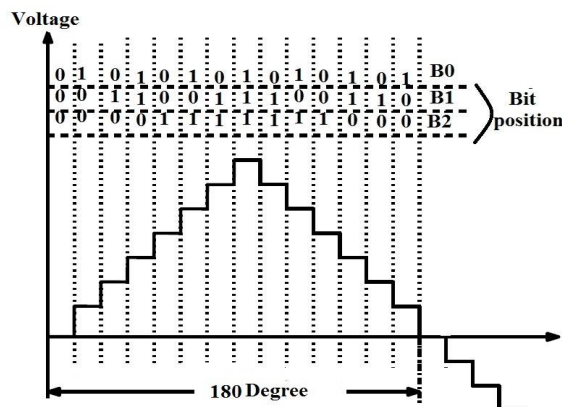


Figure 6. Expected DC Link Voltage and respective binary coding

Table 1. Switching Logic

Binary bit Condition	Corresponding switch	Voltage output
B0=1	1 ON 1' OFF	12 V
B0=0	1 OFF 1' ON	0 V
B1=1	2 ON 2' OFF	24 V
B1=0	2 OFF 2' ON	0 V
B2=1	3 ON 3' OFF	48 V
B2=0	3 OFF 3' ON	0 V

B. Control Signal Design

In order to get lowest THD output, it is required to change the step size that matching with an original required sine wave. For an ideal sinusoidal output voltage, pulse width is modulated according to the requirement. In this paper the sine wave is assigned to pass through the midpoint of each voltage levels which will create a lower minimum THD output voltage. The maximum available number of steps are fixed and the duration of the pulses is modulated analytically is shown in Figure 9.

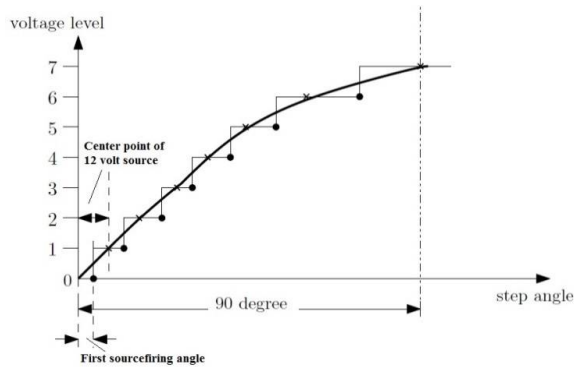


Figure 8. Pulse Width Modulation

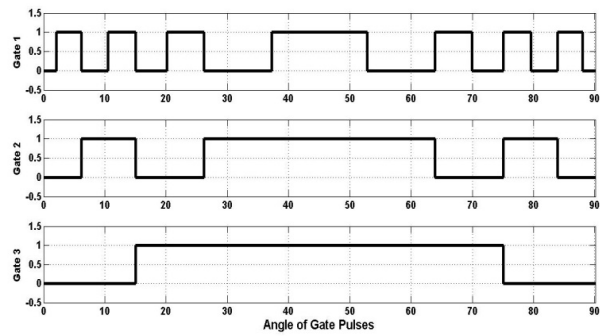


Figure 9. Control Signal Pattern

IV. SIMULATION MODELING AND RESULTS

Control signals are generated with the help of pulse generators and logic gates. Control signal to the switches are generated in open loop and it is shown in Figure 10.

Combination of the switches over a period gives required repeating dc levels is then applied to an inverter. Figure 11 shows the input to the inverter H-bridge and it is measured in between the terminals a and b. Simulation result is shown in the Figure 12 and the result reveals that there are eight levels in the positive side (including zero) and seven levels in the negative half. The reversal of the supply occurring at the zero levels, it will decrease the switching stress and hence dv/dt can be greatly reduced. When taking an overall period there are fifteen levels.

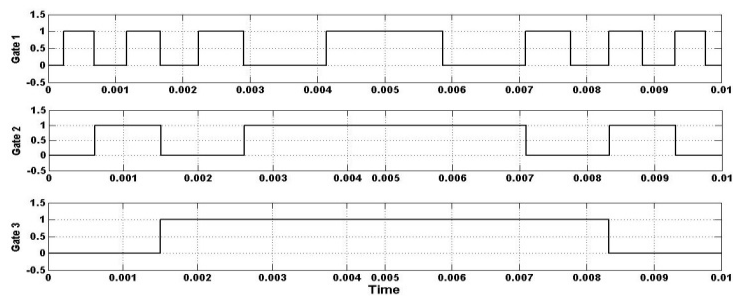


Figure 10. Control signal Generated

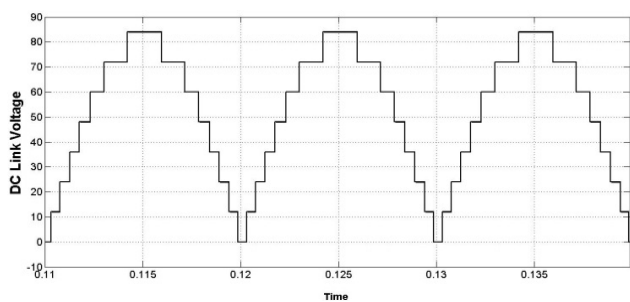


Figure 11. DC link voltage

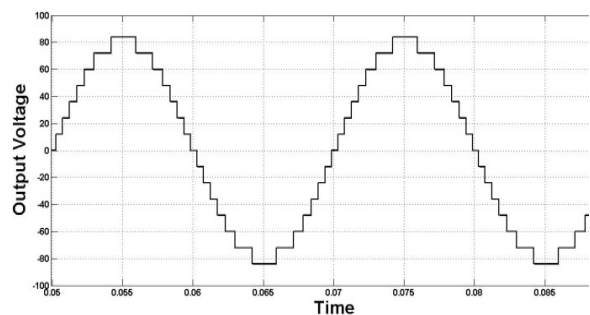


Figure 12. Output Voltage waveform

The FFT analysis of the given output waveform is shown Figure 13, from the figure it is evident that the fundamental component is 82.75% and the THD is 6.07%.

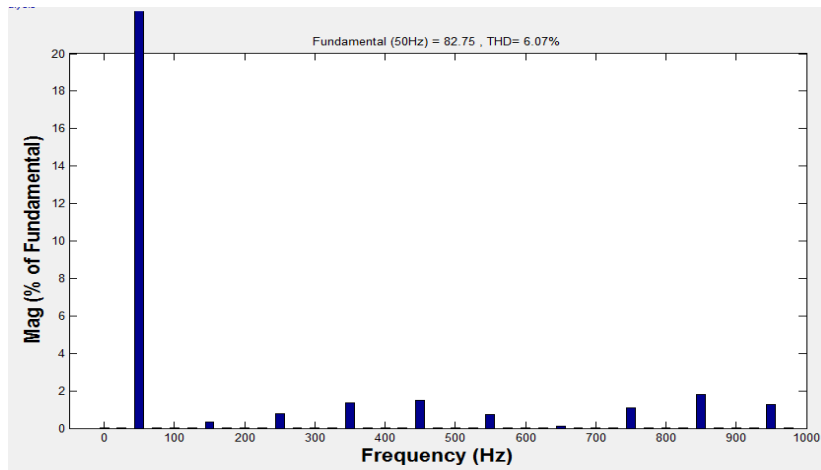


Figure 13. FFT analysis result of output voltage

V. CONCLUSIONS

A new 15 level inverter with optimum number of switches and sources has been designed and the performance is verified. The proposed binary hybrid cascaded H-bridge multilevel converter consists of three sources and ten switches. The total harmonic distortion (THD) of the obtained output voltage is 6.07% which is acceptable in a multilevel inverter. For a fixed level, number of sources is reduced and the use of large number of cells connected in series is avoided. Multilevel voltages with less harmonic is helpful to improve the performance of the motor drives in electric vehicles. Total weight and size of the module is reduced compared to reported cascaded modules. Effective use of the sources can be ensured by using this topology and maximum combination achievement is the main attraction of the converter. Inverter side switching at the zero voltage level decreases switching stress at the H-bridge converter switches.

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