

# High Power Factor Bridgeless SEPIC Rectifier for Drive Applications

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**ABSTRACT:** Rectifiers are mostly used as the front end converters in drive applications like volt per hertz speed control of induction motors, traction drives, textile industries etc. Front end converters suffer from many problems like poor power factor, harmonics, switching losses, low efficiency etc. Bridgeless topologies can resolve many of these issues. In bridgeless converter, conduction losses are reduced as the number of simultaneously conducting components on input current path is lesser than conventional converters. In this paper a bridgeless Single Ended Primary Inductance Converter (SEPIC) PFC rectifier suitable for drive application is presented which has minimum number of components, less conduction losses and high power factor. Conventional SEPIC PFC rectifier with input rectifier bridge circuits have large size and high switching stresses. The modified bridgeless SEPIC rectifier having multiplier stage gives better efficiency at low input voltage, low inrush current, low magnetic emissions and reduced switch voltage stress than existing bridgeless topologies available so far. A step-up bridgeless single phase ac-dc power factor correction (PFC) rectifier based on SEPIC topology is proposed for many applications. The absence of an input rectifier bridge and the presence of only two semi conductor switches in the current flowing path during each switching cycle result in less conduction losses and improved thermal management compared to the conventional full bridge topology. The new circuit is compared with the existing full-bridge SEPIC rectifier in terms of efficiency, THD, and power factor. This new rectifier is then used as the front end converter for speed control circuit of induction motor. Detailed converter analysis, comparison with open loop and closed loop simulation of the SEPIC rectifier along with overall simulation are presented. The simulation results show that the circuit can attain power factors about 0.95 and THD of 4.04 % for input voltage of 230 V.

**KEYWORDS:** SEPIC, Total harmonic distortion (THD), Power Factor Correction (PFC), Active Front End (AFE)

## I. INTRODUCTION

Recently the demand for improving power quality of ac system has become a great concern due to the rapid increase in electronic equipments in the customer side. To reduce harmonic contamination in power lines and to improve the transmission efficiency [1], for electrical engineers and designers, PFC research has become an attractive topic in power electronics. In fact, the PFC circuits are becoming mandatory on power supplies where more strict power quality regulations and strict limits of input current THD are imposed. Power supplies with active power factor correction (PFC) techniques [2] are becoming necessary for many types of electronic equipment to meet harmonic regulations and standards, such as the IEC 61000-3-2.

The equipment connected to an electricity distribution network usually require some kind of power conditioning, mostly rectification, which produces a non-sinusoidal line current due to the non-linear input characteristic. In both single and three-phase rectifiers, a large filtering capacitor is usually connected across the rectifier output to reduce the ripple in the DC. As a consequence, the line current become non sinusoidal. The presence of nonlinear loads leads to high harmonics and results in poor power factor at the input side and also poor power quality. Most power factor correction topologies now a days uses a boost-type circuit configuration at its front end because of its low cost and its high performance in terms of efficiency, power factor and simplicity.

It is analysed that the boost converter operating in discontinuous current mode (DCM) [3]-[4] can have a number of advantages such as inherent PFC function, very simple control, soft turn-on of the main switch, reduced diode reverse recovery losses etc. However, the DCM operation requires a high quality boost inductor since it must switch extremely

high peak ripple currents and voltages. As a result, a more rated filter at the input must be employed to suppress the high-frequency components of the pulsating input current, which increases the overall weight and cost of the rectifier. The PFC circuits with boost converter at the DC-DC converter stage also suffers from many limitations like, large sized EMI filter, input-output isolation cannot be implemented easily, larger PFC inductance, high start up inrush current, and there is a lack of current limiting during overload conditions [6]. To overcome the problems associated with boost type PFC converters, especially in universal applications where the output voltage is lower than the input voltage, the step up/down converters such as buck-boost, cuk, Single Ended Primary Inductance Converter (SEPIC) etc. can be used. Among them a SEPIC converter offers several advantages as it can be used for both step up and step down operation [7]. Also unlike the buck-boost and cuk topology, polarity of the output voltage is not reversed and thereby the control and protection circuits can be easily implemented [6]. Also if the input inductance is high, input current will have lesser ripples, thereby EMI filter requirements are reduced.

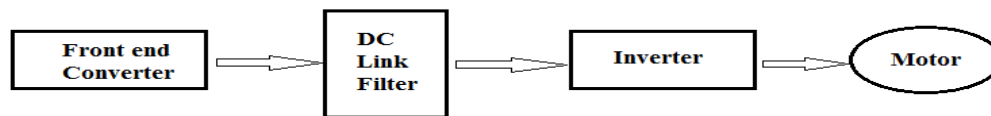


Fig. 1. Components of an induction motor drive.

In a normal motor drive, the rectifier is made of diodes. But with an Active Front End (AFE) converter these are replaced with an active switching devices like MOSFET or IGBT. This active rectifier creates canceling harmonics that effectively eliminate those created in standard VFDs [5], [8]. The Fig. 1 shows the components of an AFE rectifier based drive system, including front end converter, DC link filter, and the inverter. Because of its series installation, the active rectifier needs to be able to transmit the full power of the load. In addition to performing harmonic correction, the active front end rectifier has the ability to feed electrical energy back to the utility during braking. AFE drives usually have very low current distortion (often down to 5% THD) and high power factor. The ability to feedback braking energy is very useful in drive applications [8], while in others, AFEs are only installed for their effectiveness in reducing harmonic distortion.

The main problems associated with the front end converter in drive applications are the presence of harmonics due to non linear rectifier and occurrence of low power factor. These two main problems thus create power quality issues. By using proper PFC rectifiers, these issues can be limited to some extent [5].

The Single Ended Primary Inductance Converter (SEPIC) rectifier with several advantages such as step up and step down capabilities in addition to magnetic coupling leading to reduction in input current ripple[10]-[11] is considered as a solution to reduce the power quality issues in drive applications. In this paper the bridgeless SEPIC PFC rectifier [12] is compared with basic SEPIC rectifier [9] in terms of power factor, THD and voltage stress by matlab simulation and it is verified by the simulation results that the closed loop SEPIC rectifier at rated single phase voltage gives better THD and very good power factor about 0.995 which is near to unity. This rectifier is then used as the front end converter for driving a three phase induction motor whose matlab simulations are created. The simulation results proved that the THD of the entire drive system is improved and operates at desirable power factor .

This paper is organised as section II describes working of SEPIC rectifier, section III explains the design of the rectifier and in section IV simulation results are discussed and section V gives the conclusion.

## II. SEPIC RECTIFIER

Single ended primary inductor converter (SEPIC) is a type of DC-DC converter allowing the electrical potential (voltage) at its output to be greater than, less than, or equal to that of input voltage, the output of the SEPIC is controlled by the duty ratio of the switch. The conventional SEPIC rectifier[9] is having a diode bridge at the input side. The bridgeless topologies discussed in[10]-[11] have several advantages, but it has three extra passive elements which increase the volume and weight of the converter. But the major problem with this converter is that it doubles the output voltage which considerably increases the size of output filter. To overcome these restrictions, a new bridgeless SEPIC PFC rectifier[12] suitable for front end converter is discussed in this paper. . In this rectifier, the number of component is reduced and it gives high efficiency due to the absence of the full-bridge diode. However, in

this converter, an input inductor with large inductance has to be used in order to reduce the input current ripple. The operating principle of the bridgeless SEPIC rectifier is explained by the circuit diagrams in three modes of operation with the support of necessary graphs [12].

### Comparison of bridgeless SEPIC with conventional

The SEPIC rectifier with input bridge [9] has a lot of limitations owing to the inclusion of four diodes which not only increases the conduction loss, but the overall size and weight also. The bridgeless SEPIC rectifier suffer from the inclusion of high value inductor in the circuit in order limit the input current ripple, and hence harmonics. Both these rectifiers are taken in to consideration and are analysed using matlab simulation. The simulation result of SEPIC rectifier with bridge shows higher THD about 65 % and lower power factor about 0.83 lag., while that of bridgeless closed loop SEPIC rectifier shows lower THD about 4 % and very good power factor about 0.995 which is very near to unity. The simulation results for various input voltages are summarised and shown on the table. 2.

### SEPIC rectifier with feed back

The above discussed bridgeless SEPIC rectifier was modelled and simulated in matlab for closed loop operations. Here output voltage is sensed and fed back to the input so that the closed loop control is provided. A PI controller is used for this purpose [12]. The simulation results shows that the input current is almost sinusoidal which indicates lower harmonics and good power quality. The output voltage become constant after a small transient time interval and it become steady which is shown in Fig. 7.

## III. DESIGN AND RATINGS OF COMPONENTS

A bridgeless boost converter is widely used in advantage of reduced input current ripple, but its output voltage should be higher than the peak voltage of the input voltage. Relatively low output voltage of PFC converters is required in many applications such as low-voltage switched-mode power supplies. PFC buck converters are more suitable for these applications due to their low output voltage.

A SEPIC PFC converter can provide a high power factor regardless its output voltage due to its step up/down function, several bridgeless single ended primary inductor converters (SEPICs) were proposed. The efficiency of these converters is improved by removing the input bridge diode. However, buck input inductor or another LC filter is required to suppress the input current ripple. In this section, the components of the modified circuit will be designed and the operation of the circuit with the calculated values will be validated using simulation in the coming section IV.

### a ) Voltage Conversion Ratio M

Average diode current over half-line cycle is calculated using the following equations,

$$I_{DO} = \frac{1}{\frac{T_L}{2}} \int_0^{\frac{T_L}{2}} i_{do} dt \quad (1)$$

where  $T_L$  is the period of the line voltage and  $i_{do}$  is the average output diode current over a switching cycle. Hence, the average current of diode  $D_o$  over half-line cycle can be presented by

$$i_{DO} = \frac{dI^2 T_s V_m}{T_L L e} \int_0^{T_L/2} \frac{\sin^2 \omega t}{M - \sin \omega t} dt \quad (2)$$

From the above two equations we get,

$$di = \sqrt{\frac{Km}{\alpha}} \quad \text{Where } \alpha \text{ is the duty ratio and } K \text{ is found by } \frac{2 Le}{T_s RL}$$

### b ) Inductor Design

The inductor values are calculated using inductor current ripple equation shown below

$$\Delta i_{L1} = \frac{V_{ac}(t)}{2L1 \, d1 \, Ts} \quad (3)$$

The input inductances  $L_1$  and  $L_2$  can be calculated as bellow,

$$\frac{1}{Le} = \frac{1}{L1} + \frac{1}{L2} + \frac{1}{Lo} \quad (4)$$

### c ) Capacitor Design

The energy transfer capacitors  $C_1$  and  $C_2$  are important elements in the proposed topology since their values greatly influence the quality of input line current. These capacitors are designed under the following constraints.

The resonant frequency between ( $L_1, C_1, Lo$ , and  $C_2$ ) during DCM stage of the switching cycle shown in Fig. 5 must be much greater than the line frequency ( $f_L$ ) to avoid input current oscillations at every line half cycle and lower than switching frequency ( $f_s$ ) to assure constant voltage in a switching period,

$$f_L < f_r < f_s \quad (5)$$

$$\text{where } f_r = \frac{1}{2\pi\sqrt{(L1+Lo)(C1+C3)}} \quad (6)$$

Based on the conditions above, the value of  $C_1 = C_2 = C_3 = 1.2 \text{ F}$  is chosen for this particular design.

### d ) Output Capacitor $C_o$

The output capacitor must be large enough to minimize the output voltage ripple since the output voltage ripple frequency is twice the input line frequency. The output filter capacitor ( $C_o$ ) is determined as in bridgeless SEPIC rectifier discussed above. For an output voltage ripple which equal to 2 percentage of the output voltage, the output capacitance is expressed as

$$C_o = \frac{1}{\Delta V_{co}} = \left( \frac{d1^2 Ts Vm^2}{4LeVa} \left( \frac{Tl}{8} + \frac{Tl}{4\pi} \right) - \frac{VoTl}{4Rl} \right) \quad (7)$$

$$\text{Where, } V_{c1} = \frac{Vo - Vm}{2} \quad (8)$$

A simplified design is presented in this section to determine the component values of the new rectifier for the following power stage specifications. The values are in standard units.

- 1) input voltage = 230 V at 50 Hz
- 2) output voltage = 560 V
- 3) output power = 400 W
- 4) switching frequency  $f_s = 50 \text{ kHz}$
- 5) maximum input current ripple  $i_{L1} = 10 \%$  of fundamental input current
- 6) output voltage ripple  $v_o = 2 \%$  of  $V_o$ .

The table .1 shows the components used in the modified SEPIC rectifier with their values with type and ratings.

Table.1 Components used in modified SEPIC rectifier

Sl no.	Parameter	Value	Type
1	Inductor L1 & L2	2.2 mH	Toroid inductor DC4- 2200, 4 A
2	Inductor Lo	180 micro H	Toroid inductor DC4- 180, 11.4 A
3	capacitor C1, C2 & C3	1.2 micro F	Polypropylene 1000 V
4	Capacitor Co	1000 micro F	Electrolytic 450 V
5	Diodes Dp & Dn	-----	SBR 10U 300CT Schotky, 600V
6	Diodes D1, D2 & Do	-----	BY 329 Fast recovery, 1000 V, 8A
7	Switches Q1 & Q2	-----	STW34NM60ND 600 V, 29 A

The load resistance  $R_L$  is designed according to the requirement of output power which is 400 W here. Hence the resistance is determined by the fundamental equation,  $R = \frac{V^2}{P} = \frac{560^2}{400} = 784$  ohms , which is approximately equal to 800 ohms. The switching frequency is determined according to the requirement of output voltage and power.

#### IV. SIMULATION AND RESULTS

##### a ) SEPIC rectifier with bridge

The SEPIC rectifier with bridge [9] has been simulated using the calculated components as per the simulink diagram shown in Fig. 3 and then it is compared with the simulation of modified bridgeless SEPIC rectifier [12] whose simulink diagram is shown in Fig. 5. The simulation results, waveforms are observed and THD analysis is done by simulink THD spectrum. The input, output waveforms and THD spectrum are shown in Fig. 2 and Fig. 4 respectively. The simulation results are tabulated for various input voltages along with various other parameters which can be seen on Table. 2.

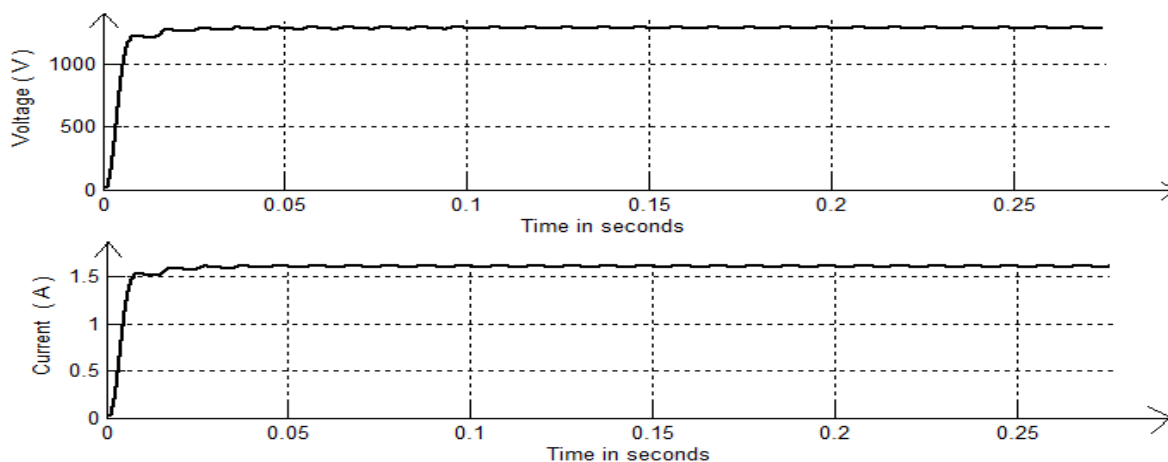


Fig. 2 Output waveforms of the SEPIC rectifier with bridge.

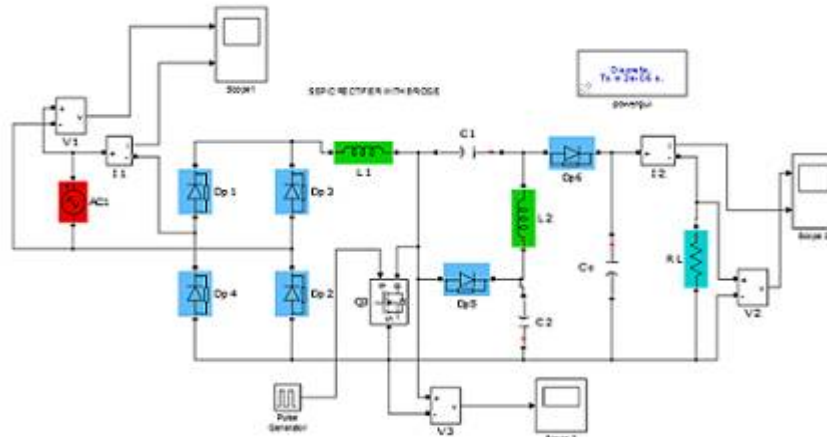


Fig. 3 Simulink diagram of the SEPIC rectifier with bridge.

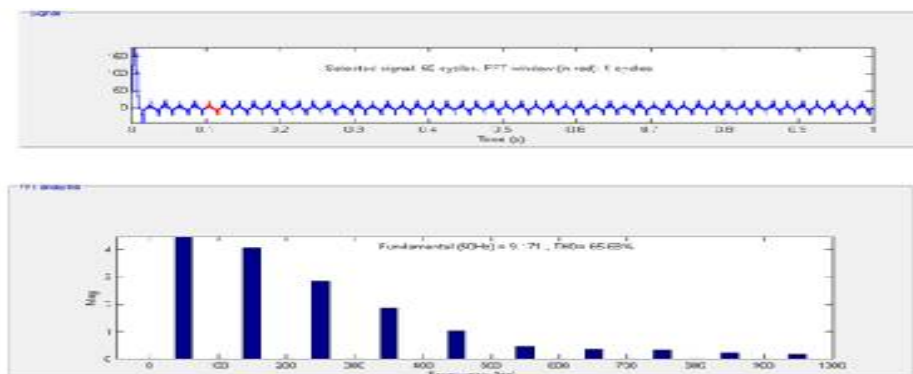


Fig. 4 FFT spectrum of the SEPIC rectifier with bridge.

Here the SEPIC rectifier is simulated in matlab for various input voltages including the standard single phase voltage, that is 230 V. For various input voltages the corresponding measurements are taken by connecting proper meters and display which are available in simulink library. It is observed that THD is around 65 % which is undesirable value as far as PFC rectifiers are concerned. More over the power factor is also shown to be less in value. These parameters are entered on table .2 for the sake of comparison.

Table. 2 Simulation result of SEPIC rectifier with bridge.

SL NO.	Parameters	Vin 100 V	Vin 150 V	Vin 230 V	Vin 300 V
1	Input current	0.01	0.02	0.025	0.03
2	Output voltage	424.6	640	985	1287
3	Output current	0.53	0.80	1.23	1.61
4	Switch voltage	3	4.88	7.88	10.5
5	THD	65.84	65.75	65.68	65.65
6	Power factor	0.82	0.83	0.83	0.83

**b ) Bridgeless SEPIC rectifier with feed back**

Here a feedback system is provided which sense the output voltage and given to the PI controller. Depending on the variations of the output voltage, the PI controller reacts accordingly so that the voltage output remains constant at any time.

The matlab simulations are carried out based on the simulink diagram shown in Fig. 5 and the results are observed. THD analysis is got from simulink THD spectrum shown in Fig. 7 and the output waveforms in Fig. 6 . The table. 3 shows the parameters of the rectifier at various input voltages.

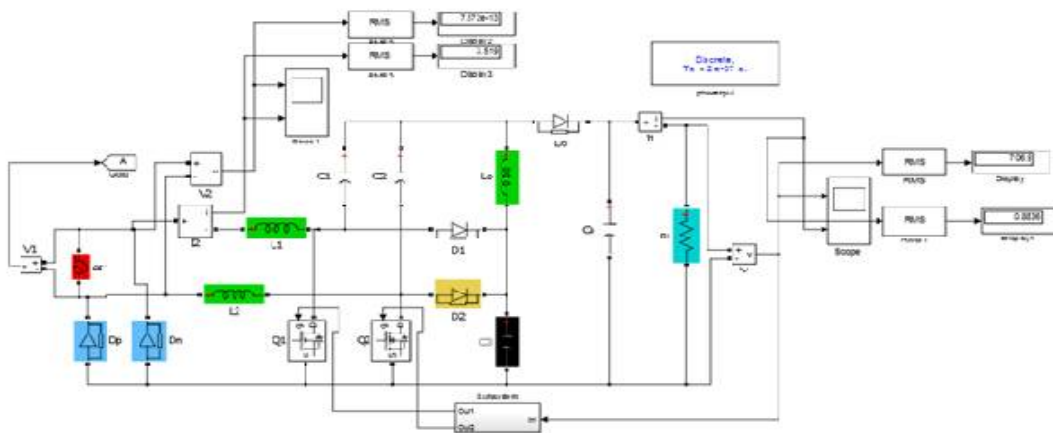


Fig. 5 Simulink model of Bridgeless SEPIC rectifier with feedback.

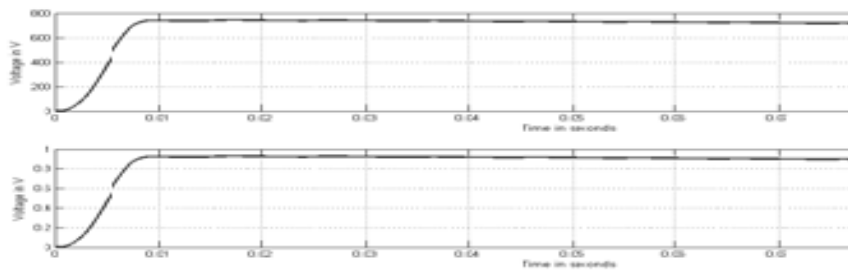


Fig. 6 Closed loop bridgeless SEPIC rectifier Output waveforms.

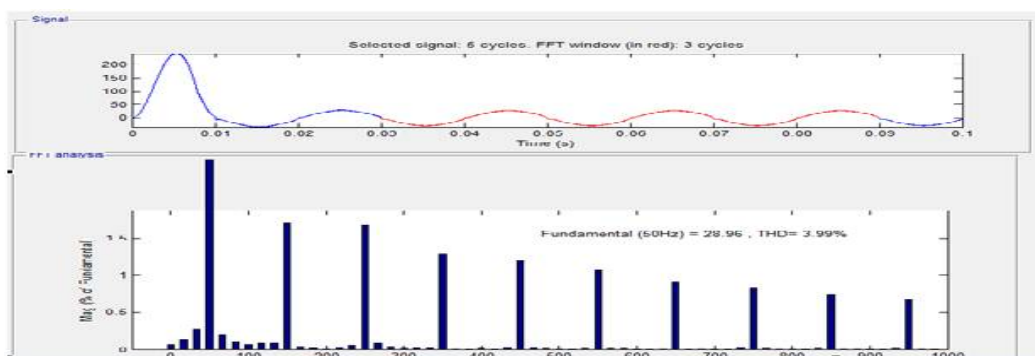


Fig. 7 Closed loop bridgeless SEPIC rectifier FFT spectrum.

Table.3 Closed loop bridgeless SEPIC rectifier simulation results.

SL NO.	PARAMETERS	Vin 100 V	Vin 150 V	Vin 230 V	Vin 300 V
1	Input current	9.9	4.55	3.52	4.59
2	Output voltage	483	582	707	879
3	Output current	0.60	0.73	0.88	1.09
4	Switch voltage	3	4.88	7.88	10.5
5	THD	12.75	7.08	3.99	4.09
6	Power factor	0.98	0.99	0.995	0.995

In this paper, the Bridgeless PFC circuit based on SEPIC converter has been discussed and simulated in matlab. It is seen that the bridgeless circuit is capable to achieve high power factor and low THD under normal input supply voltage. This circuit is therefore most suitable to be used as a front end converter for variable speed drives especially in volt per hertz control application as the quality of power is improved.

**C) Volt per hertz speed control of induction motor**

The induction motor speed variation can be easily achieved by either stator voltage control or rotor resistance control. But both of these schemes result in very low efficiencies at low speeds. The most efficient scheme for speed control of induction motor is by varying supply frequency. This not only results in scheme with wide speed range but also improves the starting performance. If the machine is operating at speed below base speed, then v/f ratio is to be kept constant so that flux remains constant. This retains the torque capability of the machine at the same value. .

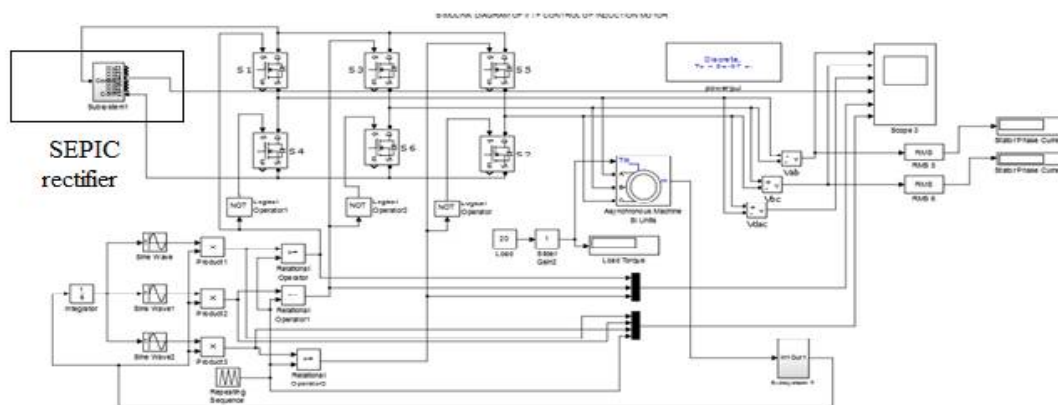


Fig. 8 SEPIC rectifier as front end converter for IM drives.

Here the SEPIC rectifier is used as the front end converter for speed control of induction motor using volt per hertz control method. Usually in volt per hertz control, it requires a converter and an inverter. Here the SEPIC PFC rectifier is used as the front end converter and it is followed by a three phase inverter. The output voltage and frequency of the inverter is controlled and hence the speed of induction motor also. The motor used is 5 HP, 3ph, 440 V, 50 Hz and 1440 rpm. The power quality problems can be limited by using the bridgeless SEPIC rectifier at the front end. The overall simulink diagram is shown in Fig. 8. Here the bridgeless SEPIC rectifier is used as a sub circuit using matlab tools and the entire system is simulated.



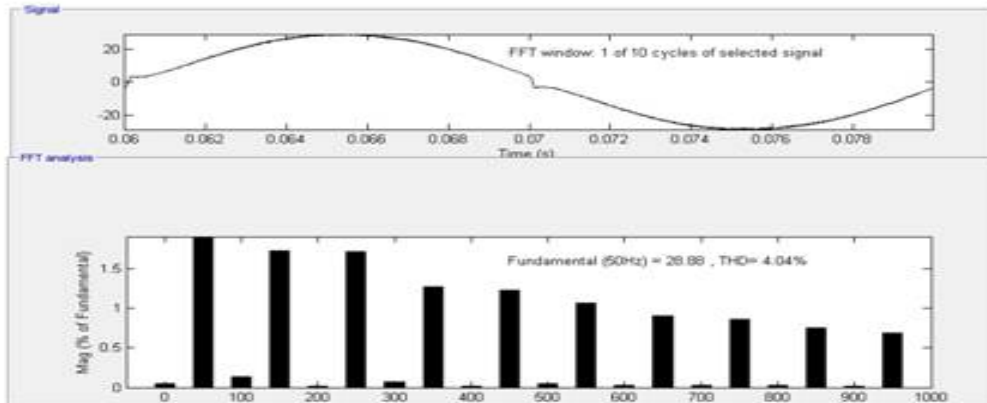


Fig. 9 FFT spectrum of the entire drive system.

The bridgeless SEPIC rectifier is thus used at the front as front end converter and is energized from a single phase voltage of 230 V. The output DC voltage which is designed as 560 V for this case and it feeds the three phase inverter. The three phase voltage available at the inverter is applied to the induction motor whose speed has to be controlled. The mat lab simulations are carried on and the various measurements are taken which are tabulated on Table. 4. From the THD spectrum it can be analyzed that the THD is reduced which is the main attraction of this circuit setup.

Table. 4 Simulation results of the entire drive system.

PARAMETER	-----	PARAMETER	-----
Input voltage	230 V	Power factor	0.95 lag
Input current	12.16 A	T H D	4.04 %
Output voltage	506.9 V	Switch stress	25.83 V
Output current	5.42 A	Phase voltage	502 V

The overall simulation including both SEPIC rectifier and inverter for speed control application shows that the THD of the system is 4.04 % which is a good result comparatively as far as front end converters are concerned. This is shown in the THD spectrum in Fig. 9. The input power factor is 0.93 lagging which is also a good result for a drive application. Due to these improved results from the entire system, the current harmonics are reduced and the power quality issues are limited to some extent.

## V. CONCLUSION

A bridgeless SEPIC rectifier with very little input current ripple has been selected as the front end converter for a motor drive. In order to improve the efficiency, the full-bridge at the input side is eliminated. With the gate driving method, the THD is improved about 4 % and power factor is improved to 0.995 which is nearly unity. The modified topology has an additional advantage that it exhibit lower voltage stress over the switches and the two power switches can be driven by the same control pulse which substantially simplifies the control circuitry. This SEPIC rectifier is made use as the front end converter for speed control of induction motor using volt per hertz method. Due to the low THD, high power factor, the power quality problems in the speed control circuit is reduced to a large extent. The theoretical analysis, simulation results are provided. A small prototype of the SEPIC rectifier has been developed.

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