

Three Stage Push Pull Inverters Based Transimpedance Amplifier

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ABSTRACT: In this paper, a transimpedance amplifier is designed using 0.18 μ m CMOS technology. In the proposed transimpedance amplifier (TIA), feedback resistor R_f of conventional transimpedance amplifier which was implemented using PMOS transistor has been replaced by NMOS transistor as an active feedback resistor. This circuit operates at 1.6 V power supply voltage and for a current of 3 μ A. The proposed transimpedance amplifier posses high gain, low noise, low power dissipation, and high bandwidth. The proposed Transimpedance Amplifier exhibits a power dissipation of 0.871mwatt, transimpedance gain of 54.55 dB, a bandwidth of 371.32MHz, an input-referred noise which is equal to 0.827×10^{-12} A/ $\sqrt{\text{Hz}}$.

KEYWORDS: Transimpedance amplifier, High gain, High Bandwidth, Low noise, Low power dissipation, Push-Pull inverters topology.

I. INTRODUCTION

The most basic definition of a Transimpedance amplifier is, It is a current to voltage converter. It is mainly used to amplify the signal from sensor, such as photodiode. In optical sensing systems, the generated current from photodiodes are generally small and most of the processing's at later stage occurs in the voltage domain, thus it needs to be converted into voltage.

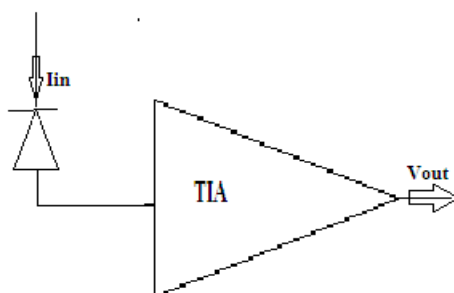


Fig. 1. Basic Function of Transimpedance amplifier

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Hence we can say that there is a wide range of applications where we can use the Transimpedance amplifier, because Optical receivers are used in almost every day to day used things. From a house-hold used Television to High speed Optical communication system, optical receivers are used. Every Optical Receiver will use a photodiode to convert the photons into current. To convert this incoming current to voltage, Transimpedance amplifier is used. Hence Transimpedance amplifier is a widely used device.

II. RELATED WORK

The topology used in Reference [1] is Differential Regulated cascode topology which works on the process technology of 0.18 μ m CMOS technology. It was mainly designed for optical interconnects. But differential regulated cascode topology results in more noise, hence [2] comes up with another topology named as 1 stage push-pull inverter based transimpedance amplifier. It was mainly for an integrated CMOS optical receiver with clock and data recovery circuit. It works on the process technology of 0.35 μ m CMOS technology. Here the noise produced is less as compared to [1]. [3] uses a regulated cascode input stage with shunt feedback topology. Here the supply voltage is 3V. This paper presents the design of an optical receiver analog front-end circuit capable of operating at 2.5 GHz. Fabricated in a low-cost 0.35 μ m digital CMOS process, this integrated circuit integrates both transimpedance amplifier and post limiting amplifier on a single chip. Shunt-shunt feedback topology with cascode gain stage is proposed in [4]. The cascode topology is used to reduce the input capacitance of the amplifier and increase the bandwidth. . The amplifier has been designed to be pseudo differential in order to improve the common mode rejection. The optical front end presented in [5] will have application in Optical Scanning Acoustic Microscope System (O-SAM), which involves a totally non-contact method of acquiring images of the interaction between surface acoustic waves (SAWs) and a solid material to be characterized. In this work, an ultra fast optical front-end using improved regulated cascode scheme is developed based on AMS 0.35 μ m CMOS technology. The receiver consists of an integrated photodiode, a transimpedance amplifier, a mixer, an IF amplifier and an output buffer. Five stage push-pull inverter based topology is proposed in [6]. This paper presents an integrated optical receiver which consists of an integrated photodetector, and a transimpedance circuit. A series inductive peaking is used for enhancing the bandwidth. The proposed structure operates at a data rate of 10 Gb/s with a BER of 10-20 and was implemented in a 0.35 μ m CMOS process. CMOS Regulated cascode with inverter based Cherry Hooper amplifier was designed in [7]. It was a 1.57mwatt CMOS Transimpedance Amplifier for VHF Micromechanical Reference Oscillators. In [8] three stage push-pull inverters based topology is introduced which was optimized for detecting very weak signals generated for microscopy imaging in the scanning electron microscope (SEM).

III. CIRCUIT DESIGN

The three stage push-pull inverters based Transimpedance amplifier is shown in fig.2. It consists of three inverters connected with each other serially. Also after every inverter a NMOS with diode connected load is placed which is used to increase bandwidth and decrease miller effect. In proposed TIA circuit, a feedback resistor was also used which is replaced with NMOS transistor as an active feedback resistor biased by the gate voltage Vbias. Besides better controllability, the implementation of the feedback resistor using a NMOS saves chip area immensely. The value of feedback resistor can be determined by using equation 1, which is as follows-

$$R_f = \frac{L}{W\mu C_{ox}(V_{gs}-V_t)} \quad \text{eq. (1)}$$

where W =width, L = length, V_{gs} = gate to source voltage, V_t = threshold voltage and μC_{ox} = Transconductance parameter.

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There is a voltage source Vdd of 1.6 V which is applied to each PMOS transistor. Amplification of signal occurs from input to output. In TIA output is taken at terminal Vout, and a portion of output is given as feedback to the input of the amplifier.

The Gain of the Transimpedance amplifier is given by the ratio of the output voltage to the input current.

$$A = \frac{V_{out}}{I_{in}} \quad \text{eq. (2)}$$

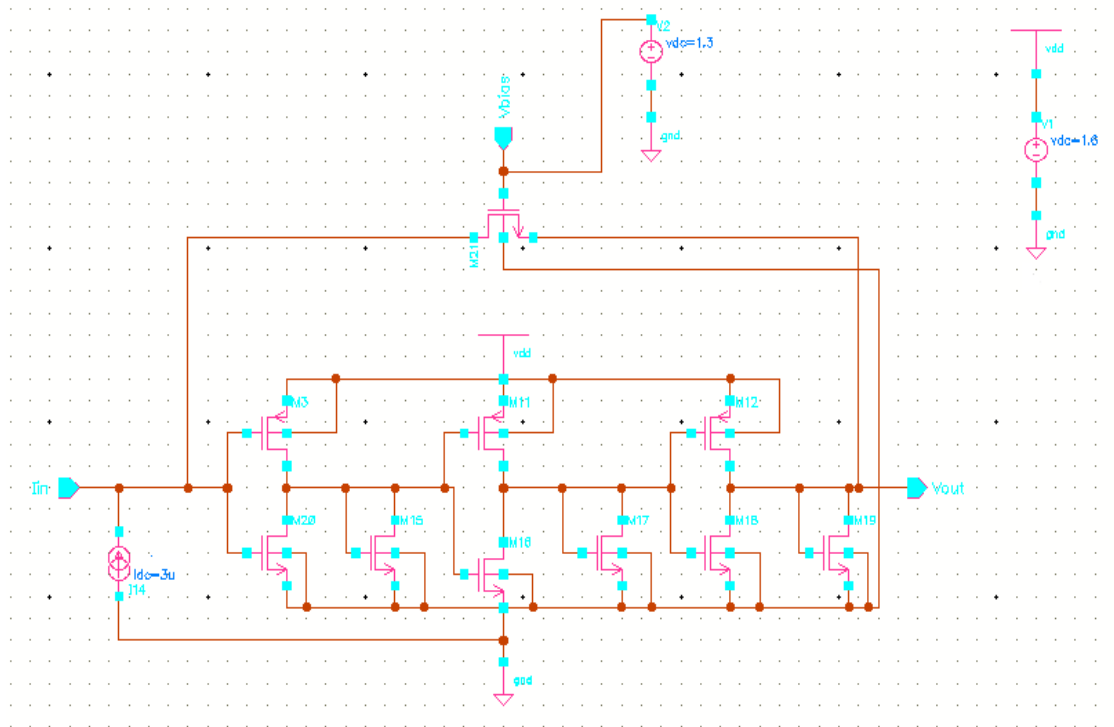


Fig.2. Circuit diagram Of Proposed Transimpedance amplifier.

Three stages transimpedance amplifier consist of three identical cascaded stages having seven NMOS transistor and three PMOS transistor. A photocurrent of 3μA is used in the circuit. A dc voltage of 1.3 V is applied to the feedback transistor as a biasing voltage. The transistors should be in saturation region in order to make them work as amplifier, except the feedback transistor which works in linear region because it is to be used as a resistor.

IV. SIMULATION RESULTS

The simulation is carried out using Spectre simulator of Cadence . The simulator works on 0.18μm CMOS technology.

Gain Calculation of TIA: As explained earlier, the gain of a Transimpedance amplifier is given by the ratio of the output voltage to input current. The gain of single stage TIA is given by,

$$A = \frac{gm_{13} + gm_{20}}{gm_{15}} \quad \text{eq. (3)}$$

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In order to calculate the gain of three stage TIA, the cube of single stage TIA is done. This is because the stages of TIA are connected in series, hence the gains of all the stages are multiplied. Since the aspect ratios of all the stages are same, hence the gain of all the stages will remain same and the overall gain will be cube of single stage TIA. The gain thus calculated is 54.55 dB. Fig 3 shows the gain of proposed TIA.

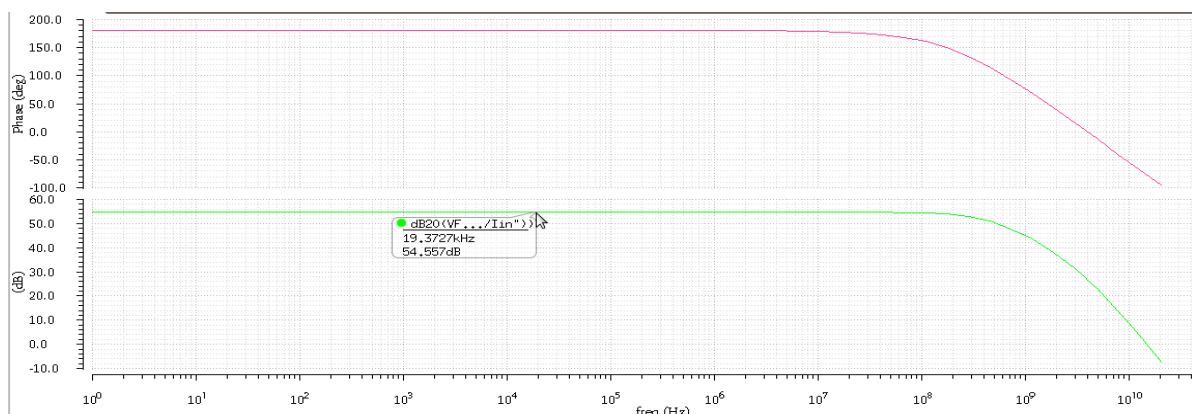


Fig. 3. Gain of Proposed TIA

Bandwidth calculation of TIA: The 3 dB bandwidth of the TIA is calculated at the point where the gain drops by 3dB. The bandwidth enhancement is one of the most important factor in designing a TIA. The bandwidth enhancement is done by proper selecting the value of the diode connected MOS. Mathematically the bandwidth can be calculated by a formula-

$$\text{Bandwidth} = \frac{1+A}{2\pi R_f C} \quad \text{eq.(4)}$$

Where A is the gain, R_f is the feedback resistance and C is the capacitance. The bandwidth thus calculated is obtained as 371.32MHz. Fig 4 shows the bandwidth of proposed TIA.

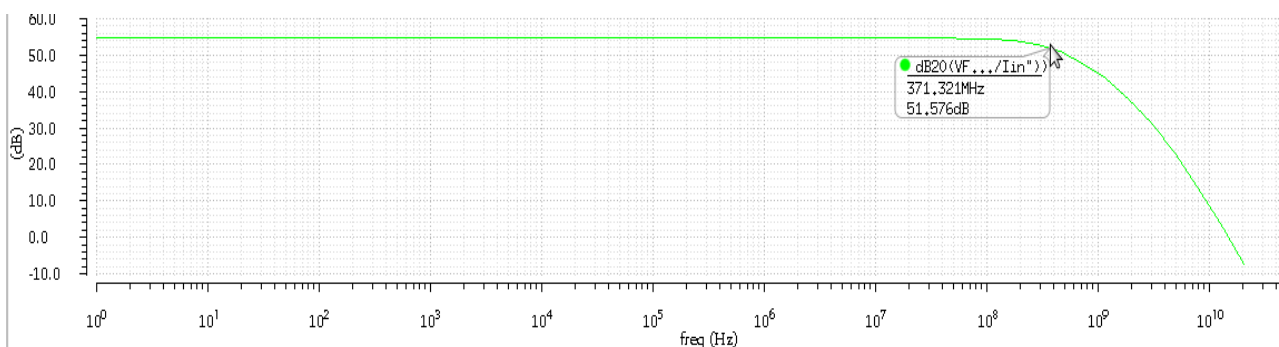


Fig. 4. Bandwidth of Proposed TIA

Noise and Power calculation of TIA: The noise calculated here is the input referred noise. The input referred noise is defined as the noise calculated by keeping all the input sources. Generally noises are calculated by removing the

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sources (By open circuiting the current sources and short circuiting the voltage sources), this noise thus calculated will not show the effect of the input sources on the device, Hence In this noise calculation the current source is placed in the circuit and then the noise is calculated. The noise thus calculated is obtained as $0.827 \times 10^{-12} \text{ A}/\sqrt{\text{Hz}}$. Fig 5 shows the noise of proposed TIA.

The power dissipation of the device should be as low as possible. Here the DC Power dissipated is 0.871mW.

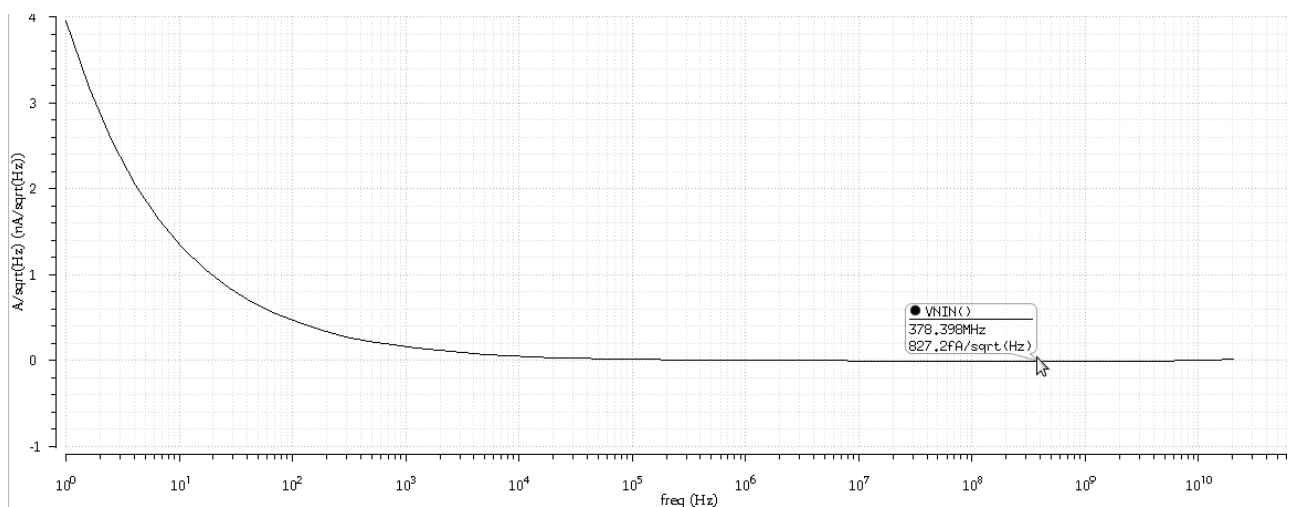


Fig. 5. Noise of Proposed TIA

Layout of Proposed TIA: After the analysis and calculations are done, The layout of the proposed TIA is made by the layout tool “Asshura” of cadence. The connections are done in such a manner so that their should not be any Design rule Check (DRC) error. Fig 6 shows the layout of proposed TIA.

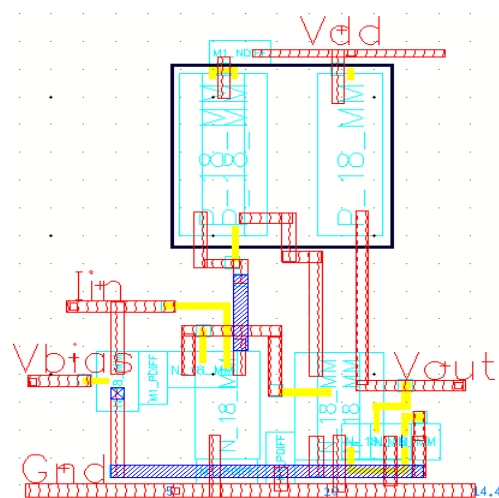


Fig. 6. Layout of Proposed TIA

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Design of TIA	[1]	[2]	[3]	[4]	[5]	[6]	[7]	[8]	This work
Process Technology	0.25 μ m Si CMOS	0.35 μ m Si CMOS	0.35 μ m Si CMOS	0.18 μ m Si CMOS	0.35 μ m Si CMOS	0.35 μ m Si CMOS	0.18 μ m Si CMOS	0.35 μ m Si CMOS	0.18 μ m Si CMOS
Topology	Differential Regulated Cascode	1-stage push pull inverter	Regulated cascade input with shunt feedback	Shunt-shunt feedback with cascode gain stage	Improved regulated cascode	5-stage push pull inverters	Regulated cascode with Cherry-Hooper amplifier	3-stage push pull inverters	3-stage push pull inverters
Supply voltage(volt)	2.5	3.3	3	3.5	3.3	3.3	1.5	3.3	1.6
Bandwidth	670MHz	910.5MHz	2.2GHz	1.8GHz	6GHz	10Gb/s	280MHz	12.5MHz	371.32MHz
Input referred noise(pA/ \sqrt Hz)	20.9	6.03	17.1	9	21	25.8	-	3.54	0.827
Power consumption	27mW	-	-	115mW	-	87.4mW	1.57mW	60mW	0.871mW
Gain(dB)	80	69.7	55	64	51	36.56	99	107.3	54.55

TABLE I
PERFORMANCE COMPARISON OF THIS WORK WITH RECENTLY PUBLISHED TIA'S

V. CONCLUSION

A transimpedance amplifier is designed using 0.18 μ m CMOS technology. In the proposed transimpedance amplifier (TIA), feedback resistor R_f of conventional transimpedance amplifier which was implemented using PMOS transistor has been replaced by NMOS transistor as an active feedback resistor. This circuit operates at 1.6V power supply voltage and for a current of 3 μ A. The proposed transimpedance amplifier posses low noise, low power dissipation, high gain and high bandwidth. The simulation results shows that the proposed Transimpedance Amplifier exhibits a power dissipation of 0.871 mW, transimpedance gain of 54.55 dB, bandwidth of 371.32 MHz, an input referred noise of 0.827×10^{-12} A/ \sqrt Hz. Table I shows the comparison of various topologies of TIA's with this work. The future work in this amplifier can be done in terms of increasing the number of stages and to decrease the sizing of the transistors. Here the minimum length is taken as 180nm. With the advancement of Technology, the length and width of the device will decrease and thus the power dissipation will also decrease.

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