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Vol. 5, Issue 7, July 2016

# Modelling and Analysis of SET Effect in Charge Pump PLL

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**ABSTRACT**: In this paper we analyse the effect of Single event effect (SEE) in charge pump phase locked loop and the responses with different aspects such as voltage and current with respect to time. We demonstrate this impact of Single event transient (SET) effect on the charge pump circuit by modelling in matlab and Simulink tool. This SET effect has an impact on settling time, pulse width and frequency of the synthesized signal. A SET pulse of small amplitude and period is generated and tested for the modelled circuit examining the settling time and impacts of this pulse is studied. This generated pulse is tested before the low pass filter unit, Charge pump and for the Voltage controlled oscillator unit. The obtained responses are figured out and studied which will be further helpful for the radiation hardening of the system respectively. This is modelled using the MATLAB and SIMULINK tool.

**KEYWORDS**: Charge Pump (CP), Phase Locked Loop (PLL), Single Event Transient (SET), Voltage Controlled Oscillators (VCOs), Phase Frequency Detector (PFD).

### I. INTRODUCTION

Electronic gadgets utilized on shuttle must be shielded from the impacts of radiation. This method of shielding the devices from the radiations of the externals is known as radiation hardening. The examination of the impacts of radiation on test PLLs demonstrates the simple escalated outline of a customary charge pump based PLL is not reasonable for radiation hardening applications. Frequency synthesizers are crucial building obstructs in wave frequency, correspondences, and simple sign handling for producing high precision wave signs. A case study of clementine failure, in which an noise caused due to the asteroid hit the device, which was very small in fact had a huge impact in the synthesis of the signal at the receiver part which led to the loss of data eventually failure of the device. Hence this study is helpful in analysis those effects on the system which is can be resourced to design radiation hardened system in further work.

### II. RELATED WORK

A Space Craft launched for a mission on 25<sup>th</sup> January 1994, for the release of satellite on the orbit. Initially the mission was successfully placed on the precise orbit. In further days is main system sent and unintentional signal that caused thrust to fire. Eventually the satellite lost the altitude and began revolving abruptly, impacting in the burst of the satellite. Later the research study identified the problem for the cause, being the radiations in the environment having the high energy ion hitting the satellite which caused the miss match of the output and eventually ending up in the mission failure. This case study shows the importance of the study of the SET effect on the devices which is open to the radiation in the space. The transfer function for the closed loop system is studied for the modelling of the current circuits. The study in this paper helps in analysing the effect of radiation and also mitigating it by the suitable hardening technique which can be incorporated in the devices of the system which are easily affected by radiation. The SET tolerant devices can designed using the techniques like triple modulo reduction, majority decision voter circuit, code word state preserving technique and so on.



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#### III. PROPOSED SYSTEM

The simple circuit of charge pump PLL comprised of the Phase Frequency-detector circuit for phase detection which has a feedback from the divider which is as shown in the figure. The system also comprises of the charge pump which converts voltage to current pulses.

#### A. Overall Structure of CP PLL



Fig. 1 Proposed Charge Pump PLL

The figure above represents the conventional charged pump PLL block diagram, which constitute of the Phase Frequency Detector (PFD), Charge Pump (CP) circuit, Loop Filter, Voltage controlled oscillator (VCOs) and the Frequency Divider Circuit. This circuit is modelled for the analysis of the SET effect on the system. The charge pump circuit senses the changes in voltage converting it to the current pulses. The VCO governs the frequency agility of the circuit.

#### B. Charge Pump model

The Charge pump model comprises of an arrangement of current sources with sizes of IP1 and IP2 amps separately. As a rule the present sources are symmetrical in this manner IP1 = IP2 = IP. These are connected to the source and the ground respectively which acts as the sink as shown in the figure.





The Up and the down signal are fed from the previous circuit PFD. The charge pump consists of the current sources as shown in the above diagram. These current sources converts the voltages to the current or pulse. The



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signal from the PFD which when fed, the upper signal leads to the positive current pulse, charging the capacitor at the loop filter and the down signal leads to the negative current pulse, eventually discharging the capacitor at the loop filter to the ground. These are activated by the switched S1 and S2 shown above. These switches both will never be ON. This enhances pumping the current into the filter, hence the name.



Fig. 3 Phase model of Charge Pump

When  $Q_A$  is high the capacitor charges and discharges when  $Q_B$  is high as shown in the above diagram. The resultant curve is the difference of the signal pulse obtained. There are many types of Charge Pumps available namely,

- Conventional Tri-Stage
- Current Steering
- Differential input with Single-Ended output
- Fully Differential charge pumps

Which are based on the power consumption, speed, clock skew, Power and also based on clock generator. There are many non-idealities in charge pump like leakage current, mismatching of timing and charge sharing, etc. though there are many advantages of the charge pump as it devours less power than active filters, and has less noise comparatively. It is better with the objective of putting the loop filter in the chip.

### C. SET analysis for the voltage response

The below block shows the modelled Charge pump for which the small current pulse i(s) is provided indicated below



Fig. 4PLL model for SET characterization

Here  $I_P$  is the charge pump current,  $K_{VCO}$  is the gain of the VCO,  $R_P$  is the resistance of the loop filter and  $C_1$  is the capacitance of the loop filter and  $C_2$  is very less comparatively which can be neglected. Transfer function of the system is given by



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$$H(s) = \frac{Vc(s)}{i(s)}$$
$$H(s) = \frac{\frac{1}{C1}s(RpC1s + 1)}{s2 + \frac{IpKvco}{2\pi C1}RpC1s + \frac{IpKvco}{2\pi C1}}$$

On substitution we get the primary output of V<sub>C</sub> as illustrated below,

$$Vc(t) = Ip * Rp(e^{-\tau \omega n t} f\tau(t) - e^{-\tau \omega n (t-T)} f\tau(t-T))$$

Where  $f\tau(t)$  varies with the  $\tau$ , as shown in the simulated results, the transient V<sub>C</sub> responses by varying the pulse width (T), and by varying w.r.t the SET pulse amplitude I<sub>P</sub> and by varying the settling time constant  $\tau\omega n$  is mentioned in the simulated result.



Fig. 5 Transient V<sub>C</sub> response as a function of T,  $I_P$  and settling-time constant  $\tau\omega n$ 

#### D. SET Analysis for the Error Response

The below block shows the current pulse  $I_{pulse}$  of small magnitude impacting on the PFD/CP, which also excites the VCO output of the same. The error response is plotted by using the below mentioned transfer function and using the tool matlab and Simulink the response is obtained as follows.



Fig. 6 PLL model for SET Characterization



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The transfer function for the same is given by,

$$\frac{\varphi e}{\text{lin}}(s) = \frac{\text{Kvco F}(s)}{\text{Ns} + \text{Kpfd Kvco F}(s)}$$

In time domain the current equation is given by

$$\mathbf{I}_{in}(t) = \mathbf{I}_{Pulse}^* (\mathbf{u}(t) - \mathbf{u}(t-T))$$

Laplace transformation of the same is

$$I_{in}(s) = \frac{Ipulse}{s} (1 - e^{-st})$$

For the error function the reverse Laplace transformation is applied to get the following error response equation as follows,

$$\varphi e(t) = \frac{Ipulse}{Kpfd} \left( 1 - e^{-\zeta \omega nt} \left( \cos\left(\omega n\sqrt{1-\zeta^2}\right)t - \frac{\zeta}{\sqrt{1-\zeta^2}} \sin\left(\omega n\sqrt{1-\zeta^2}\right)t \right) \right) * \left\{ u(t) - u(t-T) \right\}$$



The figure shows the responses modelled as a function of bandwidth and pulse width. In the above figure the band width is varied retaining the time period as 1ns, similarly error response for different pulse width is obtained retaining the bandwidth as 1 MHz as shown in the following figure.



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Fig. 8 Error response for different pulse width

#### E. SET analysis for the Output Voltage

The below model is designed and the SET pulse i(s) is provide before the VCO block diagram as shown and characterised.



Fig. 9 PLL model for output characterization

The SET signal is of very small magnitude and of the time period 1ms. The impact of the same is measured and plotted accordingly. The transfer function of the output voltage Vc(s) varies w.r.t the pulse i(s), and is calculated as

G(s) = Kvco/s

The above equation G(s) shows the open loop transfer function, the overall equation for H(s) is given by

$$H(s) = \frac{V(s)}{I(s)} = \frac{\left(\frac{Kvco}{s}\right)^*}{1 + \left(\frac{Kvco}{s}\right)^* \left(\frac{Ip}{2\pi}\right)^* (Rp + 1/Cs)}$$



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On simplification the Output is found to be,

$$V(s) = \frac{\left(\frac{Kvco}{s}\right)*I(s)}{1 + \left(\frac{Kvco}{s}\right)*\left(\frac{Ip}{2\pi}\right)*(Rp+1/Cs)}$$

Where,

$$I(s) = Iset(1/s - e^{-Ts}/s)$$

The model designed and conclusions are affirmed by simulations done utilizing the tool Simulink and matlab codes are also being synthesized. The simulation result of the PLL is a shown in the following figure.



### IV. CONCLUSION

From the above experiment and analysis we understand the effect of SET behaviour on the different stages of the component on the system. If this small pulse has a huge impact on the overall output, hence from the study, in order to mitigate this effect, optimization of the parameters such as  $R_P$ ,  $\zeta$ ,  $\omega n$ , T, is necessary. And this study is beneficial in further building the radiation hardened circuits by the analysis and effectively choosing the component parameters.

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