

DO-254 Implementation of CAN for Mil-Aero/ Safety Critical Applications

Reshma N¹, Dr. Srividya P², Kumaraswamy K V³

P.G. Student (VLSI Design and Embedded Systems), Dept. of E.C.E, SJBIT, Bengaluru, Karnataka, India¹

Associate Professor, Dept. of E.C.E, SJBIT, Bengaluru, Karnataka, India²

Technical Manager, Trident Tech Labs Private Limited, Bengaluru, Karnataka, India³

ABSTRACT: Aim is to design CAN and to make it DO-254 compatible to ensure compliance in designing safety critical/avionic hardware. DO-254 standards provide most stringent policies and compliance rules to ensure that the hardware designed is fool proof one and wouldn't fail under unexpected scenarios. In order to accomplish DO-254 flow that includes planning, requirement capture, conceptual design and detailed design, Mentor graphic toolset i.e ReqTracer, HDL Designer, Precision RTL Plus and Questasim are used for different phases of the FPGA flow including design entry, simulation, safe synthesis and implementation of the design.

KEYWORDS: Baud rate prescaler, bit stream processor, arbitration, time quanta, delta delay.

I. INTRODUCTION

CAN was developed by Bosch as a message broadcast system with maximum signalling rate of up to 1Mbps. Unlike USB or Ethernet that transmits large blocks of data point-to-point from one node to the other under the supervision of a central bus master. CAN broadcasts short messages to the entire network. The CAN communications protocol, ISO-11898: 2003, describes how information is passed between devices on a network and conforms to the Open Systems Interconnection model that is defined in terms of layers. Initially it had 11 bit identifiers and now after the release of CAN2.0B (after CAN2.0A) in 2012 it has 29 bit identifiers to communicate between nodes which are connected in the system. CAN protocol needs CAN transceivers to exchange the data from one node to other node.

The CAN communication protocol is a carrier-sense, multiple-access protocol with collision detection and arbitration on message priority (CSMA/CD+AMP). CSMA means that every node on the bus has to wait for a prescribed period of inactivity before an attempt is made to send a message. When the bus is free any node may start to transmit a message. The node with the message of highest priority to be transmitted gains the bus access. If two or more nodes start transmitting messages at the same time, the bus access conflict is resolved by bit-wise arbitration using the Identifier. The mechanism of arbitration guarantees that neither information nor time is lost. If a Data frame and a Remote frame with the same Identifier are initiated at the same time, the Data frame prevails over the Remote frame Bus access is won by the higher priority identifier.

The basic structure of CAN is shown in Figure 1. The tasks carried out in bit stream processor are acceptance filtering and acceptance masking. The four non overlapping time segments of the nominal bit time are synchronization segment, propagation time segment, phase buffer segment 1 and phase buffer segment 2 each of which consists of time quanta which are of programmable numbers. Baud Rate Prescaler (BRP): $tq = BRP / fsys$. Where tq is length of time quanta and fsys is the system clock.

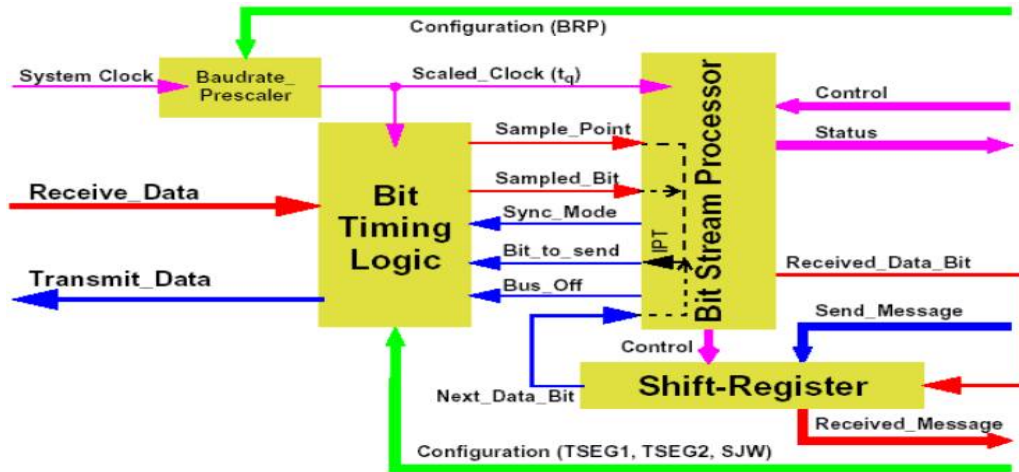


Figure 1: structure of CAN protocol controller

DO-254 provides guidance on the processes and methodologies which should be applied in the development and verification of electronic hardware to achieve an acceptable level of confidence such that the end hardware functions correctly and will be in compliance with airworthiness requirements. DO-254 is an avionics industry document entitled “Design Assurance Guidance for Airborne Electronic Hardware” that focuses to ensure product performs its intended function (via design assurance process). It was invoked as law by the FAA/EASA in 2005 and it is now a worldwide standard for aviation design and also spreading into military applications. It is also influencing other safety-critical industries.

If the failure of a system could lead to consequences that are determined to be unacceptable, then the system is safety-critical and CAN is one such system. Paper is organized as follows. Section II describes various systems on Controller Area Network systems being proposed. The flow diagram in section III represents the DO-254 flow. Section IV presents experimental results showing simulation waveforms, RTL schematic and area report. Finally, Section V presents the conclusion.

II. RELATED WORK

A methodology was proposed using Controller Area Network (CAN), protocol, standards and their architecture. Where in, overview of the CAN applications both in the non-industrial and the industrial field, it was also used in home automation [1]. Later a system that discusses about Control Area Network for vehicle law enforcement application based on the requirements of an advanced law enforcement vehicle demonstrator and Control Area network architecture has been implemented [3].

In an effort to reduce the amount of point to point wiring in law enforcement vehicles and to centralize the communication between devices, CAN is suggested as a means to serialize data communication within the vehicle environment. A comparative case study of distributed network architectures [4] for different automotive applications was made and a table which distinguishes the various protocols such as Control Area Network (CAN), Local Interconnect Network (LIN), and Media Oriented System Transport (MOST) was published. Then, CAN protocol using PIC for vehicle monitoring system was implemented [4]. Controller Area Network (CAN) is mainly used in the automotive and automation industries due to its ease in use, low cost and the reduction in wiring complexity.

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DO-254 flow

The DO-254 FLOW shown in Figure 2 is explained as follows:

- The planning phase is crucial in the DO-254 project lifecycle as it defines how all the aspects of project achieve DO-254 compliance.
- Design requirements are tracked by ReqTracer along with the test results throughout the entire product development cycle, ultimately providing real-time measurement of progress.
- Code is created in the HDL Designer such that the pre-defined DO-254 coding rules are met. This helps in the quality assessment of the code and also the code is tagged to the requirements. Coding is done such that the design assurance mandates are met and the pre-defined rule-set makes it is easy to fix the violations.

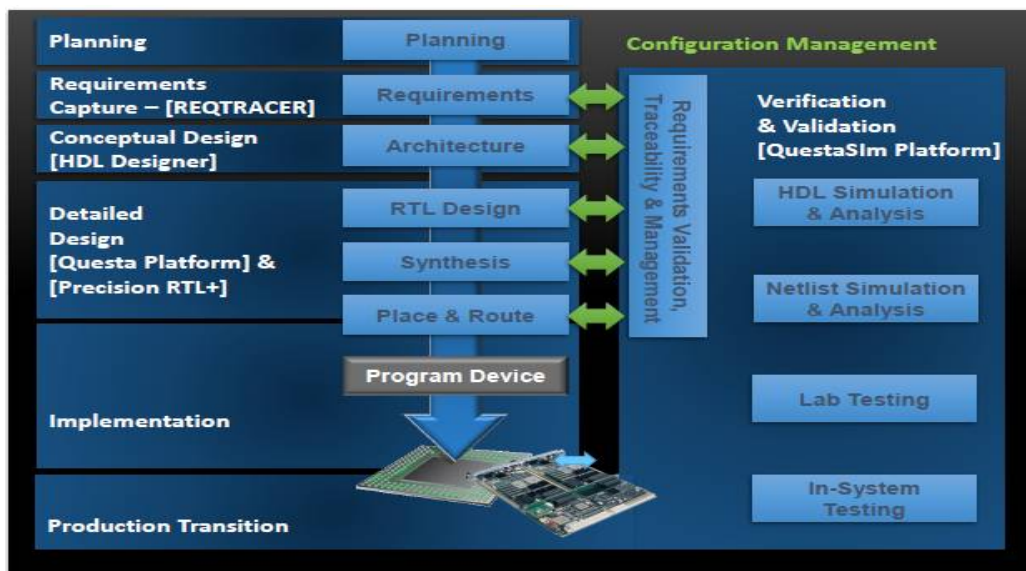


Figure 2: DO-254 Flow

- Using Questasim the code is then compiled and simulated with code coverage which helps in coverage-driven verification and verification management. Simulation wave windows can be expanded to show delta delays. Dataflow window allows to explore physical connectivity of the design and to find out the cause of failure if there is any.
- For the physical synthesis Precision RTL is the Flagship FPGA Synthesis solution from Mentor Graphics which is Vendor-Independent Solution for breakthrough productivity and best suited for Commercial, Mil-Aero & Safety Critical Applications
- Synthesis and place and route processes help to bridge the transition from design to implementation. If the RTL code is synthesizable, it can be easily dumped to the FPGA.

III. EXPERIMENTAL RESULTS

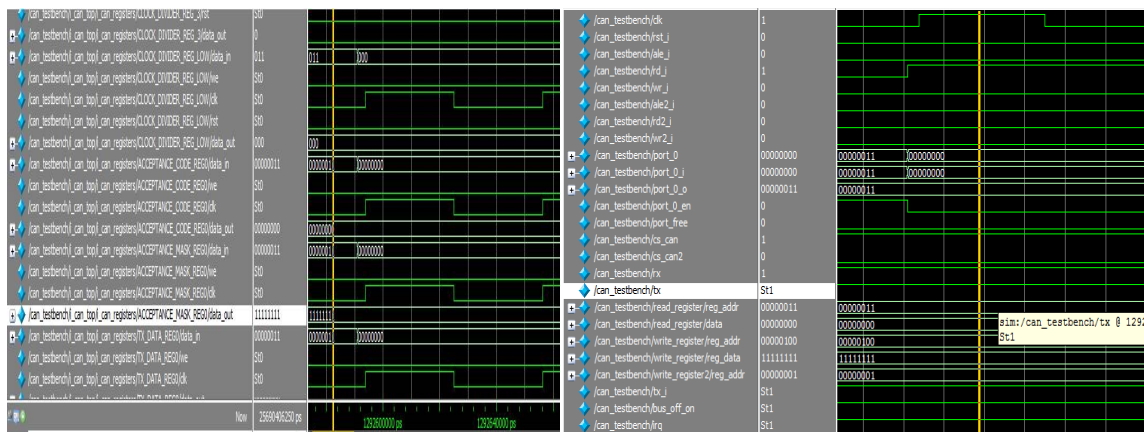
The verilog compiler of Questasim compiles the CAN source code into retargetable, executable code. It is then simulated. Figure 3 (a) shows the simulation waveforms for acceptance filtering and acceptance masking carried out in bit stream processor. There are 2 sets of registers that handle selective receive of CAN message. The CAN acceptance

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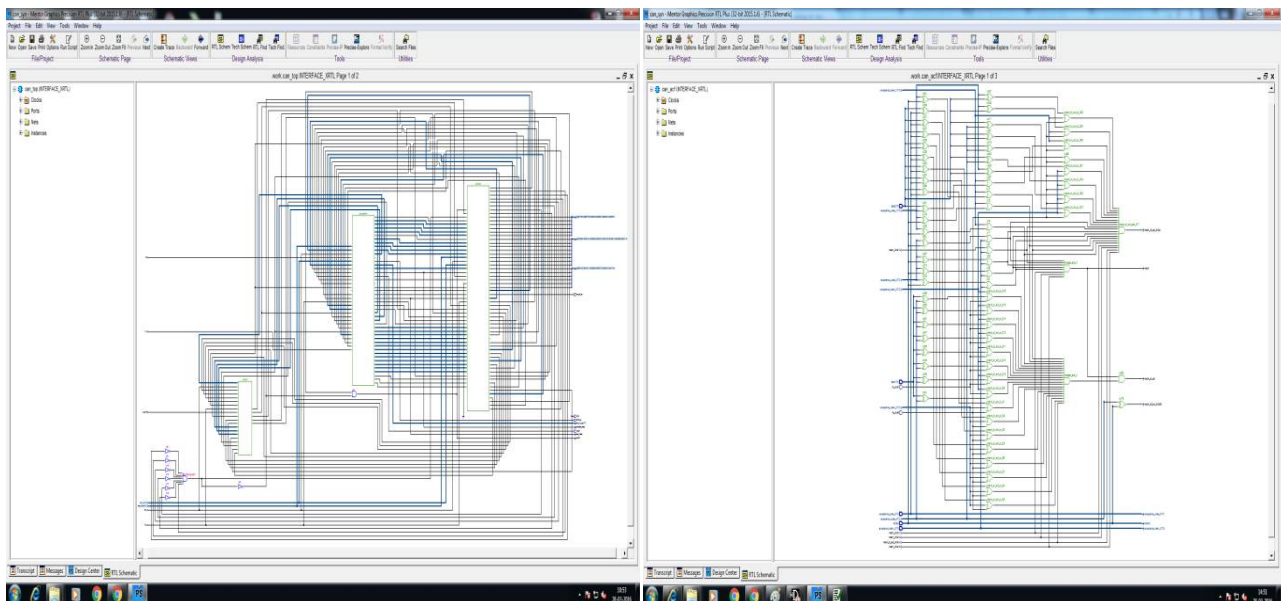
mask set of registers are used to indicate which of the bits in received CAN frame id will be used by CAN filter set of registers. CAN filter set of registers compare received CAN id bits with corresponding bits in CAN filter register set. If match is seen between filter and CAN id, CAN frame is accepted by CAN engine and transferred to CAN receive buffer else dropped. Fig 3 (b) show the simulation results of the port outputs respectively.



3(a)

3 (b)

High-level RTL schematics help to determine the impact of coding styles while detailed technology schematics show where and how device specific resources such as RAM and ROM are utilized. Figures 4 (a) and (b) represent the high-level RTL schematics for CAN and acceptance filtering in particular respectively obtained using Precision RTL Plus.



4(a)

4 (b)

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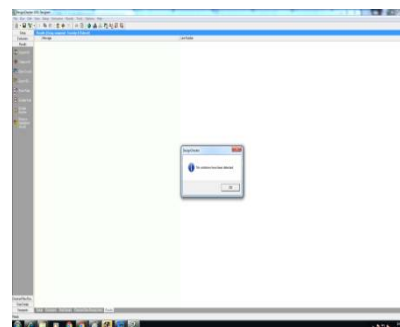
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```
// Running on Windows 7 intern4@INTERN4-PC Service Pack 1 6.01.7601 x86
//
// Start time Mon Mar 28 10:38:48 2016
```

```
*****
Device Utilization for 6SLX75FGG676
*****
```

Resource	Used	Avail	Utilization
I/Os	19	408	4.66%
Global Buffers	1	16	6.25%
LUTs	1094	46648	2.35%
CLB Slices	274	11662	2.35%
Dffs or Latches	624	93296	0.67%
Block RAMs	0	172	0.00%
Distributed RAMs			



5(a)

5 (b)

Area report is the detailed description of device utilization and Figure 5(a) shows the area utilization of CAN before optimization. Figure 5(b) represents the design checker display indicating that no DO-254 violations are detected which implies that the code is DO-254 compatible.

IV. CONCLUSION

The design requirements are traced using ReqTracer. For the conceptual design, Code is created in the HDL Designer such that the pre-defined DO-254 coding rules are met. The design is then Compiled and Simulated using Questasim with the code coverage. Synthesis is successfully done using Precision RTL Plus. The design for CAN is DO-254 compatible and can be used for mil-aero and safety critical applications.

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BIOGRAPHY

Reshma N is an M.tech student in the specialization of VLSI Design and Embedded Systems, Dept of E.C.E, SJBIT, Karnataka, India.

Dr. Srividya P, specialised in VLSI Design and Embedded Systems, is an Associate Professor, Department of Electronics and communication Engineering, SJBIT, Karnataka, India.

Kumaraswamy K V received B.E, Degree from Mysore University, M.Tech in VLSI Design and Embedded Systems, Degree from Visvesvaraya Technological University, currently pursuing Ph.D in Semiconductor devices, worked in Conexant Systems, Infineon Technologies and so on, 22 years of experience in Semiconductor Industries.