

Design and Implementation of Index Based Round Robin Arbiter for NOC Routers Using FPGA

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ABSTRACT: The paper offerings the project and investigation of an arbiter for well-organized multisystem collaboration with sharedresources. The arbitration algorithm contains Index format of round robin arbiter to gain fast system performance and lower areaexecution and cost. The enquiry for data requests of clients under different priorities has been simulated. The resultsindicate, a better performance can be accomplished with this arbitration structure. Based on the performance study, importance arbitration scheme can be custom tuned to meet the design necessities. The implementation of the arbiter withimportance arbitration scheme for SoC applications has also been explained. The arbiter was implemented on FPGA andsynthesized by XILINX 14.2 version. The priority arbiter can be custom tuned to obtain high bandwidth utilization, low latencypower operative for on-chip bus communication.

KEYWORDS:Arbiter micro-architecture; critical path delay; network on chip; router arbiter design

I. INTRODUCTION

Following the quick technological progress, the difficultybefits one of themost pressuring aspects in the design of embedded systems. Price and controlconcernsarisealongside to add to the problems in awareness of network-on-chip [1], NoC, applications,where many IPs (Intellectual Property) such as processor cores, memories, DSPprocessors and peripheral devices are placed together, on a single die. These segmentscommunicate, most often, by means of a shared resource, the on-chip network. The growingdifficulty of the single devices, the growing demand for higher bandwidthon the network lines and an effective frequency defeat new bounds with nearlyevery new design, place the communicué and/or calculationassets arbitration beingthe presentation bottleneck of the NoC system.Arbiters are a fundamental component in systems containing shared resources, and a Centralized arbiter is a firmlyassimilated design for its input requests. In this study, wepropose a new centralized arbiter, which may be used in arbitration of a crossbar switch inNoC routers [2], computer networks [9], or any shared resources. Fig. 1 shows the Structure of an $n \times n$ switch and a crossbar switch fabric implemented with many transmissiongates as switches between input ports and output ports. Each input port contains n virtual output queues (VOQs) to avoid head-of-line blocking. The task of the arbiter isto decide a set of contention-free connection between input and output ports by turningON/OFF those transmission gates.

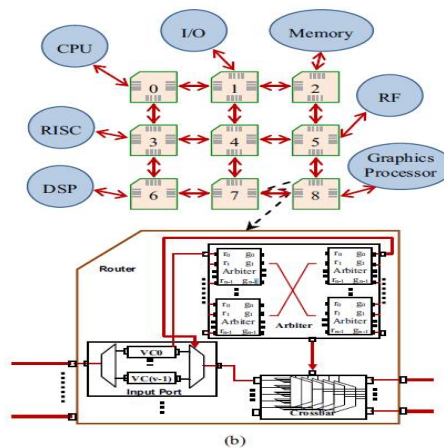


Fig 1. (a) 2D SoC mesh. (b) NoC router.

II. RELATED WORK

The following literature survey includes some of the IEEE papers related to Arbiters algorithm used in FPGA and various techniques used to implement them on FPGA.

1. The crossbar button of a router is the core of the router data path. It changes the data from the input port to the output port doing the kernel of the router operation. The innerconstruction of a crossbar contains of ancollection of multiplexers. In this planning it consists of five 5:1 multiplexers. The five multiplexers have five forty bit data as input. All the five inputs are linked to all the five multiplexers. The data to be progressed to the output depends on the select lines. The select lines are produced by the arbiter dependent on the request signals. There are five select lines of three bit width to select one of the five ports. So the output of each multiplexer depends on the select line of that multiplexer.
2. The secondconstruction uses the CDMA method that has been broadly used in wireless communication systems because it has excessive bandwidth efficacy and multiple access capability. CDMA is a spread spectrum technique that encrypts the information prior to transmission, and thenconveys the encoded data to the transmission standard so that concurrently the middle can be used for distinctinfo streams. The straightforwardhint of this system is that by using suitable interconnections and CDMA encoding the intersect wiring can be made very less. CDMA methodtrusts on the standard of code word, orthogonally, such that when multiple code words are summed they do not delaytotally with each other at any idea in time and can be disconnected without loss of material.
3. SoCchange from wide area systems in their local closeness and because they display less no determinism. Local, high performance networks—such as those established for extensive multiprocessors— have alikenesses and restraints. Some characteristicfeatures, such as vitalityrestraints and design-time concentration, are exclusive to SoCnetworks, however. Whereas calculation and storage driveimportantlyadvantage from device scaling, which deliverslessergates and memory cells, the energy for global communiqué does not scale down. On the opposing,as the “Wiring Delays” sidebar specifies, plansfounded on current delay optimization methods for global wiredisplay that global on-chip communication will needprogressivelydeveloped energy consumption. Hence, reducing the energy used for infrastructures will be a growing concern in upcomingmachineries. Further, network trafficrogulator and intensive care can help better achievethe power that networked computational resources consume. For example, the clock speed and voltage of end nodes can vary rendering to obtainable network bandwidth.
4. The SoC network design problem, design-time speciality, advancesseveral new tasks. Macroscopic links emphasize common- purpose communication and modularity. Communiquésystem design has customarily been decoupled from specific end applications and is toughlyinclined by normalization and compatibility limitations in legacy network substructures. In SoC networks, these restrictions are less restraining because originators design the statement network

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fabric on silicon from scratch. Thus, only the abstract network interface for the end nodes necessitate tuning. Designers can tailor the network architecture itself to the application, or class of applications, the SoC plan targets. We thus visualize a vertical design pour in which every layer of the micro network stack is dedicated and elevated for the target presentation dominion. Such an application-specific on-chip network- synthesis paradigm signifies an open and stimulating research field. Specialization does not imply complete loss of flexibility, however. From a design standpoint, network configurability will be crucial in as long as plug-and-play element use because the components will interact with one another through reconfigurable protocols.

III. CONCEPT OF ARBITER

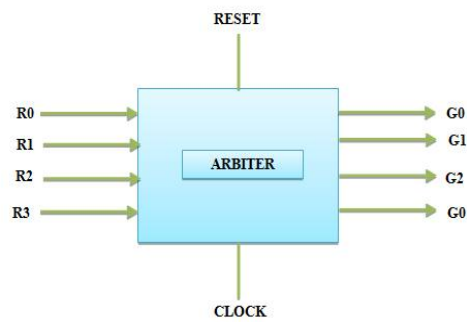


Fig 2.Simple Arbitrer structure

The fig.2 shows simple arbitrer structure. The core arrangement of the arbitrer has a D flip flop, ring counter, five priority logic blocks and five input OR gates. In logic projects flip flops are used to create simple finite state machines. The ring counter is a counter where simple shift registers are linked in cascade to each other. The output of the last flip flop is linked as the input to the main flip flop. The figure design will socialize as long as the clock pulses are functional. In the arbitrer it is the ring counter that chooses the arriving requests in round robin way and gives it to the importance logic block. The functionality of the priority logic block is like to a priority encoder without output encoding. Since each block has different order of inputs the priority of chosen signals varies with the chosen block. With a round-robin arbitrer, the last request to be serviced will have the lowest priority in the next round of arbitration. The fig. 3 shows the Round Robin Arbitrer Structure.

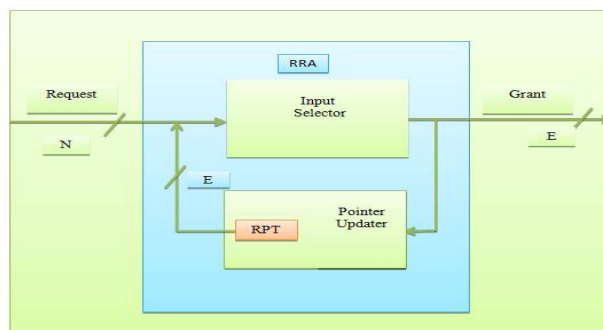


Fig 3.Round Robin Arbitrer structure

IV. PROPOSED ALGORITHMS

In this paper, we present a new arbitrer design called Index-based Round Robin (IRR) arbitrer that employs a least recently served priority scheme and achieve strong fairness arbitration. The proposed arbitrer has smaller arbitration delay, lower chip area and it also consumes less power as compared to the aforementioned arbitrers. Before describing

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the IRR arbiter architecture, we introduce an inseparable and critical output in the arbiter design. The fig.4 shows IRR arbiter design.

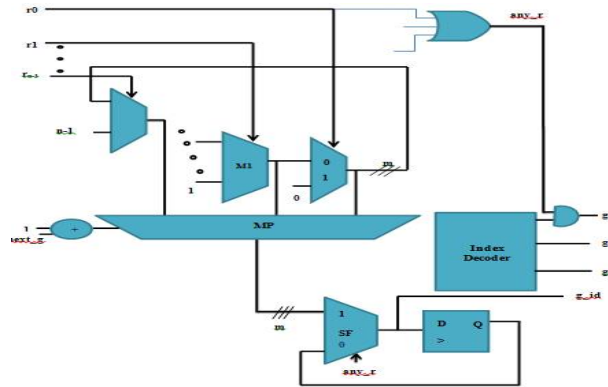


Fig.4 n-input IRR arbiter, where $m=\log_2(n)$.

The fig. 5 shows flow chart of IRR. It explains the overall process of IRR. It reads the request line and grant the signal only when the input request is having highest priority and highest priority request is not equal to last recently served request.

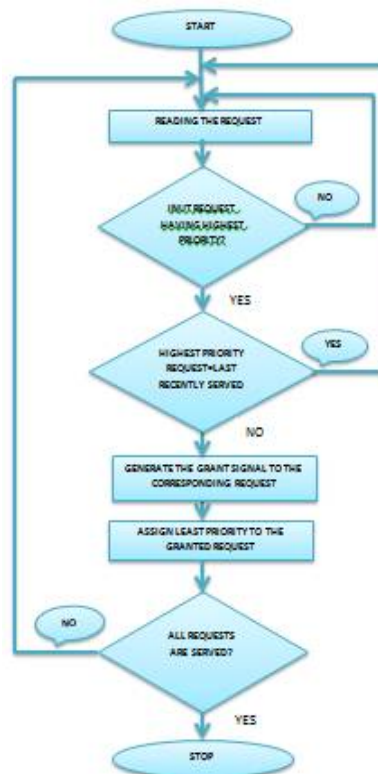


Fig.5 Flow Chart of IRR.

V. RESULTS

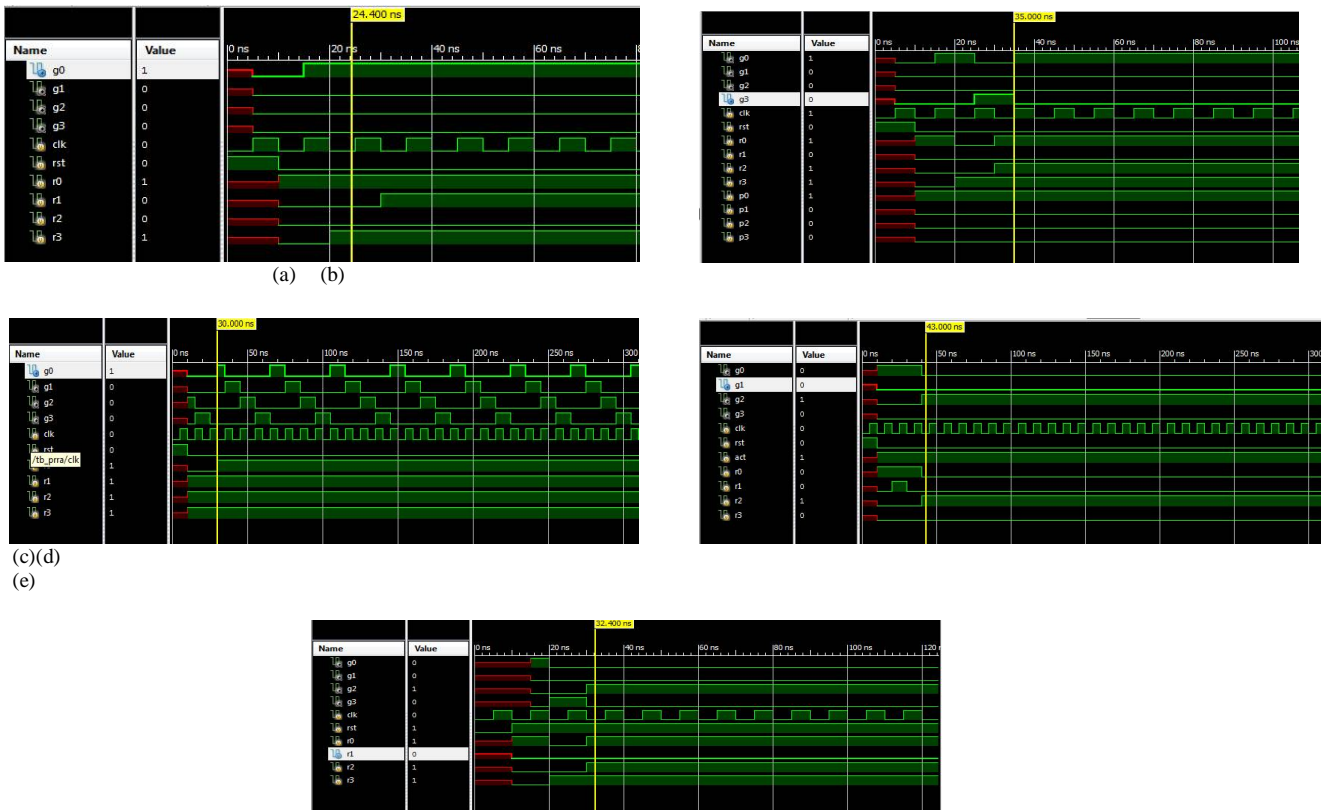


Fig. 8 Simulation results of (a) Fixed priority arbiter (b) Variable priority arbiter (c) Parallel Round Robin arbiter (d) HDRA arbiter (e) Index based Round Robin Arbiter

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	6	54576	0%
Number of Slice LUTs	37	27288	0%
Number of fully used LUT-FF pairs	6	37	16%
Number of bonded IOBs	10	218	4%
Number of BUFG/BUFGCTRL/BUFGCE	1	16	6%

(a)

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	4	54576	0%
Number of Slice LUTs	11	27288	0%
Number of fully used LUT-FF pairs	4	11	36%
Number of bonded IOBs	10	218	4%
Number of BUFG/BUFGCTRL/BUFGCE	1	16	6%

(b)

Fig.9 Device Consumption of (a)Existing System (b) Proposed System.

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VI. CONCLUSION

Synthesis and performance analysis of IRR algorithms is carried out in the project. The results showed different methods and ways of using available resources in FPGA device. Totally the trade-off between throughput, area and delay will determine correct approach of implementing Scheduling algorithm on on-chip router.

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