

A Design of PLL with a Process-Immune Locking-in Monitor and Reduce Jitter

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ABSTRACT: A PLL circuit includes phase detector for detecting phase error between an input and output signal of the PLL circuit and outputting pump up and pump down signal. A charge pump generates a charge pump signal in response to pump up and pump down signals. A loop filter filters charge pump signal to generate a filtered signal. A boost-up device coupled to loop filter output terminal charges a loop filter input terminal, to expedite the filtered signal reaching predetermined voltage level. A VCO coupled loop filter output terminal and the phase detector generates output signal. A common mode voltage reaching lock-in time is reduced by boost-up device charging loop filter to expedite filtered signal reaching common mode voltage, when filtered signal is lower than predetermined detecting voltage.

KEYWORDS: PLL, VCO, TDC, Phase Detector

I. INTRODUCTION

Phase locked loops are found a myriad of electronic applications such as communication receivers and clock synchronization circuits for computer systems. Fig. 1 is schematic block diagram illustrating a conventional differential PLL circuit. The PLL circuit includes phase detector, a charge pump, a loop filter, and a voltage controlled oscillator (VCO).

The phase detector monitors the phase difference between an input signal IN to the PLL circuit and an output signal OUT from PLL circuit, output signal OUT being fed back from the voltage controlled oscillator (VCO). The phase detector also generates up control signals up and down control signals dn and dn for input to charge pump circuit. The charge pump can be implemented as a current pump or a voltage pump. The charge pump charges and discharges loop filter with a pair of charge pump signals VOP and VON.

The charge pump signals VOP and VON are subsequently filtered by loop filter, which is typically constructed as a low pass filter. The loop filter also assists in removing or reducing high frequency components and clock jitter. Signals VOP' and VON' are output from loop filter to the VCO. The variable oscillator 40 can be implemented as voltage controlled oscillator (VCO) or current controlled oscillator. The VCO oscillates in response to the filtered signals VOP' and VON'. The output oscillation of VCO is output signal OUT. When the PLL circuit is phase locked, output signal OUT will be locked at desired output frequency.

In general, practical limits of output frequency range are defined by dynamic loop characteristics underlying the PLL circuit. The loop characteristics include loop variables are loop bandwidth, natural frequency, damping factor, among others. Values of the loop characteristics are typically based on parameters of component parts for the PLL circuit. The present parameters typical frequency synthesis outside a predefined range PLL.

It is common for the PLL to lose phase lock when input signal IN fades or jumps to radically different frequency of operation. The out-of lock state can be detected with lock detection circuit (not shown) and system processing suspended until PLL circuit can re-achieve phase lock. The transition time is unlocked state to locked state is referred to as the lock-in time or pull-in time. The lock-in time consists of common mode voltage reaching time of

International Journal of Innovative Research in Science, Engineering and Technology

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Vol. 5, Issue 5, May 2016

the filtered signals VOP' and VON', and tracking time of phase detector. The common mode voltage reaching time occupies the major part of the lock-in time.

Thus reduce common mode voltage reaching time, the current from charge pump is increased, or a time constant (i.e., $\tau=RC$) of the loop filter 30 is decreased. The time constant τ may be reduced by adjusting resistor R or capacitor C of loop filter, so that they charge more quickly. However, the loop bandwidth increases in proportion to reduction of time constant. In that case, the high frequency components are not filtered sufficiently by loop filter in proportion to increase in loop bandwidth. Furthermore, the loop characteristics of PLL circuit vary with respect to designed loop characteristics. Therefore, the PLL circuit cannot operate stably.

II. PHASE LOCKED LOOP

A phase detector for detecting a phase error between input signal and the output signal and outputting a pump up signal and pump down signal based on phase error; a charge pump coupled to said phase detector for generating a charge pump signal in response to pump up and pump down signals; a loop filter coupled to said charge pump for filtering out high-frequency components charge pump signal to generate a filtered signal, said loop filter having input terminal and output terminal; boost-up means coupled to output terminal of said loop filter for charging input terminal of said loop filter in response to filtered signal, to expedite filtered signal reaching predetermined voltage level; and voltage-controlled oscillator coupled to the output terminal are loop filter and phase detector, for generating the output signal in response to the filtered signal.

The phase locked loop circuit according to claim 1, wherein said boost-up means comprises: bias means for biasing predetermined detecting voltage; input means for receiving the filtered signal; detecting means for detecting filtered signal is less than detecting voltage; and charging means for charging the input terminal of said loop filter in response to detection result from said detecting means. The phase locked loop circuit according to claim 1, wherein said charging input terminal of said loop filter when the detection result indicates that filtered signal is less than the detecting voltage. A differential phase locked loop circuit for generating an output signal in response to input signal, comprising: a phase detector for detecting a phase error between input signal and output signal, and outputting a pair of pump up signals and a pair of pump down signals based on phase error; charge pump coupled to said phase detector for generating a pair of charge pump signals in response to pump up and pump down signals; a loop filter coupled to said charge pump for filtering out high frequency components from the charge pump signals to generate a first and a second filtered signal, said loop filter having two input and two output; boost-up means coupled to the output terminals of said loop filter for charging input terminals of loop filter in response to first and the second filtered signals, to expedite first and second filtered signals reaching a predetermined common mode voltage level; voltage-controlled oscillator coupled to output terminals of said loop filter and said phase detector for generating the output signal in response to the first and the second filtered signals.

The differential phase locked loop circuit according to claim 4, wherein said boost-up means comprises: bias means for biasing a predetermined detecting voltage; detecting means for detecting whether the first filtered signal is less than detecting voltage; first charging means for charging said loop filter in response to a detection result detecting voltage; second input means for receiving second filtered signal; second detecting means detecting whether second filtered charge signal is less than the detecting voltage; and second loop filter in response to detection result from said second detecting.

The phase locked loop circuit according to claim 5, wherein said first bias means comprises: a PMOS transistor having a source, a drain, and a gate, the source being coupled to a power supply voltage source, and drain being coupled to gate; and a current sinker coupled between the drain of PMOS transistor and a ground voltage source. The phase locked loop circuit according to claim 6, wherein said first input means comprises:

The phase locked loop circuit wherein said second PMOS transistor forms a first current mirror with PMOS transistor of said first bias means. The phase locked loop circuit according to wherein said second NMOS transistor forms second current mirror with first NMOS transistor of first input means. The phase locked loop circuit charging comprises a fourth PMOS transistor having current path formed between power supply voltage source and a third line, and a gate coupled to a second node.

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 5, May 2016

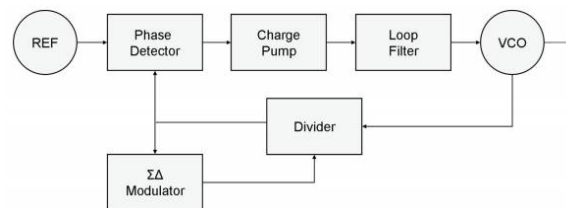


Fig. 1 Phase Locked Loop

III. DETAILS OF THE DIGITAL-CONTROL CIRCUITS

The detailed circuit of TDC, which is composed of a charge pump, CPTD, a comparator CH, which has a hysteresis characteristics (as shown in the right bottom of Fig. 3) with two threshold voltages, V_{thH} and V_{thL} , a D-flip flop (DFF), and a six-bit counter. The current sources of CPTD are controlled by the feedback signal, FQ, which is the output Q of DFF. During the locking-in process, $FQ = 1$ and CPJ gets charged for the positive half cycle of the reference clock CLK as shown in Fig. 4(a). In the figure, V_{cap} is the voltage of the CPJ. The current source I_c is designed to be large enough to charge V_{cap} to exceed V_{thH} , the upper threshold of the comparator CH, within this half cycle. V_{out} , the output of CH, will be switched to HIGH. This will toggle DFF to change its state, i.e., FQ becomes LOW. Then CPJ will enter into the discharging process. During this period, whenever PD goes to HIGH, CPJ gets discharged. PD is a series of pulse trains whose width is dependent of the difference of DIV and CLK in Fig. 1. The larger the difference, the wider of the pulse, and the more of CPJ gets discharged. In other words, the number of PD pulses to discharge V_{cap} to V_{thL} is inverse proportional to the width of the pulses. The V_{cap} waveform of Fig. 4(a) shows such a discharging process, where it takes three PD pulses to discharge the CPJ to reach V_{thL} . The six-bit counter is used to count the number of these discharging pulses.

Bandwidth Control Unit

The detailed circuit of BCU is shown in Fig. 5. It is composed of three flip-flops: DFF1, DFF2, and DFF3. The third bit of the six-bit counter and the FQ from TDC are its input. The third bit is chosen because in our demonstrative design, N_c is chosen to be 4. For TDC, when the FQ switches from logic LOW to HIGH, i.e., the circuit CPTD switches from the discharging process to the charging process, $STHN$ of this BCU will be reset to HIGH by DFF2. Then, DFF3 will send a HIGH to reset DFF1. As a result, output Q of DFF1 resets DFF3 again to make it ready for the next judgment to see whether the PLL has entered into the locked-in state. When the value of N_c of TDC exceeds 4, the third bit of counter is HIGH, i.e., $STHP = 1$. Consequently V_{set} becomes HIGH. At the same time, $STHN$ becomes LOW by DFF2. This $V_{set} = 1$ will make the PLL set into the locked-in state, i.e., the CP and the LF of the narrower bandwidth will be in operation to give a lower jitter. In the above, whenever $FQ = 1$, DFF2 and DFF3 are cleared.

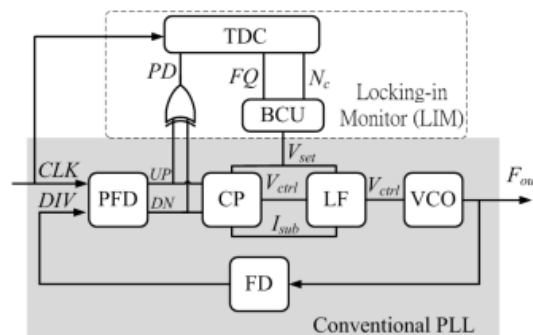


Fig. 2 Adaptive PLL with LIM

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Vol. 5, Issue 5, May 2016

IV. RESULTS

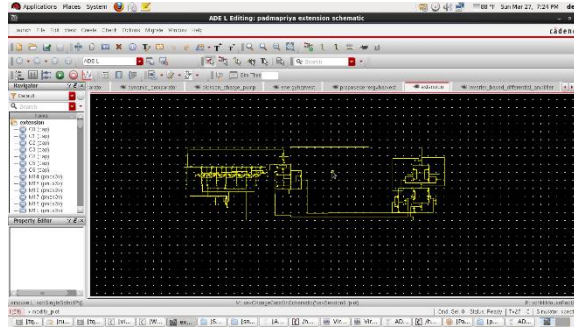


Fig. 3 TDC Architecture

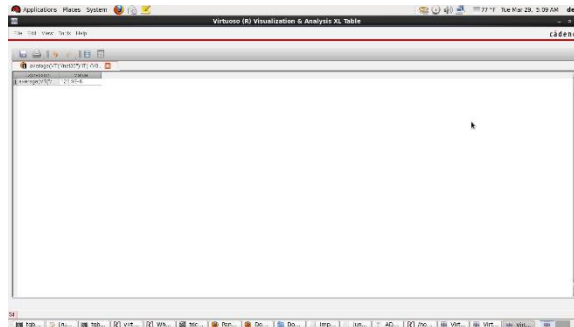


Fig. 4 Architecture for Power Consuming

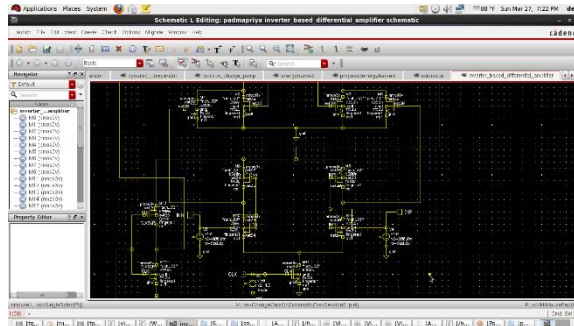


Fig. 5 Inverter Based Differential Amplifier

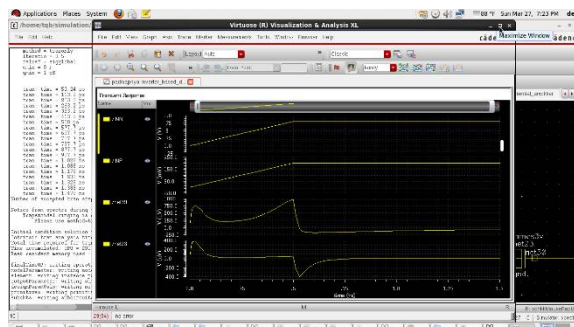


Fig. 6 Output Waveform for Analog IO

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 5, May 2016

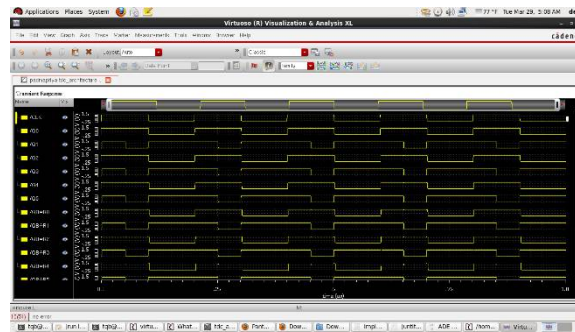


Fig. 7 Output waveform for Digital IO

V. CONCLUSION

A digitally controlled adaptive PLL, which utilizes digital TDC and BCU to accomplish the locked-in state detection with a bandwidth control algorithm. The algorithm uses a fixed phase threshold with a delay-independent dual-slope transfer function to achieve the bandwidth control. A design for the hysteresis comparator using the positive feedback to achieve the robust thresholds eliminates the use of a reference voltage, which was used in the conventional adaptive PLL designs. Also, a process-immune charge pump circuit is also incorporated. These altogether make the proposed adaptive PLL insensitive to the process variations. Simulation and the implemented chip measurement results show that the PLL is process variation immune and demonstrate the fast locking-in while still maintain the low jitter performance.

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