

Design and Implementation of CLA Using Reversible Logic Gates

S.T.Suria, M.Jenath^(*)

Department of Electronics and Communication Engineering, Adhiparasakthi Engineering College, Melmaruvathur, Chennai, India

ABSTRACT: Reversible logic is a popular concept in energy efficient computations and this will be the demand for upcoming future computing technologies. Reversible logic is emerging as an important research area and it will be having wide applications in many fields such as optical information processing, quantum computing and Low power CMOS design. The main purpose of designing reversible logic is to decrease quantum cost, depth of the circuits and the number of garbage outputs. Reversible are circuits (gates) that have one to one mapping between vectors of inputs and outputs; thus the vector of input states can be always reconstructed from the vector of output states. Reversible logic is playing a significant role in quantum computing as quantum operations are unitary in nature. Quantum computer performs computation at an atomic level; thereby doing high performance computations beyond the limits of the conventional computing systems. Reversible arithmetic units such as adders, subtractors, multipliers form the essential component of a quantum computing system. Among the adder designs, carry look-ahead is widely used in high performance computing due to its $O(\log n)$ depth. In this work, we present improved designs of both in-place and out-of-place reversible carry look-ahead adder proposed. The proposed designs utilize the properties of the Reversible Peres gate to optimize the logic depth, quantum cost and gate count compared to the existing designs proposed to both the improved designs assume no input carry ($C_0=0$). While the first approach makes use of ancilla bits to store the sum outputs, the second approach stores the sum outputs in one of the input locations.

KEYWORDS: Reversible logic gates, Reduced garbage output, Quantum cost, Low power design, Carry look-ahead adder, Peres gate, Ancilla bits.

I. INTRODUCTION

The demand for implementing ultralow-power digital systems in many modern applications, such as mobile systems, sensor networks, and implanted biomedical systems, has increased the importance of designing logic circuits in subthreshold regime. These emerging applications have low energy as the primary concern instead of performance, with the eventual goal of harvesting energy from the environment.

The heat dissipated in the circuit will gradually decrease the performance and also life span of the circuit or device. In order to overcome these types of problems, we require low power consumption and less dissipation components in the circuit. He proposed two conditions of reversibility. 1st condition: For any device to be reversible if its input and output will be uniquely retrievable from each other called logical reversibility. 2nd condition: A device can run actually backwards then it is called physically reversible.

The reversible circuits are those in which reversible logic gates are basic building blocks and there is no energy loss. The reversible logic gates will be having n -input and n -output i.e. equal number of input and equal number of output, and also with one-to-one mapping i.e. inputs can be uniquely recovered from the outputs. Reversible logic supports the process of running the system both forward and backward.

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II. REVERSIBLE LOGIC

The reversible logic gate will generate unique output vector from unique input vector or vice-versa. In reversible logic, Input vector is $Iv=(I_1, I_2, I_3 \dots I_n)$ and Output vector is $Ov=(O_1, O_2, O_3 \dots O_n)$, For each particular vector $j Iv \leftrightarrow Ov$.

Fig.1 shows a general reversible gate; the gate will be having k inputs and k outputs and it is called $k \times k$ reversible gate. In reversible gates, fan-out are not permitted. No feedback paths are allowed i.e. circuit is acyclic. Some important factors are Garbage output, constant input etc. Garbage output is the un-utilized output from the reversible gate, very much essential to achieve reversibility and it must be not used for further computation. Constant inputs are those that will be added to $k \times k$ function to make it reversible. For an optimized reversible circuit, the number of garbage outputs, the number of constant inputs and the number of reversible gates used should be minimum.

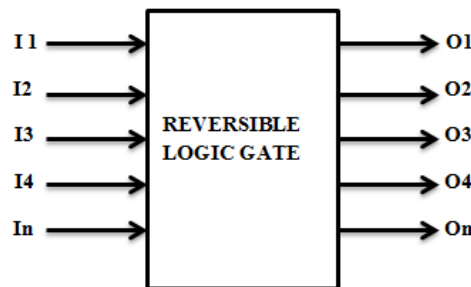


Fig.1. General reversible gate

In the design of reversible logic circuits the following points must be considered to achieve an optimized circuit. They are:

- Fan-out is not allowed.
- Loop or feedback is not permitted.
- Garbage outputs should be minimum.
- Minimum delay.
- Minimum quantum cost.

FREDKIN GATE (FRG)

The input vector is $I(A, B, C)$ and the output vector is $O(P, Q, R)$. The output is defined by $P=A$, $Q=A'B \oplus AC$ and $R=A'C \oplus AB$. The Quantum cost of a Fredkin gate is 5.

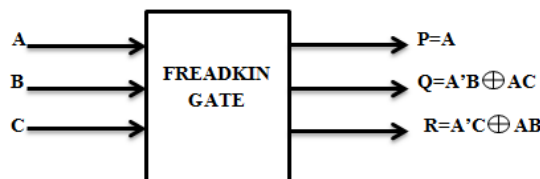


Fig.2:3*3 Fredkin gate.

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TRUTH TABLE OF PARITY PRESERVING FREDKIN GATE

Input			Output		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

NEW FAULT TOLERANT GATE (NFT)

The NFT gate is a 3*3 Reversible gate with three inputs and three outputs[8]. The input vector is I(A, B, C) and the output vector is O(P, Q, R). The output is defined by $P=A \oplus B$, $Q=BC \oplus AC'$, $R=BC \oplus AC'$ and is shown in the Fig. 4. The Quantum cost of a NFT gate is 5.

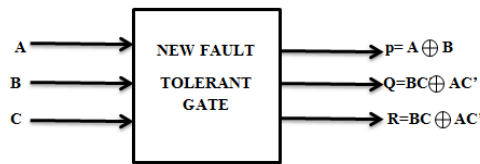


Fig 3.3*3 NFT gate.

TRUTH TABLE OF PARITY PRESERVING NFT GATE

Input			Output		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	1	0	0
0	1	1	1	0	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	0	1	1
1	1	1	0	0	1

MODIFIED IG GATE (MIG)

The MIG gate is a 4*4 Reversible gate with four inputs and four outputs[8]. The input vector is I(A, B, C, D) and the output vector is O(P, Q, R, S). The output is defined by $P=A$, $Q=A \wedge B$, $R=(A \wedge B) \wedge C$, $S=(A \wedge B) \wedge D$ and is shown in the Fig. 5. The Quantum cost of a MIG gate is 7.

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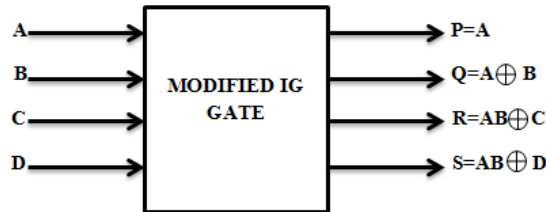


Fig 4.4*4 MIG gate.

TRUTH TABLE OF PARITY PRESERVING MIG GATE

Input				Output			
A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1
0	1	0	0	0	1	0	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	0
0	1	1	1	0	1	1	1
1	0	0	0	1	1	0	1
1	0	0	1	1	1	0	0
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	0
1	1	1	1	1	0	0	1

INPUT			OUTPUT		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

FEYNMAN GATE

Feynman gate is a 2x2 reversible gate. The input vector is I(A,B) and the output vector is O(P,Q). The output defined by $P=A, Q=A \oplus B$. Quantum cost of a Feynman gate is 1. Feynman gate can be used as copying gate.

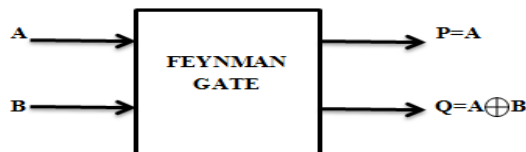


Fig 5.2*2 Feynman gate

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TRUTH TABLE OF FEYNMAN GATE

INPUT		OUTPUT	
A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

TOFFOLI GATE

Toffoli gate is 3x3 reversible gate. The input vector is I(A,B,C) and the output vector is O(P,Q,R).The outputs are defined by $P=A, Q=B, R=AB \oplus C$. Quantum cost of a TOFFOLI gate is 5.

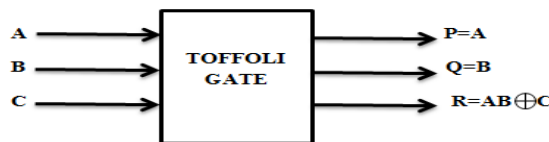


Fig 6: 3*3 Toffoli gate

PERES GATE

Peres gate is 3x3 reversible gate. The input vector is I(A,B,C) and the output vector is O(P,R,S).The output is defined by $P=A, Q=A \oplus B$ and $R=AB \oplus C$. Quantum cost of a Peres gate is 4.

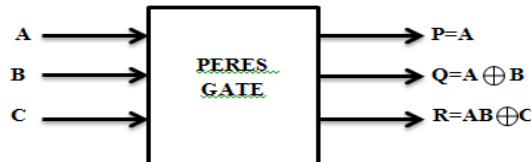
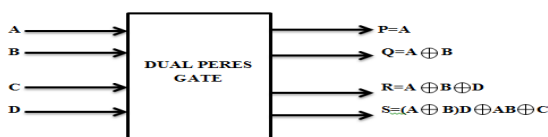


Fig 7: Peres gate

TRUTH TABLE OF PERES GATE:

DOUBLE PERES GATE (DPG)

DPG gate is 4x4 reversible gate. The input vector is I(A,B,C,D) and the output vector is O(P,Q,R,S). The output is $P=A, Q=A \oplus B, R=A \oplus B \oplus D$ and $S=(A \oplus B)D \oplus AB \oplus C$. Quantum cost of DPG gate is 6.It can work singly as Reversible full adder with $C=0$ and $D=Cin$.



INPUT			OUTPUT		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

Fig 8.4*4 dual peres gate

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TRUTH TABLE OF DUAL PERES GATE

INPUT				OUTPUT			
A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	1	0
1	0	0	1	1	1	1	1
1	0	1	0	1	1	0	1
1	0	1	1	1	1	0	0
1	1	0	0	1	0	0	1
1	1	0	1	1	0	0	0
1	1	1	0	1	0	1	1
1	1	1	1	1	0	1	0

CARRY LOOK-AHEAD ADDER

Carry look-ahead adder are fastest adder of all adders because it calculates the carry bits before the summation. Carry look-ahead adder actually determines the carry bit by two modules first is “generate a carry” and second is “propagate a carry”. Carry signal will be generated in two conditions. When both bits A_i and B_i are equal to 1 or when carry-in is 1 and A_i or B_i is 1.

Carry propagation (P_i) and Carry generation (G_i) are

$$P_i = A_i \oplus B_i$$

$$G_i = A_i \cdot B_i$$

Sum signal can be calculated as follows:

$$S_i = A_i \oplus B_i \oplus C_i = P_i \oplus C_i$$

Carry signal can be calculated as

$$C_{i+1} = G_i \oplus P_i \cdot C_i$$

Applying this to a 4-bit adder ,we have:

$$C_1 = G_0 \oplus P_0 C_0$$

$$C_2 = G_1 \oplus P_1 C_1 = G_1 \oplus P_1(G_0 \oplus P_0 C_0)$$

$$C_3 = G_2 \oplus P_2 C_2 = G_2 \oplus P_2(G_1 \oplus P_1 C_1)$$

Partial Full Adder (PFA): This adder generates G_i , P_i and S_i .

$$P_i = A_i \oplus B_i,$$

$$G_i = A_i \cdot B_i,$$

$$S_i = A_i \oplus B_i \oplus C_i$$

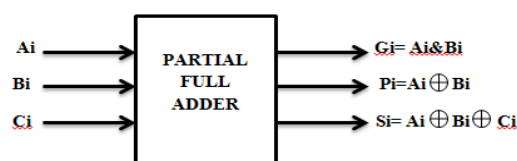


Fig 9. Partial full adder

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REVERSIBLE LOGIC CARRY LOOK AHEAD ADDER

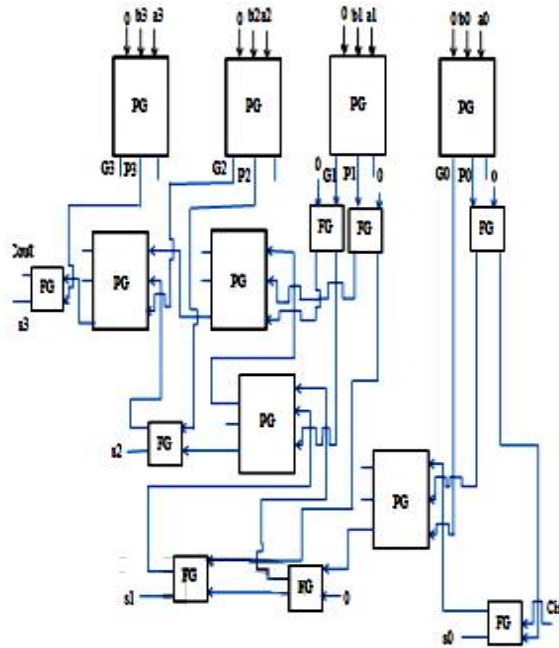


Fig.10.Architecture of proposed 4-bit reversible carry look-ahead adder

III. RESULT

SIMULATION OUTPUT

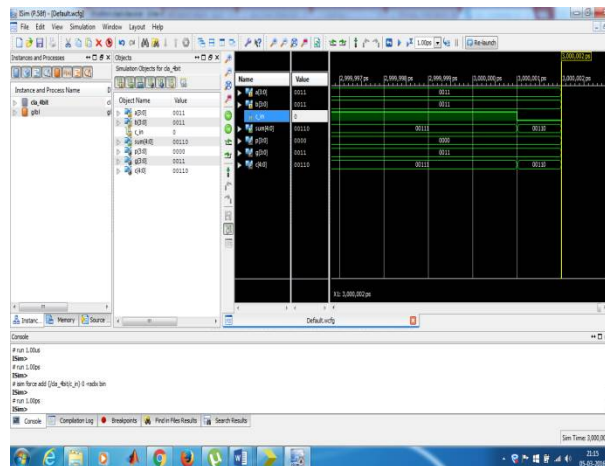


Fig.11.simulation output

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AREA

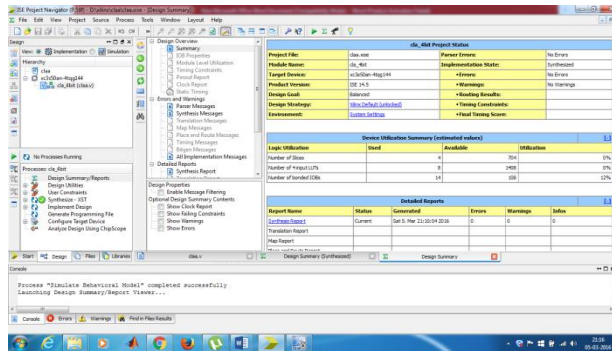


Fig.12.performance of area report

CALCULATE DELAY

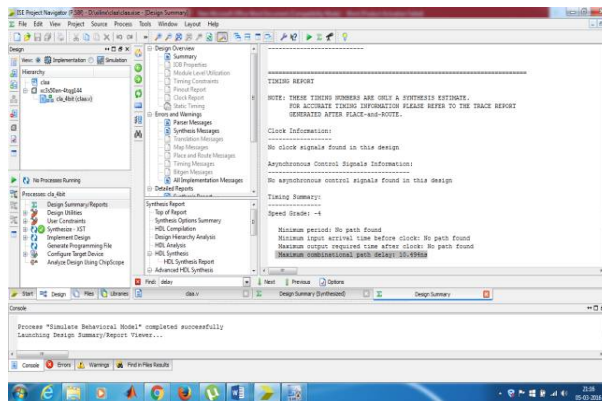


Fig.13.performance of delay

RTL DIAGRAM

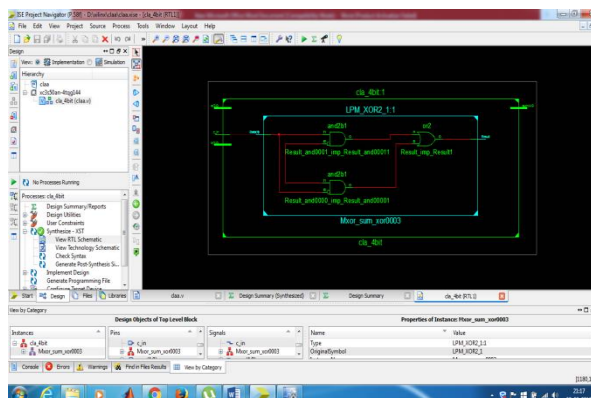


Fig.14.Performance of RTL diagram

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PROCESS OF TECHNOLOGY

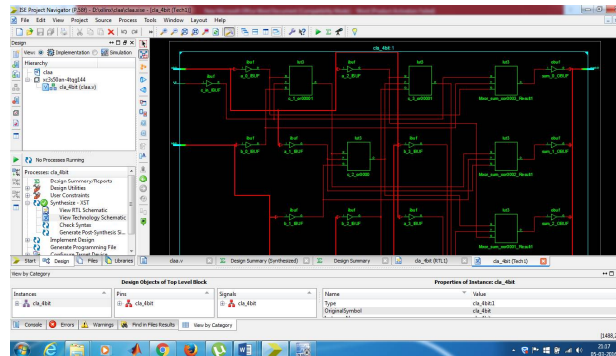


Fig.15.Technology diagram

POWER CONSUMPTION

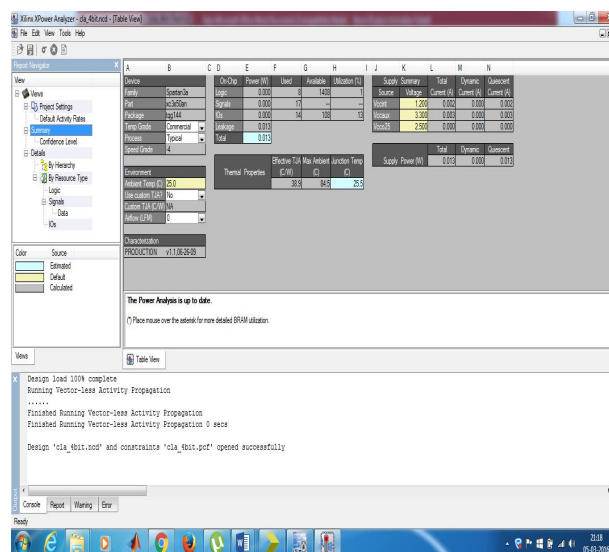


Fig.16.power consumption diagram

IV. CONCLUSION

Reversible logic gates are used to Reduced the power consumption, Minimum delay ,Garbage outputs should be minimum, Minimum quantum cost, performance is high due to area is reduced.

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