

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 5, May 2016

Design and Implementation Mechanism of Aging-Aware Reliable Multiplier by Using Adaptive Hold Logic

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ABSTRACT: Advanced multipliers are among the most critical arithmetic functional units. The general execution of these frameworks relies on upon the throughput of the multiplier. In the meantime, the negative inclination temperature flimsiness impact happens when a pMOS transistor is under negative predisposition ($V_{gs} = -V_{dd}$), expanding the limit voltage of the pMOS transistor, and diminishing multiplier speed. A comparable wonder, positive predisposition temperature unsteadiness, happens when anMOS transistor is under positive inclination. Both impacts corrupt transistor speed, and in the long haul, the framework may fizzle because of timing infringement. Along these lines, it is critical to outline solid superior multipliers. In this paper, we propose a maturing mindful multiplier outline with novel versatile hold rationale (AHL) circuit. The multiplier can give higher throughput through the variable inactivity and can conform the AHL circuit to relieve execution corruption that is because of the maturing impact. Besides, the proposed design can be connected to a section or column bypassing multiplier. The trial results demonstrate that our proposed engineering with 16×16 and 32×32 segment bypassing multipliers can accomplish up to 62.88% and 76.28% execution change, separately, contrasted and 16×16 and 32×32 settled inertness section bypassing multipliers. Besides, our proposed engineering with 16×16 and 32×32 line bypassing multipliers can accomplish up to 80.17% and 69.40% execution change as contrasted and 16×16 and 32×32 altered inactivity column bypassing multipliers. Likewise we expelled the tristate cushion from the segment by pass multiplier. With the goal that we can diminish the door number and enhance the effectiveness and speed and decrease the force utilization.

KEYWORDS: Adaptive hold logic (AHL), negative bias temperature instability (NBTI), positive bias temperature instability (PBTI), reliable multiplier, variable latency.

I. INTRODUCTION

DIGITAL multipliers are among the most basic number-crunching utilitarian units in numerous applications, for example, the Fourier change, discrete cosine changes, and advanced separating. The throughput of these applications relies on upon multipliers, and if the multipliers are too moderate, the execution of whole circuits will be diminished. Moreover, negative predisposition temperature insecurity (NBTI) happens when a pMOS transistor is under negative inclination ($V_{gs} = -V_{dd}$). In this circumstance, the cooperation between reversal layer gaps and hydrogen-lack of involvement Si iotas break the Si-H security created amid the oxidation procedure, producing H or H₂ particles. At the point when these atoms diffuse away, interface traps are cleared out. The gathered interface traps amongst silicon and the door oxide interface result in expanded limit voltage (V_{th}), decreasing the circuit exchanging speed. At the point when the one-sided voltage is evacuated, the opposite response happens, diminishing the NBTI impact. Be that as it may, the opposite response does not dispense with all the interface traps produced amid the anxiety stage, and V_{th} is expanded in the long haul. Henceforth, it is vital to plan a solid elite multiplier. The comparing impact on anMOS

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transistor is prone to pre-irradiation temperature instability (PBTI), which happens when a nMOS transistor is under positive bias. Contrasted with the NBTI impact, the PBTI impact is much smaller on oxide/polygate transistors, and subsequently is generally overlooked. In any case, for high-k/metal-gate nMOS transistors with noteworthy charge trapping, the PBTI impact can never again be overlooked. Truth be told, it has been demonstrated that the PBTI impact is more huge than the NBTI impact on 32-nm high-k/metal-gate forms. A customary technique to relieve the maturing impact is overdesign [5], [6], including such things as watchman banding and door oversizing; be that as it may, this methodology can be extremely negative and territory and force wasteful. To keep away from this issue, numerous NBTI-mindful approaches have been proposed. A NBTI-mindful innovation mapping system was proposed into certification the execution of the circuit amid its lifetime. In], a NBTI-mindful rest transistor was intended to diminish the maturing consequences for pMOS rest transistors, and the lifetime steadiness of the force gated circuits under thought was moved forward. Wu and proposed a joint rationale rebuilding and stick reordering technique, which depends on identifying utilitarian symmetries and transistor stacking impacts. They likewise proposed a NBTI improvement strategy that considered way refinement dynamic voltage scaling and body-biasing methods were proposed to decrease control or develop circuit life. These methods, be that as it may, require circuit alteration or don't give streamlining of particular circuits. Customary circuits use basic way postpone as the general circuit check cycle keeping in mind the end goal to perform accurately. Notwithstanding, the likelihood that the basic ways are initiated is low. As a rule, the way defer is shorter than the basic way. For these noncritical ways, utilizing the basic way postpone as the general cycle time frame will bring about critical planning waste. Thus, the variable-idleness configuration was proposed to decrease the planning misuse of conventional circuits. Variable-inactivity outline partitions the circuit into two sections: 1) shorter ways and 2) longer ways. Shorter ways can execute effectively in one cycle, though more ways need two cycles to execute. At the point when shorter ways are enacted as often as possible, the normal inactivity of variable-dormancy outlines is superior to that of conventional plans. For instance, a few variable-idleness adders were proposed utilizing the theory strategy with blunder discovery and recuperation. A short way initiation capacity calculation was proposed into enhance the precision of the hold rationale and to upgrade the execution of the variable-dormancy circuit. A guideline booking calculation was proposed into calendar the operations on no uniform inertness useful units and enhances the execution of Very Long Instruction Word processors. In, variable-inactivity pipelined multiplier engineering with a Booth calculation was proposed. In, procedure variety tolerant engineering for number juggling units was proposed, where the impact of procedure variety is considered to build the circuit yield. Moreover, the basic ways are isolated into two shorter ways that could be unequal and the clock cycle is set to the postponement of the more one. These exploration plans could lessen the planning misuse of customary circuits to enhance execution, yet they didn't consider the maturing impact and couldn't alter themselves amid the runtime. A variable-inactivity snake plan that considers the maturing impact was proposed in and. Notwithstanding, no variable-inertness multiplier plan that considers the maturing impact and can modify powerfully has been finished.

In this paper, we propose an aging-aware reliable multiplier design with novel adaptive hold logic (AHL) circuit. The multiplier is based on the variable-latency technique and can adjust the AHL circuit to achieve reliable operation under the influence of NBTI and PBTI effects. To be specific, the contributions of this paper are summarized as follows:

- 1) Novel variable-latency multiplier architecture with an AHL circuit. The AHL circuit can decide whether the input patterns require one or two cycles and can adjust the judging criteria to ensure that there is minimum performance degradation after considerable aging occurs.
- 2) Comprehensive analysis and comparison of the multiplier's performance under different cycle periods to show the effectiveness of our proposed architecture.
- 3) an aging-aware reliable multiplier design method that issuitable for large multipliers. Although the experiment is performed in 16- and 32-bit multipliers, our proposed architecture can be easily extended to large designs.

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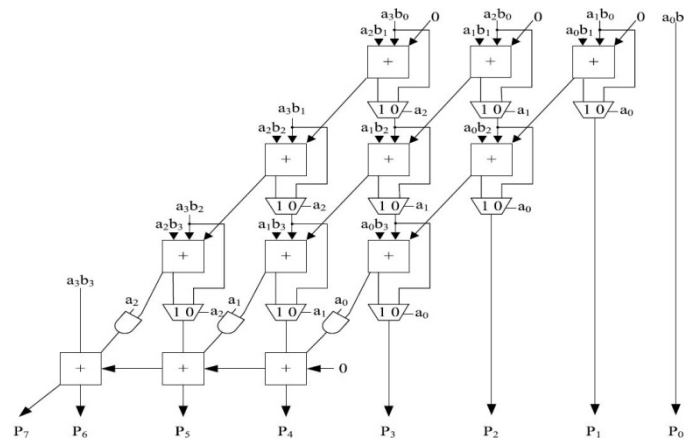


Fig. 1. 4×4 column-bypassing multiplier.

II. PRELIMINARIES

A. Column-Bypassing Multiplier

A section bypassing multiplier is a change on the ordinary exhibit multiplier (AM). The AM is a quick parallel AM. The multiplier cluster comprises of $(n-1)$ columns of convey spare viper (CSA), in which every line contains $(n-1)$ full snake (FA) cells. Every FA in the CSA cluster has two yields: 1) the whole piece goes down and 2) the convey bit goes to the lower left FA. The last line is a swell snake for convey engendering. The FAs in the AM are constantly dynamic paying little mind to info states. In [22], a low-control section bypassing multiplier outline is proposed in which the FA operations are debilitated if the relating bit in the multiplicand is 0 it demonstrates a 4×4 segment bypassing multiplier. Assuming the inputs are $10102 * 11112$, it can be seen that for the FAs in the first and third diagonals, two of the three information bits are 0: the convey bit from its upper right FA and the incomplete item $a_i b_i$. In this way, the yield of the adders in both diagonals is 0, and the yield whole piece is just equivalent to the third piece, which is the aggregate yield of its upper FA.

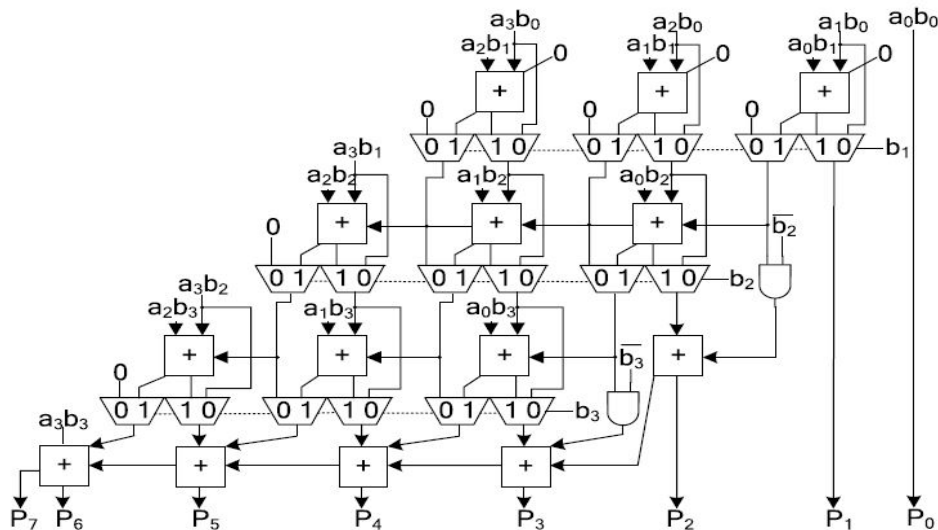


Fig 2 Column-Bypassing Multiplier

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Selector of the multiplexer to decide the output of the FA, and $aican$ also be used as the selector of the tristate gate to turn off the input path of the FA. If $aais$ 0, the inputs of FA are disabled, and the sum bit of the current FA is equal to the sum bit from its upper FA, thus reducing the power consumption of the multiplier. If $aais$ 1, the normal sum result is selected. More details for the column-bypassing multiplier can be found in [2].

B. Row-Bypassing Multiplier

A low-control line bypassing multiplier [23] is likewise proposed to lessen the action force of the AM. The operation of the low-control line bypassing multiplier is like that of the low-control section bypassing multiplier; however the selector of the multiplexers and the tristate entryways utilize the duplication It is a 4×4 line bypassing multiplier. Every info is associated with a FA through a tristate door. At the point when the inputs are $11112 * 10012$, the two inputs in the first and second columns are 0 for FAs. Since $b1$ is 0, the multiplexers in the principal column select $aib0$ as the aggregate piece and select 0 as the convey bit. The inputs are avoided to FAs in the second columns, and the tristate doors turn off the info ways to the FAs. In this way, no exchanging exercises happen in the main line FAs; consequently, control utilization is diminished. Additionally, in light of the fact that $b2$ is 0, no exchanging exercises will happen in the second-push FAs. Notwithstanding, the FAs must be dynamic in the third column in light of the fact that the $b3$ is not zero. More subtle elements for the line bypassing multiplier can likewise be found in [3].

C. Variable-Latency Design

Section I mentioned that the variable-latency design was proposed to reduce the timing waste occurring in traditional circuits that use the critical path cycle as an execution cycle period. The basic concept is to execute a shorter path using a shorter cycle and longer path using two cycles. Since most paths execute in a cycle period that is much smaller than the critical path delay, the variable-latency design has smaller average latency. For example It is an 8-bit variable-latency ripple carry adder (RCA). $A8-A1, B8-B1$ are 8-bit inputs, and $S8-S1$ are

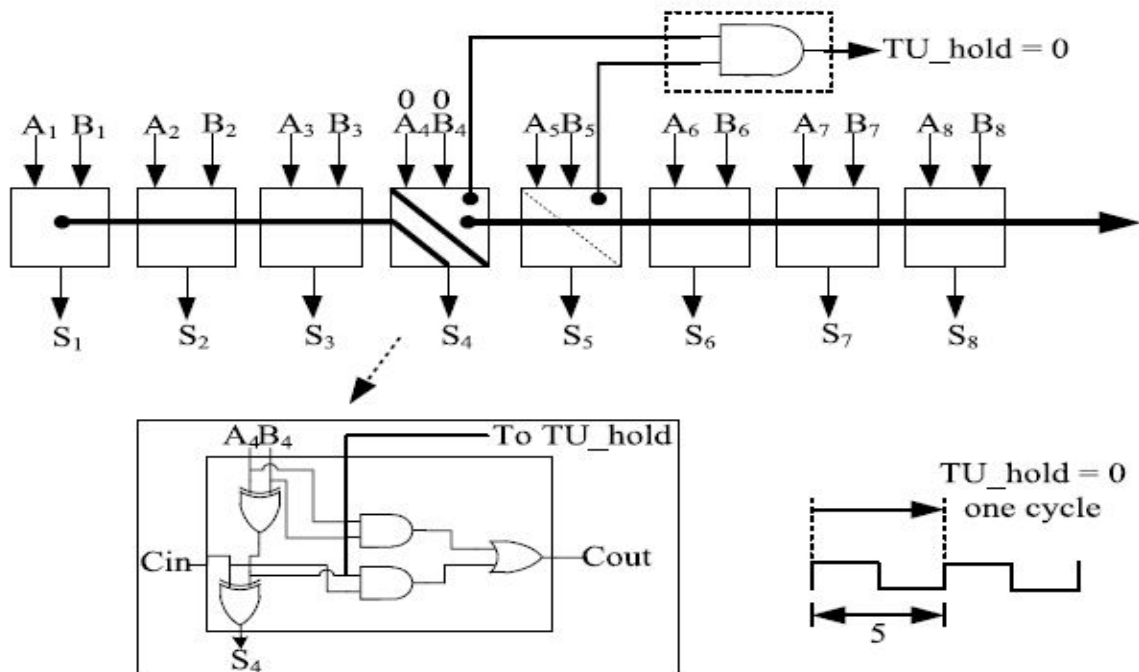


Fig. 3. 8-bit RCA with a hold logic circuit.

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D. Aging Model

As mentioned in Section I, the NBTI (PBTI) effect occurs when a pMOS (nMOS) transistor is under negative (positive) bias voltage, resulting in V_{th} drift. When the bias voltage is removed, the recovery process occurs, reducing the V_{th} drift.

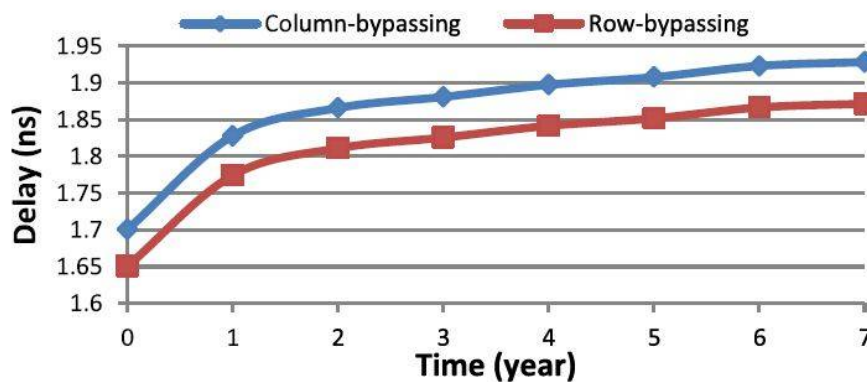


Fig. 4. Trend for circuit aging for a 16×16 column-bypassing multiplier.

$$K_{DC} = A \times T_{OX} \times \sqrt{C_{OX}(V_{GS} - V_{th})} \times [1 - V_{DS}/\alpha(V_{GS} - V_{th})] \times \exp(E_{OX}/E_0) \times \exp\left(-\frac{E_a}{kT}\right)$$

Where A is a constant and T_{OX} is the oxide thickness. E_{OX} is the gate electric field, which is $(V_{GS} - V_{th})/T_{OX}$; k is the Boltzmann constant, and T is the temperature. E_0 and E_a are technology-independent characteristics of the reaction that are equal to 1.9–2.0 MV/cm and 0.12 eV, respectively. More details about this model can be found in [26]. In this paper, we use 32-nm high- k metal gate models. We set the temperature at 125 °C in our simulation and use the above BTI model to predict the BTI effect on the circuits. It shows the simulated delays of the 16×16 column and row-bypassing multipliers under a seven-year NBTI/PBTI effect. It can be seen that the BTI effect increased the critical path circuit delay by ~13%. Hence, if the BTI effect is not considered during circuit design, the increased delay may cause system failure in the long term.

IV. PROPOSED AGING-AWARE MULTIPLIER

This section details the proposed aging-aware reliable multiplier design. It introduces the overall architecture and the functions of each component and also describes how to design AHL that adjusts the circuit when significant aging occurs.

A. Proposed Architecture

It shows our proposed aging-aware multiplier architecture, which includes two m -bit inputs (m is a positive number), one $2m$ -bit output, one column- or row-bypassing multiplier, $2m$ 1-bit Razor flip-flops [27], and an AHL circuit.

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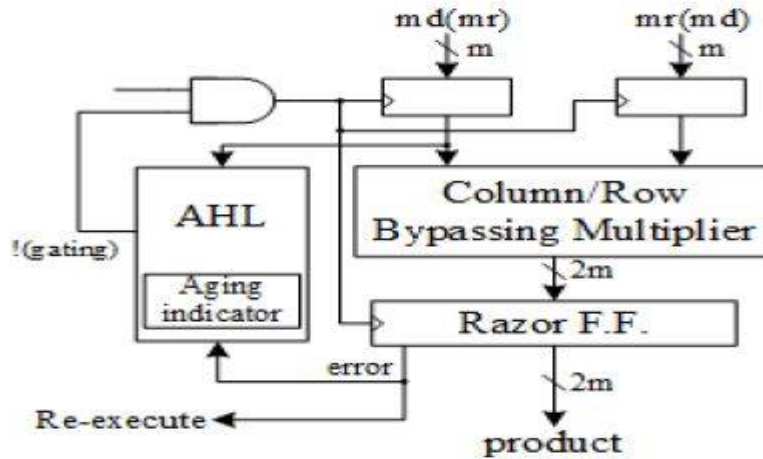


Fig. 5. Proposed architecture (md means multiplicand; mr means multiplication).

The inputs of the row-bypassing multiplier are the symbols in the parentheses. In the proposed architecture, the column- and row-bypassing multipliers can be examined by the number of zeros in either the multiplicand or multiplication to predict whether the operation requires one cycle or two cycles to complete.

When input patterns are random, the number of zeros and ones in the multiplication and multiplicand follows a normal distribution. Therefore, using the number of zeros or ones as the judging criteria results in similar outcomes. Hence, the two aging-aware multipliers can be implemented using similar architecture, and the difference between the two bypassing multipliers lies in the input signals of the AHL. According to the bypassing selection in the columnar row-bypassing multiplier, the input signal of the AHL in the architecture with the column-bypassing multiplier is the multiplicand, whereas that of the row-bypassing multiplier is the multiplication. Razor flip-flops can be used to detect.

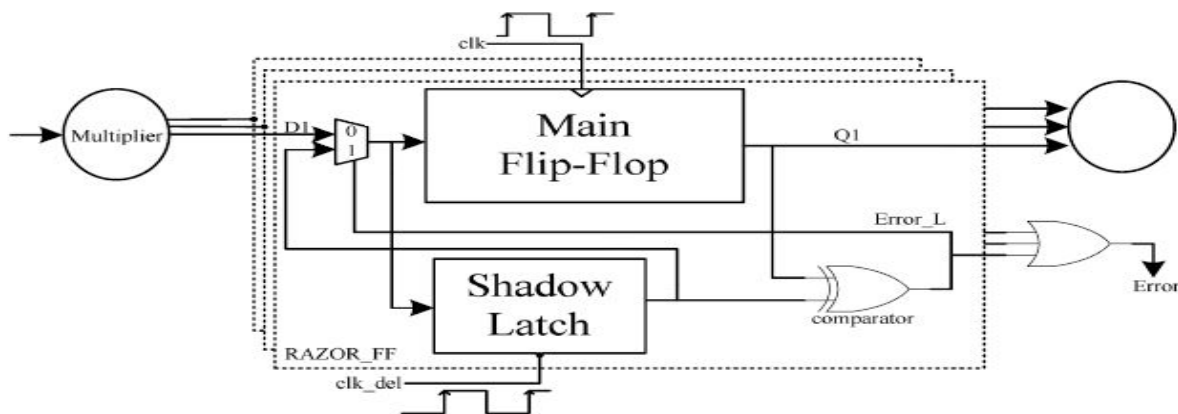


Fig 06 Razor flip flops.

Points of interest of Razor flip-flops. A 1-bit Razor flip-flop contains a principle flip-flop, shadow hook, XOR door, and mux. The principle flip-flop gets the execution result for the mix circuit utilizing a typical clock signal, and the shadow hook gets the execution result utilizing a postponed clock signal, which is slower than the ordinary clock signal. In the event that the hooked piece of the shadow lock is not quite the same as that of the principle flip-floander, this implies the way defer of the present operation surpasses the cycle time frame, and the fundamental flip-flop gets a wrong result. In the event that blunders happen, the Razor flip-failure will set the mistake sign to 1 to advise the

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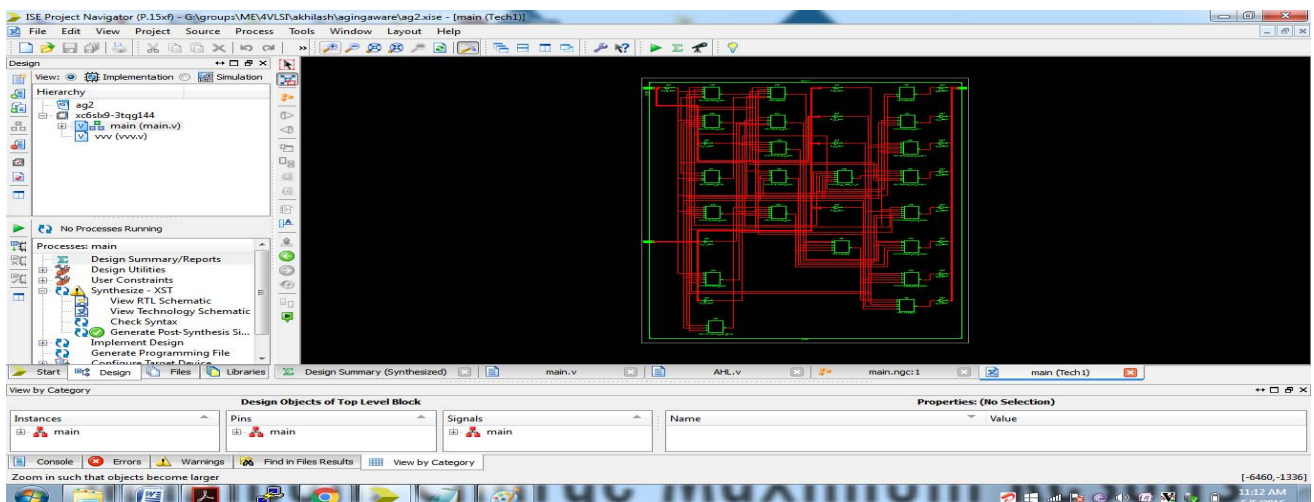
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framework to reexecute the operation and tell the AHL circuit that a blunder has happened. We utilize Razor flip-failures to distinguish whether an operation that is thought to be a one-cycle example can truly complete in a cycle. If not, the operation is reexecuted with two cycles. Despite the fact that the reexecution may appear to be expensive, the general expense is low in light of the fact that the reexecution recurrence is low. More points of interest for the Razor flip-failure can be found. The AHL circuit is the key segment in the maturing product variable-dormancy multiplier. It demonstrates the subtle elements of the AHL circuit. The AHL circuit contains a maturing pointer, two judging squares, one mux, and one D flip-flop. The maturing marker demonstrates whether the circuit has endured huge execution debasement because of the maturing impact. The maturing marker is executed in a straightforward counter that tallies the quantity of blunders over a specific measure of operations and is reset to zero toward the end of those operations. In the event that the cycle period is too short, the section or line bypassing multiplier is not ready to finish these operations effectively, creating timing infringement. These planning infringement will be gotten by the Razor flip-flops, which create mistake signals. On the off chance that blunders happen much of the time and surpass a predefined limit, it implies the circuit has endured critical planning debasement because of the maturing impact, and the maturing pointer will yield signal 1; else, it will yield 0 to show the maturing impact is still not noteworthy, and no activities are required.

V. EXPERIMENTAL RESULT

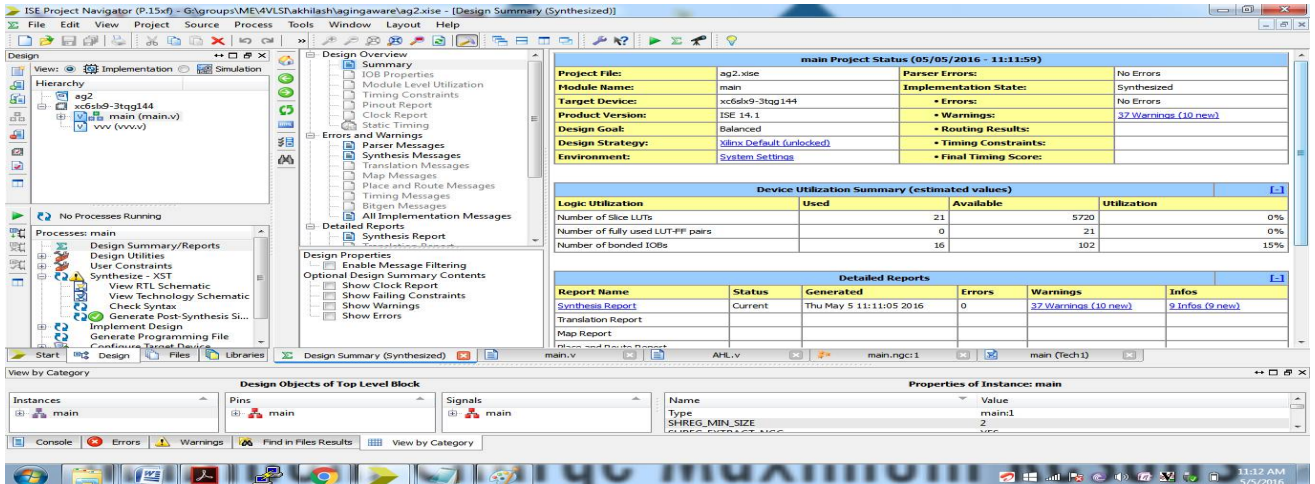
Our experiments are conducted in a Linux operating system. We adopt a 32-nm high- k predictive technology model [1] to estimate the BTI degradation for seven years. The proposed multiplier is designed in Verilog and converted to SPICE files using SpringSoft Laker. Then SynopsysNanosim is used to analyze the delay and power of the circuit. The Vthdrift caused by BTI is estimated using the BTI model proposed in Section II-D and is added into the SPICE files during Simulation. In the variable-latency design, the average latency is affected by both the percentage of one-cycle patterns and the cycle period. If more patterns only require one cycle, the average latency is reduced. Similarly, if the cycle period is reduced, the average latency is also reduced. However, the cycle period cannot be too small. If the cycle period is too small, large amounts of timing violations will be detected by the Razor flip-flops, and the average latency will increase. Hence, it is important to analyze the tradeoff between the percentage of one-cycle patterns and the cycle period. To achieve this, we analyze three scenarios for both 16×16 and 32×32 variable latency column-bypassing (VLCB) and variable-latency row bypassing (VLRB) multipliers. We also compare the results with the AM, a FLCB multiplier, and a fixed-latency row bypassing (FLRB) multiplier.



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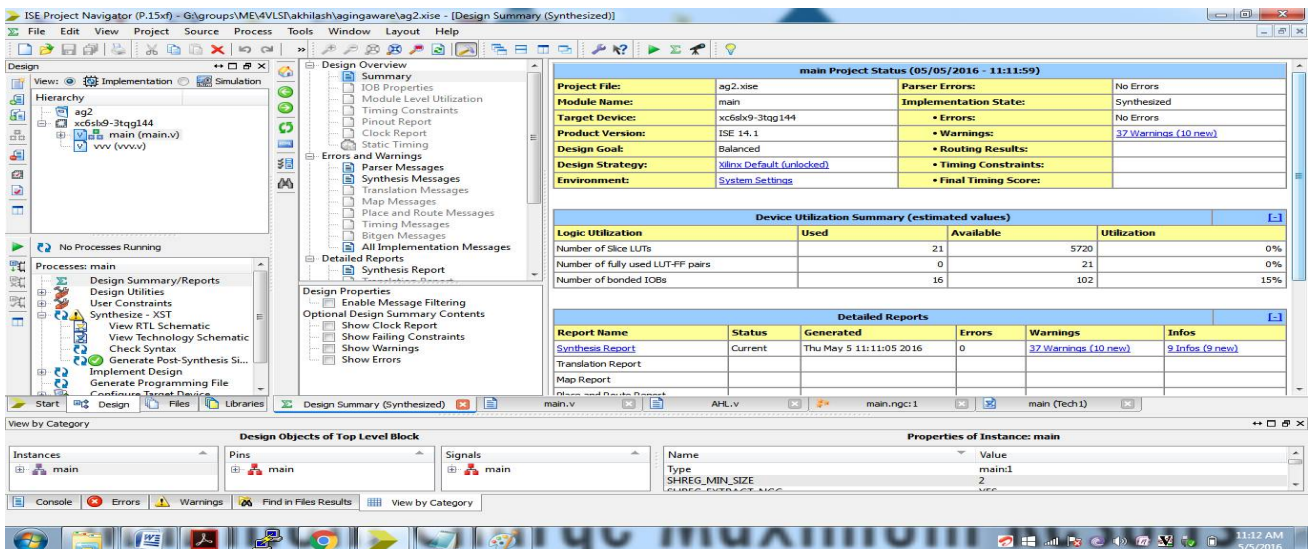


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Module Name:	main	Implementation State:	Synthesized
Target Device:	xc6slx9-3tqg144	Errors:	No Errors
Product Version:	ISE 14.1	Warnings:	37 Warnings (10 new)
Design Goal:	Balanced	Routing Results:	
Design Strategy:	Xilinx Default (unlocked)	Timing Constraints:	
Environment:	System Settings	Final Timing Score:	

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice LUTs	21	5720	0%
Number of fully used LUT-FF pairs	0	21	0%
Number of bonded IOBs	16	102	15%

Detailed Reports				
Report Name	Status	Generated	Errors	Warnings
Synthesis Report	Current	Thu May 5 11:11:05 2016	0	37 Warnings (10 new)
Translation Report				9 Infos (9 new)
Map Report				



main Project Status (05/05/2016 - 11:11:59)

Project File:	ag2.xise	Parser Errors:	No Errors
Module Name:	main	Implementation State:	Synthesized
Target Device:	xc6slx9-3tqg144	Errors:	No Errors
Product Version:	ISE 14.1	Warnings:	37 Warnings (10 new)
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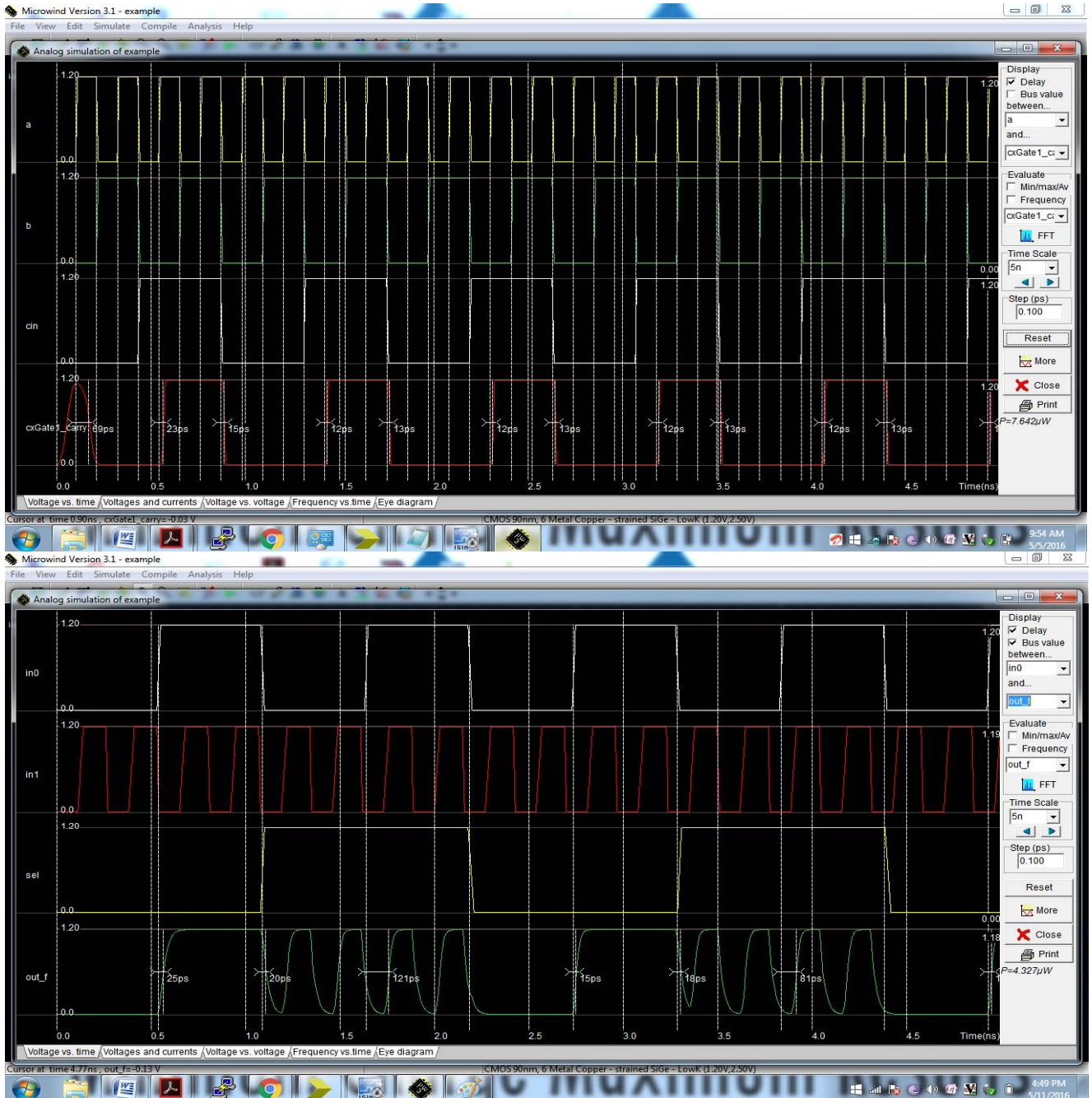
Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice LUTs	21	5720	0%
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Detailed Reports				
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Translation Report				9 Infos (9 new)
Map Report				

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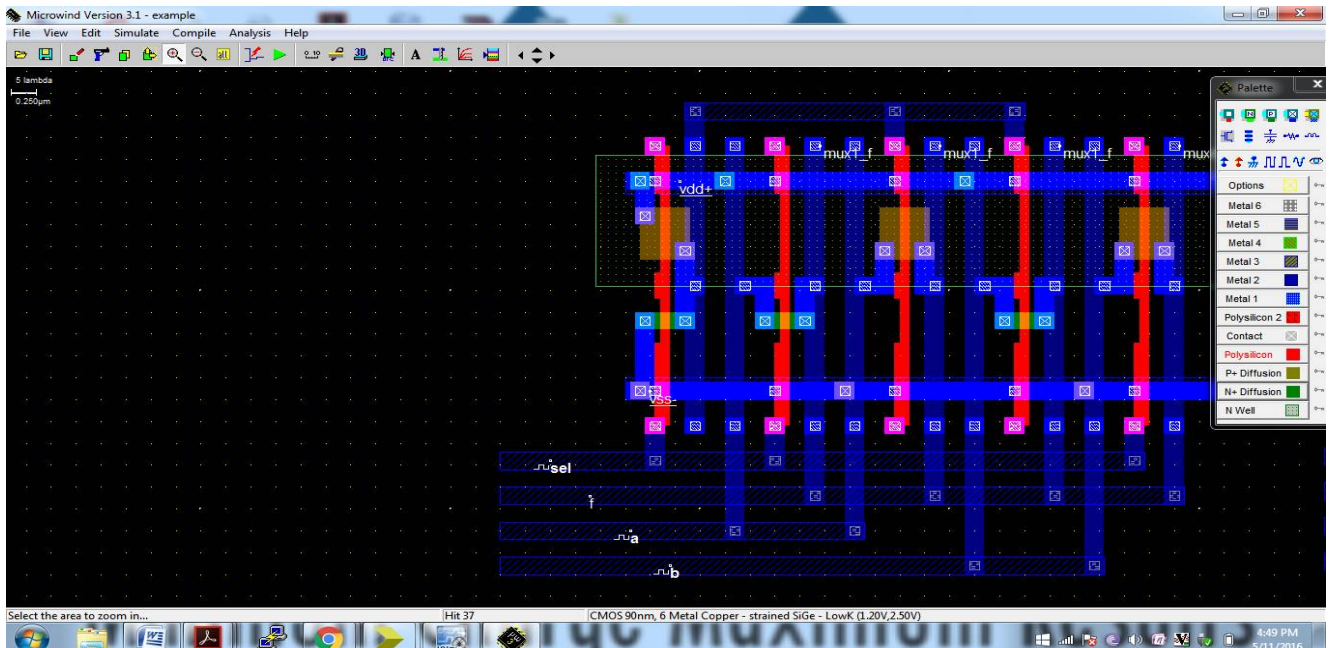
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A. Average Latency Comparison

We first compare the average latency of the AM, FLCB,FLRB, VLCB, and VLRB multipliers in both 16×16 and 32×32 multipliers. In the case of the 16×16 variable-latency bypassing multiplier, there are three scenarios: 1) Skip-7; 2) Skip-8; and 3) Skip-9. For VLCB multipliers, Skip-7 means the patterns that have seven or more zeros in the multiplicand are regarded as one-cycle patterns, and Skip-8 means the patterns that have eight or more zeros in the multiplicand are regarded as one cycle patterns, and so on. Similarly, for VLRB multipliers, Skip-7 means the patterns that have seven or more zeros in the multiplication are regarded as one-cycle patterns, and Skip-8 means the patterns that have eight or more zeros in the multiplication are regarded as one-cycle patterns, and so on. Table I lists the one-cycle pattern ratio of a one-cycle pattern ratio in the 16×16 variable-latency bypassing multiplier.

	16x16 VLCB	16x16 VLRB
Skip-7	73.58%	77.39%
Skip-8	53.78%	59.89%
Skip-9	33.22%	40.20%

ONE-CYCLE PATTERN RATIO IN 16×16 MULTIPLIER

	32x32 VLCB	32x32 VLRB
Skip-15	66.46%	66.99%
Skip-16	52.68%	52.74%
Skip-17	38.18%	38.42%

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ONE-CYCLE PATTERN RATIO IN 32×32 MULTIPLIER

B. Latency Comparison among Different Skip Numbers

We also compare the average latency of a variable-latency bypassing multiplier under three different skip numbers it compares the average latency in the 16×16 VLCB and VLRB multipliers under three different skip numbers without the aging effect.

C. Average Latency Improved by AHL

Because of the aging effect, the circuit speed is degraded. The path delay of the one-cycle patterns becomes larger than the cycle period and causes timing violations. In this situation, the operations need to be reexecuted. If timing violations occur too frequently, the extra cycles of the reexecution will increase the average latency. In order to mitigate performance degradation, these one-cycle patterns that cause timing violations must be changed to two-cycle patterns.

D. Area Comparison

It compares the normalized area of the AM, FLCB, A-VLCB, FLRB, and A-VLRB in 16×16 and 32×32 multipliers. The data are normalized to the area of the AM. In the 16×16 multiplier, the area of the A-VLCB and A-VLRB is 22.9% and 23.5% higher than FLCB and FLRB. In the 32×32 multiplier, the area of the A-VLCB and A-VLRB is 12.3% and 5.7% higher than that of the FLCB and FLRB, respectively. This is because when a fixed-latency bypassing multiplier is changed to a variable-latency bypassing multiplier, additional circuits are needed for AHL and Razor flip-flops to ensure the correct operations of the multiplier after degradation. Note that the increased area overhead ratio of the 32×32 A-VLCB and A-VLRB is much smaller than that of the 16×16 A-VLCB and A-VLRB. This is because AHL and Razor flip-flops both occupy a smaller area ratio in larger multipliers.

E. Latency, Power, and Energy-Delay Product (EDP) Comparison of FLCB, A-VLCB, FLRB, and A-VLRB Over Seven Years it compares the latency, power, and EDP of the AM, FLCB, FLRB, A-VLCB, and A-VLRB in 16×16 multipliers from year 0 to year 7. The average latency is normalized to the latency of AM at year 0. To make comparison simpler, the cycle period of the A-VLRB and A-VLCB is set to 1.2 ns, and the skip number is 7, and therefore, no timing violations occur, and the average latency of the A-VLCB and A-VLRB are similar.

VI. CONCLUSION

This paper proposed a maturing mindful variable-idleness multiplier outline with the AHL. The multiplier can change the AHL to alleviate execution corruption because of expanded postponement. The trial results demonstrate that our proposed design with 16×16 and 32×32 section bypassing multipliers can achieve up to 62.88% and 76.28% execution change contrasted and the 16×16 and 32×32 FLCB multipliers, individually. Moreover, our proposed engineering with the 16×16 and 32×32 column bypassing multipliers can accomplish up to 80.17% and 69.40% execution change contrasted and the 16×16 and 32×32 FLRB multipliers. Moreover, the variable-dormancy bypassing multipliers showed the most minimal normal EDP and accomplished up to 10.45% EDP lessening in 32×32 VLCB multipliers. Note that notwithstanding the BTI impact that expansions transistor delay, interconnect likewise has its maturing issue, which is called electro relocation. Electro movement happens when the present thickness is sufficiently high to bring about the float of metal particles along the bearing of electron stream. The metal ions will be slowly uprooted after a timeframe, and the geometry of the wires will change. In the event that a wire gets to be smaller, the resistance and postponement of the wire will be expanded, and at last, electro movement may prompt open circuits. This issue is additionally more genuine in cutting edge process innovation since metal wires are smaller, and changes in the wire width will bring about bigger resistance contrasts. In the event that the maturing impacts created by the BTI impact and electro relocation are viewed as together, the postponement and execution debasement will be more noteworthy. Luckily, our proposed variable inertness multipliers can be utilized affected by both the BTI impact and electro relocation. Moreover, our proposed variable dormancy multipliers have less execution corruption since variable inactivity multipliers have less planning waste, however customary multipliers need to consider the debasement brought on by both the BTI impact and electro movement and utilize the most pessimistic scenario delay as the cycle time frame.

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