

Power Efficient Hardware Platform for Multicontroller Environment Based on Cots Devices

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ABSTRACT: Embedded structures are for the most part essentialness constrained. Additionally, in these structures, extended effectiveness and decreased time to market are basic for thing accomplishment. To layout complex embedded systems while lessening the progression time and cost, there is a marvelous slant to use business off-the-rack ("COTS") devices. At structure level, dynamic voltage and frequency scaling (DVFS) is a champion amongst the best frameworks for imperativeness diminish. Regardless, various by and large used COTS processors either don't have DVFS or apply DVFS just to processor focuses. An easy to-execute COTS-based evaluation stage for low-imperativeness embedded structures is shown. To achieve essentialness saving, DVFS is suited the whole microcontroller including focus, stage darter circle, memory, and I/O. Additionally, workplaces are given to attempting distinctive things with adjustment to inward disappointment methodologies. The stage is furnished with essentialness estimation and examining gear. Physical examinations exhibit that applying DVFS when all is said in done microcontroller offers up to 47% and 12% essentialness saving differentiated and the sole usage of component power organization and applying DVFS just on the inside, independently. Notwithstanding the way that the stage is planned for ARM-based introduced systems, our technique is general and can be associated with various sorts of structures.

KEYWORDS: Dynamic power management (DPM), peripheral power down, fault tolerance.

I. INTRODUCTION

Dynamic Voltage and Frequency Scaling (DVFS) describes the use of two power saving techniques (dynamic frequency scaling and dynamic voltage scaling) used to save power in embedded systems including cell phones. This type of power saving is different from what most of us generally think about like standby or hibernate power states. You can reduce the power consumed by your embedded system by lowering the frequency and/or voltage of the CPU and attached peripherals. Why save power? Well the obvious reason your device can run longer on a given battery. Another benefit of reducing power consumption is less heat is generated by your device; this has benefits to the mechanical design. Done well it can make the difference between needing a passive or active cooling system. If you can avoid a fan (or even reduce the fan speed) you can improve a number of things including cost per device and mean time to failure. The nice thing is hardware vendors have been adding these power saving capabilities to devices so part of the work is already done for us, we do however need to understand our systems requirements. Reducing the voltage and/or frequency does have a drawback; this is a reduction in performance. It's pretty simple, reduce voltage or frequency and your CPU processes fewer instructions in a given time. Now there's the CPU but also peripheral devices. So all of these play a part in the complete embedded system. Embedded systems are ubiquitous, and demand for these systems is growing progressively. A wide range of embedded systems are battery operated. As, for many of these systems, there is no possibility of frequently charging or replacing their batteries, they are highly energy constrained [1]–[3]. Therefore, for these systems, low energy consumption has become one of the major design objectives. Examples include mobile robots and handheld devices such as personal digital assistants, cell phones, and portable medical care devices. Furthermore, the complexity of embedded systems is increasing as the number of parts

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and the number and types of interactions among them are increasing [3], [4]. Therefore, embedded system designers are always conducted at the request of designing complex embedded systems with several design objectives. In dealing with today's highly competitive embedded systems markets and time-to-market pressure and in order to deliver correct-the-first-time products with multiple system requirements, the use of commercial off-the-shelf (COTS) devices [3], [5]–[7] is very beneficial in designing embedded systems. However, instead of focusing on embedded systems, these platforms allow to functionally test the SOC or ASIC devices to be produced. Reference [23] has presented a platform for dynamic voltage and frequency scaling (DVFS) [11] in an ARM-based processor. However, this work exploits DVFS only for the processor (and not for the other parts, e.g., phase-locked loop (PLL), memory, and I/O).

There are the five observations.

- 1) The high-to-low voltage scaling delay is greater than the low-to-high delay (about 45% for the processor core and PLL and about 110% for memory and I/O).**
- 2) Voltage and frequency scaling is very effective in reducing power consumption not only for the processor core but also for the other parts of the microcontroller, including PLL, memory, and I/O.**
- 3) Although PLL, memory, and I/O have less power consumption compared with the processor core, they have comparable energy consumption to that of the core.**
- 4) Although PLL has a very small contribution in the total power consumption, as it is always operational, its energy consumption is comparable with that of the others.**
- 5) Applying DVFS on the whole microcontroller results in a considerable energy savings compared with the sole use of DPM or applying DVFS only on the processor core.**

II. RELATED WORK

Low power and world class are most indispensable objectives of embedded system plots. Furthermore, low power incorporates lower cost of operation of contraction and more diminutive battery size to make structure more flexible. As, for a significant part of these structures, there is no likelihood of occasionally charging or supplanting their batteries, they are exceedingly essentialness constrained [1],[2],[4]. Most of the introduced things are battery worked, including reduced data terminals handheld gaming bolsters, trades issue ranges, battery-supported home, splendid presentations and various more [1]. Today's introduced structures deal with a perfect chance to-business area weight, endeavor to pass on right the-principal gone through things with various system requirements, the use of business off-the-rack (COTS) contraptions [1] is amazingly useful in sketching out embedded structures. There are in like manner reconfigurable gear answers for engage the framework methodology and offer an alternate programmable basis contraptions (PLD) - based evaluation pack [1][9] (eg Xilinx). As these stages licenses value test of the SOC or ASIC contraptions, however doesn't focus on embedded system. Reconfigurable hardware course of action, for instance, Xilinx, these stages don't offer workplaces to trial imperativeness organization strategies. Embedded structures include the amount of microcontrollers. Microcontroller includes inbuilt processor focus joined with memories and distinctive peripherals in a singular chip [1],[5],[8]. Some lab tests have been performed on microcontroller based stages in reference [6]. In reference [5] a prototyping stages for ARM based introduced system has completed. Regardless, these stages don't outfit experimentation with power organization systems. In this paper, we are proposing a gear stage for investigating distinctive boulevards with respect to low power and adjustment to inward disappointment in perspective of two ARM microcontrollers. In overseeing low-control systems, selecting particular embedded structure criteria is crucial. Execution of these systems should have the targets as structure is hard-nonstop or fragile continuous and high steadfast quality. This is a general thought; we need to change this thought with particular application. DVFS and DPM are the most surely understood technique are used for power organization [1][3]. In any case, there are insults of both of these techniques if not associated it on right application. Considering an application is hard consistent application, if we apply DPM procedure on this system, then structure will require some speculation to start from unmoving mode to element mode. DVFS technique is proper for this system as it adjusts its voltage and repeat as per the given workload of the system. Not in any way like with the fragile consistent structure, DPM is more proper. Dynamic voltage scaling (DVS) has negative impact on the structure reliability [3]. Most of the techniques are simply associated with the processor focus, here we are applying these methodologies on both processor focus and peripherals.

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III. HARDWARE PLATFORM DESIGN

The microcontroller is composed of an ARM7 processor core, a system controller, memory elements, and peripheral devices. It is noteworthy that the computational power of ARM7 is quite sufficient for the majority of embedded applications. For example, ARM7 can easily execute all benchmarks in MiBench benchmark suite. When you are looking for the right embedded processors, with the FutureElectronics.com parametric search, you can filter the results by various attributes: by Clock Frequency 16 Hz, 200 MHz, 266 MHz, 400 MHz, RAM size 512 B, 4 kB, 32kB, 64 k, Data Bus Width from 16 b to 32 b. ARM7 can also execute fairly complex operating systems e.g., Real-Time Executive for Multiprocessor Systems RTEMS and Keil RTX. Nevertheless, for highly computation-intensive applications, the performance of ARM7 might not be adequate. In this case, it should be noted that our proposed platform is not inherently dependent on ARM7. Most I/O lines of the peripherals are multiplexed with the parallel I/O (PIO) controller. Each PIO line may be assigned to a peripheral or used as general purpose I/O. These features provide flexibility to designers and assure effective use of the components.

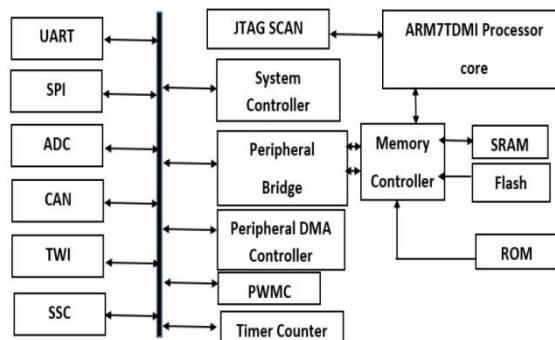


Fig 01. ARM-7 based microcontroller architecture.

A. COTS DEVICES ON EMBEDDED SYSTEM

A COTS item is normally a PC equipment or programming item customized for particular uses and made accessible to the overall population. Such items are intended to be promptly accessible and easy to understand. A run of the mill case of a COTS item is Microsoft Office or antivirus programming. A COTS item is for the most part any item accessible off-the-rack and not requiring custom advancement before establishment.

IV. PROPOSED SYSTEM MECHANISM

The point is to outline complex inserted frameworks while lessening the advancement time and cost, there is an extraordinary propensity to utilize business off-the-rack ("COTS") gadgets ECG is given as the information. Here, a simple to-execute COTS-based assessment stage for low-vitality installed frameworks is exhibited. To accomplish vitality sparing, DVFS is accommodated the entire microcontroller. Likewise, offices are given to trying different things with adaptation to internal failure methods. The stage is outfitted with vitality estimation and investigating gear. Physical investigations demonstrate that applying DVFS all in all microcontroller gives up to 47% and 12% vitality sparing contrasted and the sole utilization of element force administration and applying DVFS just on the center, separately. In managing today's exceptionally focused installed frameworks markets and time-to-business sector weight and so as to convey right the-first-run through items with different framework prerequisites, the utilization of business off-the-rack (COTS) gadget is extremely gainful in planning inserted frameworks. A few merchants offer reconfigurable equipment answers for quicken the configuration procedure and give an assortment of programmable rationale gadget (PLD)- based assessment packs. In any case, rather than centering inserted frameworks, these stages

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permit to practically test the SOC or ASIC gadgets to be created. It gives DVFS ability to the microcontrollers, including the processor centers as well as PLL, memory, and I/O Memory and I/O is entirely successful incorporates hardware too precisely and independently measure vitality/power utilization. It taking into account an ARM-based COTS microcontroller; thus, it can be utilized for an extensive variety of existing microcontroller.

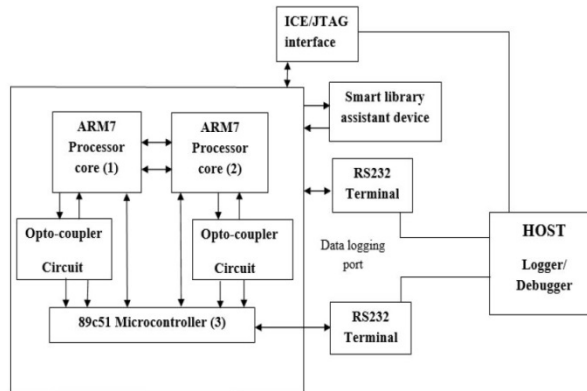


Figure. No 02. Hardware platform block diagram

V. POWER MANAGEMENT TECHNIQUES

Dynamic Voltage and Frequency Scaling (DVFS) describes the use of two power saving techniques (dynamic frequency scaling and dynamic voltage scaling) used to save power in embedded systems including cell phones. This type of power saving is different from what most of us generally think about like standby or hibernate power states. All of these are useful of course. You can reduce the power consumed by your embedded system by lowering the frequency and or voltage of the CPU and attached peripherals. This can be done by using several voltage and frequency scaling techniques.

1. DPM

DPM usually has only two operational states for systems components, namely active and idle. The active power consumption of a clock-enable component can be determined by its operating frequency and supply voltage, as denoted by P_{Active}.

$$P_{Active} = I_{Leakage}V + C_{eff}V^2f \text{ ----Eqn (1)}$$

2. DVFS

The basic idea behind DVFS techniques is to determine the minimum frequency that satisfies all timing constraints and then to adjust the lowest possible voltage that allows this speed. Assuming a linear relationship between frequency and voltage the combined effects of voltage and frequency scaling result in decreasing the active power consumption proportional to V³ and reducing the energy consumption proportional.

Clock Description	Power Management Scheme
Maste Clock	Selecting a slow clock
Processor Clock	Switching off the processor in idle mode
Peripheral Clock	Individually disable the peripherals clock
USB Clock	Disabling the associated Peripherals Clock

Table. No 01. Clock Description

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Therefore, by scaling both the voltage and frequency, the energy can be significantly reduced. However, this achievement does not come for free because a tradeoff exists between speed and energy consumption. Software controlled clock generators and voltage regulators allow the system to use DVFS. This provides the possibility for the device to vary the supply voltage rather than using just a single fixed voltage. To provide voltage scaling capability for this device, the dc/dc converter and embedded voltage regulator in is replaced with a controllable power supply.

VI. OPPORTUNITIES OFFERED BY PARALLEL PROCESSING

Since the proposed platform has multiple processing units i.e., two ARM7-based and one AVR-based microcontrollers and since it has the facilities for energy power management i.e., DVFS and DPM, one advantage of the platform is that it can be used to research into the possible opportunities for energy management that may be offered by parallel processing. To give an insight into this issue, we provide an example to illustrate when DVFS is used in executing parallel tasks; a two-processor system consumes less energy as compared with a single-processor system.

VII. EXPERIMENTAL RESULTS

The LPC2148 provides two reduced power mode: idle mode and Power down mode. Power consumption of ARM processor. Selecting the operational modes. Also for 89C51 microcontroller, PCON is used for selecting modes. Peripheral power down can also be done by software method by using PCONP special function register. The power consumption increases with application as I/O pins consumes most of the power. At run time of application, power consumption observed in the system. The power consumption increases with application as I/O pins consumes maximum of the power.

VIII. CONCLUSION

A hardware stage that includes two ARM-based microcontrollers, each managed freely by variable voltages. This stage is amazingly sensible for evaluating embedded structures with low imperativeness use and adjustment to non-basic disappointment essentials. In this stage, we give DVFS ability to the whole microcontroller including the processor focus, PLL, memory, and I/O. Physical trials exhibit that applying DVFS all things considered microcontroller is amazingly more capable in reducing power/essentialness use differentiated and applying DVFS just on the processor focus or using close down methodologies that are at this moment used by most embedded processors. Physical examinations show that applying DVFS as a rule microcontroller offers up to 47% and 12% essentialness saving differentiated and the sole use of component power organization and applying DVFS just on the inside, exclusively. Likewise, the stage is outfitted with precise imperativeness/power estimation units, investigating ports, and workplaces for evaluating adjustment to non-basic disappointment strategies. Regardless of the way that the stage is proposed for ARM-based microcontrollers, it is general, and diverse COTS devices and embedded processors can be similarly used as a part of the diagram of the stage.

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