

Design and Comparison of Unsigned 16-Bit Multiplier Based On Booth-Encoder and Wallace-Tree Modifications

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ABSTRACT: The deferral of the multiplier assumes a basic part in some fast executions and processors, for example, RISC, DSP, and picture handling centers, and so forth. In this paper, an outline of unsigned 16-bit multiplier is proposed, expecting to accomplish the best planning execution with a fitting zone. The proposed design comprises of a changed Radix-4 Booth encoder, an altered Wallace Tree adder, and a Carry Look Ahead adder.

KEYWORDS: Modified Booth Encoding multiplier, Baugh-Wooley multiplier, array multiplier, CSA, CLA Partial product, Signed-unsigned.

I.INTRODUCTION

In computerized signal handling and in addition in the universal, useful rate of multiplier operation is imperative. Prior duplication actualizes by and large utilizing succession of expansion, subtraction, and movement operation. Multiplication can be considered as a progression of rehashed increases. The number to be included is the multiplicand, the quantity of times that it is included is the multiplier, and the outcome is the product. Every progression of expansion creates a fractional product. At the point when the operands are deciphered as whole numbers, the product is for the most part double the length of operands. This rehashed expansion strategy definition is moderate that it is quite often replaced by a calculation that makes utilization of positional representation. Distinctive sorts of multiplier plans have been proposed keeping in mind the goal to overcome different necessities, for example, little range, fast, or low vitality utilization, and so on. There are number of execution strategies that have been utilized with corner encoder like Wallace tree adder, Dadda tree adder, Carry-save adder, cluster multiplier, Modified Booth Encoder and so on as a rule multiplier usage separated into three stages. In the initial step, create halfway item from the multiplier to various items. In the second step of incomplete item expansion, the procedure can be portrayed as summing up all the fractional items until the last two columns. Number of methods have been introduced so as to lessen the measure of augmentations alongside accelerating the handling by parallel outlines. When every single halfway item are decreased to sum and carry words, the last step adds the last two columns to create the last result. In the event that the quantities of halfway items to be created are of short of what it is in a roundabout way implies that we have accomplished the pace in producing incomplete items Booth's calculations are implied for this as it were. The modified Booth encoding (MBE) creates an unpredictable halfway item exhibit in view of the additional fractional item bit in any event noteworthy piece position of every incomplete item push. This paper displays a straightforward way to deal with a standard multiplication procedure with less additions and unimportant overhead. Stall Wallace multiplier is equipment proficient and performs quicker than Booth's multiplier. Wallace multiplier devours 40% less power contrasted with Booth multiplier.

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II.OBJECTIVE

1. Multiplications are most broadly and all the more frequently utilized number juggling calculation executed as a part of all advanced signal processing applications. Expansion is the essential operation for some computerized applications.
2. The point is to create region effective, fast and low power gadgets. Precise operation of an advanced framework is for the most part impacted by the execution of the adders. Multipliers are additionally imperative part in computerized frameworks.
3. In this an elite and low power 16 bit unsigned multiplier is proposed utilizing Wallace tree adders.
4. Advantage of Wallace calculation is it create the two columns toward the end of few line expansion however every line expansion is minimal complex. The fundamental target is examination of execution investigation of the area, power and speed of Radix-4 Booth multiplier and Radix-4 stall wallace multiplier.

III.LITERATURE SURVEY

The postponement of the multiplier assumes a basic part in some rapid usage and processors, for example, RISC, DSP, and picture preparing centers, and so on. In [1] an outline of unsigned 32-bit multiplier is proposed, planning to accomplish the best planning execution with a fitting territory. The proposed design comprises of an altered Radix-4 Booth encoder, a changed Wallace Tree snake, and a Carry Look Ahead viper.

[2] presents the strategies required to actualize a rapid and elite parallel complex number multiplier. The plans are organized utilizing Radix-4 Modified Booth Algorithm and Wallace tree. These two methods are utilized to accelerate the duplication procedure as their capacity to decrease fractional items era and pack incomplete item term by a proportion of 3:2. Notwithstanding that, convey spare adders (CSA) is utilized to upgrade the pace of expansion procedure for the framework.

Fast and low power MAC unit is most extreme prerequisite of today's VLSI frameworks and advanced sign handling applications like FFT, Finite motivation reaction channels, convolution and so on. In [3], creators have examined diverse sorts of multipliers like stall multiplier, combinational multiplier, Wallace tree multiplier, cluster multiplier and consecutive multiplier. Every multiplier has its own particular points of interest and impediments. Distinctive sorts of strategies are exhibited for enhancing the rate and low power utilization like pipelined corner augmentation strategy in which pipelining is utilized as a part of stall multiplier to decrease the postponement of every stage.

[4] depicts usage of radix-4 Modified Booth Multiplier and this execution is contrasted and Radix-2 Booth Multiplier. Adjusted Booth's calculation utilizes both expansion and subtraction furthermore treats positive and negative operands consistently. No unique activities are required for negative numbers. [4] Investigates the technique for executing the Parallel MAC with the littlest conceivable postponement.

IV.SYSTEM ARCHITECTURE

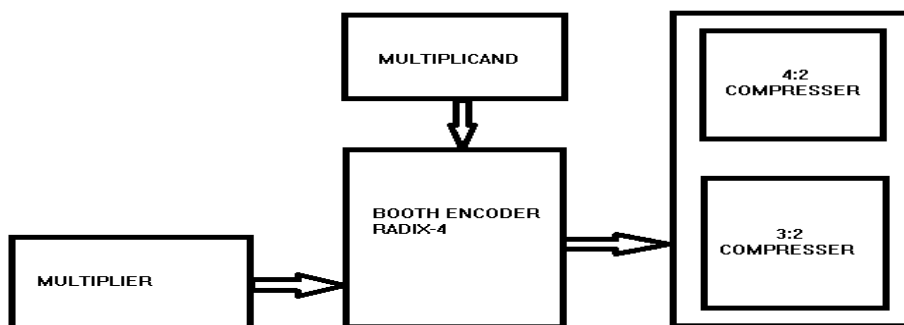


Fig 1: Proposed Architecture of Wallace tree multiplier using booth encoder

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1 Booth Encoder

Booth encoding is a technique that allows for smaller, faster multiplication circuits, by recoding the numbers that are multiplied. It is the standard technique used in chip design, and provides significant improvements over the "long multiplication" technique.

Booth multiplication algorithm gives a procedure for multiplying binary integers in signed -2's complement representation.

Following steps are used for implementing the booth algorithm:-Let X and Y are two binary numbers and having m and n numbers of bits (m and n are equal) respectively.

Step 1 Making booth table: In booth table we will take four columns one column for multiplier second for previous first LSB of multiplier and other two (U and V) for partial product accumulator (P)[3].

1. From two numbers, choose multiplier (X) and multiplicand (Y).
2. Take 2's complement of multiplicand (Y).
3. Load X value in the table.
4. Load 0 for X-1 value.
5. Load 0 in U and V which will have product of X & Y at the end of the operation.
6. Make n rows for each cycle because we are multiplying m and n bits numbers.

Step2 Booth algorithm: Booth algorithm requires examination of the multiplier bits, and shifting of the partial product (P). Prior to the shifting, the multiplicand may be added to P, subtracted from the P, or left unchanged according to the following rules:

1. $X_i X_{i-1}$
 - 0 0 Shift only
 - 1 1 Shift only
 - 0 1 Add Y to U and shift
 - 1 0 Minus Y from U and shift
 2. Take U & V together and shift arithmetic right shift which preserves the sign bit of 2's complement number. So, positive numbers and negative numbers remain positive and negative respectively.
 3. Circularly right shift X because this will prevent us from using two registers for the X value.
- Repeat the same steps until n no. of cycles are completed. In the end we get the product of X and Y.

2 Wallace Tree

A Wallacetree is an efficient hardware implementation of a digital circuit that multiplies two integers, devised by Australian Computer Scientist Chris Wallace in 1964. Wallace tree reduces the no. of partial products and use carry select adder for the addition of partial products. Wallace tree has three steps:-

1. Multiply each bit of multiplier with same bit position of multiplicand. Depending on the position of the multiplier bits generated partial products have different weights.
2. Reduce the number of partial products to two by using layers of full and half adders.
3. After second step we get two rows of sum and carry, add these rows with conventional adders.

Explanation of second step:-

As long as there are three or more rows with the same weight add a following layer:

1. Take any three rows with the same weights and input them into a full adder. The result will be an output row of the same weight i.e sum and an output row with a higher weight for each three input wires i.e carry.
2. If there are two rows of the same weight left, input them into a half adder.
3. If there is just one row left, connect it to the next layer.

V. METHODOLOGY USED

There are three steps for the computing this method. The first step of this method is to reduce the partial product. Multiplier design, for the advantage of time consuming 2-input AND gates can be used. However, the drawback is that

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the number of partial products is high, which increase significant delay in the second step. Thus, the main objective in first step is to reduce the amount of partial products.

- Radix-4 recoding of the multiplier implies a reduction in the number of digits to 7:
- To multiply X by Y using the modified Booth algorithm starts from grouping Y by three bits and encoding into one of {-2, -1, 0, 1, 2}. Table 1 shows the rules to generate the encoded signals by MBE scheme

Second Step: a tree adder is deployed to sum all the partial products. There are two common approaches with various advancements; they are Wallace Tree Adder (WTA) approach and Dadda Tree Adder (DTA) approach. The WTA-based methods are developed based on optimizing the compressor units such as 4-2 compressors and/or 5- 2 compressors while the DTA based approaches use 3-2 compressors as its basic elements. A strong advantage of WTA algorithm is that it can generate the final two rows with only few row additions. However, the complexity of each row addition is high, which leads to a high cost of timing and resources for each row-addition process. On the other hand, although each row-addition in DTA algorithm is simpler, DTA based designs have more row additions than those of the WTA based architectures.

Input Multiplier [3 bits]	Operation	Output Data		
		Partial Products	Complement carry	
000	$Y*0$	0	0	0
001	$Y*1$	Y	0	0
010	$Y*1$	Y	0	0
011	$Y*2$	$Y \ll 1$	0	0
100	$Y*(-2)$	$\sim Y \ll 1$	1	0
101	$Y*(-1)$	$\sim Y$	0	1
110	$Y*(-1)$	$\sim Y$	0	1
111	$Y*0$	0	0	0

Table 1: Truth table of MBE scheme

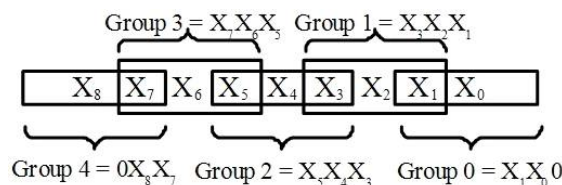


Fig 2: Bit grouping for radix-4 Booth Encoder

Modified Wallace Tree Adder:

Wallace tree adder is a technique that can sum all partial products with an advantage of processing time. From the Modified Booth Encoder in the previous step, there are partial products with their complement carry that need to be summed. Then, the process of proposed modified Wallace tree adder (MWTA) can be divided into 3 computation areas. They are signed area, MSB area, and LSB area. The signed area is the extended signed-bit of the partial products. The LSB computation area composes of LSB-bit of partial products with complement carry bits from the previous step. It can compute directly the LSB-bit of the final multiplier result during the MWTA process. Unlike the LSB computation area

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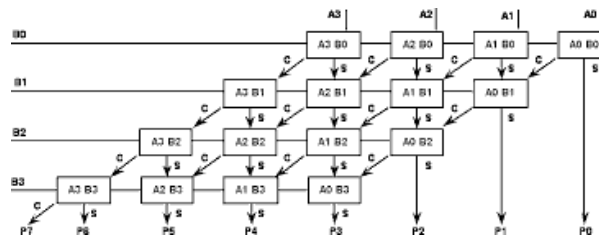
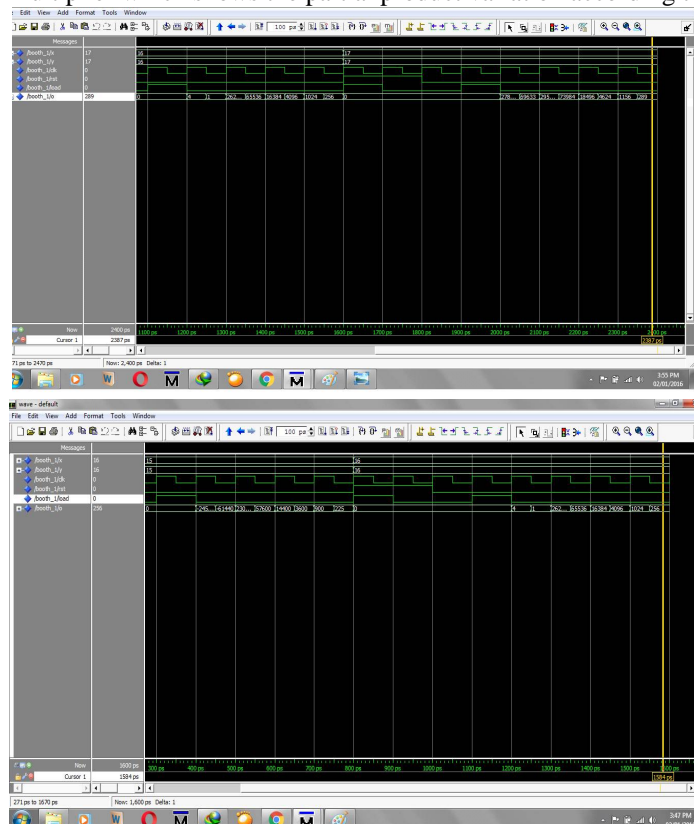


Fig 3: Wallace tree adder

Third step: In the final step, two last rows are added together to compute the final multiplier result. Many different kinds of high-speed adder have been presented such as Carry-save Adder, Carry Look Ahead Adder (CLA) , etc. However, it can be proven that there is a part of the final multiplier result can be computed at the end of each row addition processing in step 2. Therefore, the typical final step can be done during the processing of its previous step, thereby giving rises to an improvement in processing time.

VLEXPERIMENTAL RESULTS

This is waveform of booth multiplier which shows the partial product variation according to the clocks:-



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