

# Implementation of Efficient Wallace Tree Multiplier

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**ABSTRACT:** Low power consumption is an important concern for the VLSI circuit designers. Since 70% of instructions in microprocessor and most of DSP algorithms perform addition and multiplication. As a result of expanding signal processing applications, the demand of high speed multipliers is increasing. Since the common multiplication method uses shift and add algorithm, optimization of adder is required to improve the performance of multiplier. In this work, we propose a modified full adder using multiplexer to achieve low power consumption of multiplier. Designs are developed using Verilog HDL and functionalities are verified through simulation using Xilinx 14.6 and are synthesized in Cadence RTL compiler using TSMC 180nm technology.

**KEYWORDS:** Wallace tree multiplier, Full adder, Multiplexer.

## I. INTRODUCTION

Multipliers play a significant role in today's digital signal processing and other applications. High speed, low power consumption and hence delay are all the time an essential design target for any chip designer. As most of DSP structures include multipliers in their design. With the advances in technology, researchers are trying to decrease the delay of multiplier so that the delay of entire circuit can be reduced. Number of partial products to be added is the main parameter that determines the performance of multiplier. To reduce the number of partial products and achieve speed improvement, Wallace tree multiplier is the most popular technique. It involves ANDing of multiplier and multiplicand bits for the generation of partial products in the first stage. In the second stage full adders and half adders have been used for the reduction of partial products in two rows. Followed by addition of two rows using fast carry adders in the third stage.

This work mainly deals with the replacement of full adders with modified full adder in the reduction phase of the Wallace tree multiplier. In the preferred method, a modified full adder using multiplexer is useful to attain power reduction compared to the existing techniques with a small area and delay improvement.

## II. RELATED WORK

### A Typical Wallace Tree Multiplier

The Wallace tree multiplier is faster than array multipliers, since the delay in an array multiplier varies linearly, whereas in Wallace it varies logarithmically. Consider an N bits multiplication,  $N^2$  AND gates are required in order to produce the partial product terms and the number of reduction stages is given by S which is shown in (1)

$$S = \log_2 N \quad (1)$$

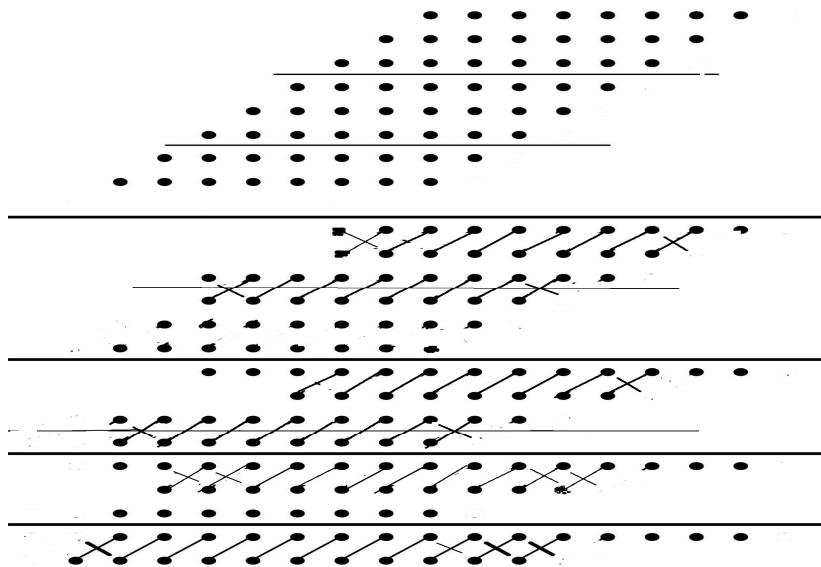


Fig1 Typical Wallace tree Multiplier

Fig1 shows 8-bit typical Wallace multiplier .It multiplies multiplicand and multiplier bits to generate the partial product in first stage.In second stage,when there are three bits,fulladders are used and for two bits ,halfadders are used.If there is any bit left in the column is passed to the next stage without processing.The final two rows are added using fast adder.

B. Using Regular Full adder

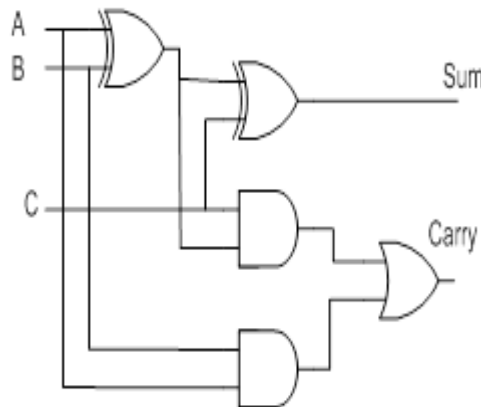


Fig 2.Regular Fulladder

Regular Wallace tree multiplier uses full adder in its reduction phase. Due to XOR gates;fulladder consumes more power. As shown in fig.2 regular full adder consists of two XOR gates in critical path of sum and one XOR gate, one AND gate and one OR gate in the critical path of the carry.Hence the critical path delay is given.

$$\text{Delay}=2*\text{xor}$$

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### C. Fulladder using two 4:1 multiplexers

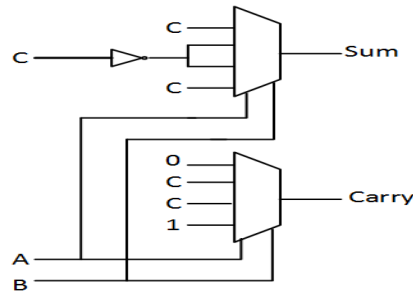


Fig.3 Fulladder using two 4:1 multiplexers

In sequence to reduce the power and area, the fulladder in reduction phase of Wallace tree multiplier is replaced by a modified full adder. In MUX based full adder, the fulladder is implemented using 4:1 multiplexers as shown in fig. 3. By implementing MUX based full adder in reduction phase of Wallace tree multiplier power reduction has been achieved. It is clear that, one 4:1 MUX can be made using three 2:1 MUX. The critical path delay can be written as shown.

$$\text{Delay} = \text{Not} + 2 * \text{Mux}$$

### D. Fulladder using six 2:1 Multiplexers

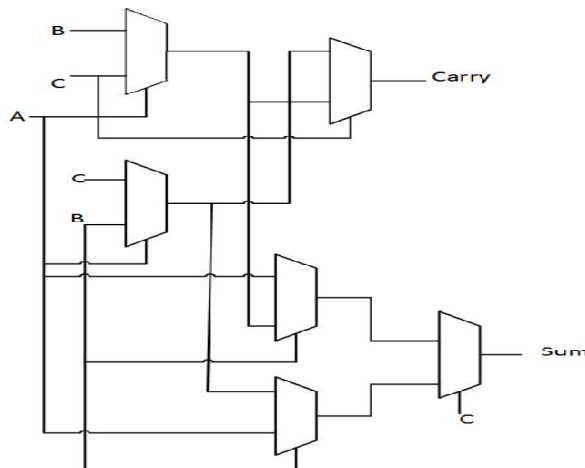


Fig.4 Fulladder using six 2:1 Multiplexers

Here, fulladder is designed using six 2:1 multiplexers. Since each multiplexer is made using six transistors, totally twelve transistors are essential for the operation of full adder circuit. Most of the power consumption in any circuit is short circuit current, leakage current and logic transition. In this circuit, there is no direct connection between vdd and vss. So, the possibility of direct path occurrence between source and ground will be avoided which results in reduction in short circuit power. In addition to that, all the internal nodes are excited by fresh inputs, switching activity will also be reduced. This causes reduction in power but at the cost of area increment. Therefore critical path delay is given by

$$\text{Delay} = 3 * \text{Mux}$$

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D Preferred Fulladder

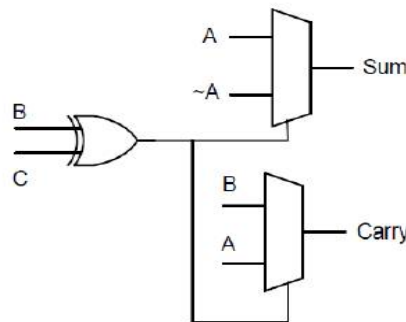


Fig.4 Preferred Fulladder

This preferred fulladder consists of two 2:1 multiplexers and xor gate. In this preferred technique, xor gate in fulladder is replaced by multiplexer block. As most of the power consumption is due to xor gates, by reducing number of xor gates, power reduction can be achieved. This modified fulladder will be applied to Wallace multiplier

$$\begin{aligned}
 Sum &= A \oplus B \oplus C \\
 &= (A \oplus B) \oplus C \\
 &= (\overline{AB} + A\overline{B}) \oplus C \\
 &= (\overline{AB} + A\overline{B})C + (\overline{AB} + A\overline{B})\overline{C} \\
 &= (\overline{AB} + A\overline{B})C + (\overline{AB} + A\overline{B})\overline{C} \\
 &= \overline{A}BC + ABC + \overline{A}B\overline{C} + A\overline{B}\overline{C} \\
 &= A(\overline{B}C + \overline{B}\overline{C}) + \overline{A}(\overline{B}C + B\overline{C}) \\
 &= (\overline{B} \oplus \overline{C})A + (B \oplus C)\overline{A}
 \end{aligned}$$

This modified expression for sum can be implemented by using first multiplexer and xor gate.

$$\begin{aligned}
 Carry &= AB + BC + CA \\
 &= C(B + A) + AB \\
 &= C(B + A)(B + \overline{B}) + AB \\
 &= C(B + A\overline{B}) + AB \\
 &= BC + A\overline{B}C + AB \\
 &= B(C + A) + A\overline{B}C \\
 &= B(C + A)(C + \overline{C}) + A\overline{B}C \\
 &= B(C + A\overline{C}) + A\overline{B}C \\
 &= BC + A\overline{C}B + A\overline{B}C \\
 &= BC(B + \overline{B})(C + \overline{C}) + A\overline{C}B + A\overline{B}C \\
 &= B(\overline{B}C + BC) + A(\overline{B}C + \overline{B}C) \\
 &= B(\overline{B} \oplus C) + A(B \oplus C)
 \end{aligned}$$

Similarly, modified expression for carry can be implemented by using second multiplexer with xor output as select line.

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In Wallace multiplier structure, partial products are divided into definite stages. In each stage, whenever there are three bits, full adder has to be used. Out of the three inputs, one input and its complement are given as inputs to the first multiplexer. The other two will be given as input to xor gate, output of which will as select line for both the multiplexers. The bits other than carry bit are used inputs to the second multiplexer. This results in reduction in switching activity and also critical path delay compared to existing techniques.

Function of this modified fulladder as follows:

- a) If both B and C are zero or one,  $sum=A$ .
- b) If either of B or C is one and another is zero,  $sum= \bar{A}$ .
- c) If either of B or C is one and another is zero,  $carry=A$ .
- d) If both B and C are zero or one,  $carry= B$ .

### III. EXPERIMENTAL RESULTS

Here, Wallace multiplier designs are developed using verilog HDL for 8 and 16bits and are verified through simulations using Xilinx ISE. The simulation waveforms of Wallace multiplier using modified fulladder for both 8 and 16bit are shown in Figures 5,6. And these multiplier designs are synthesized in cadence RTL compiler using TSMC 180nm technology.

Simulation waveforms

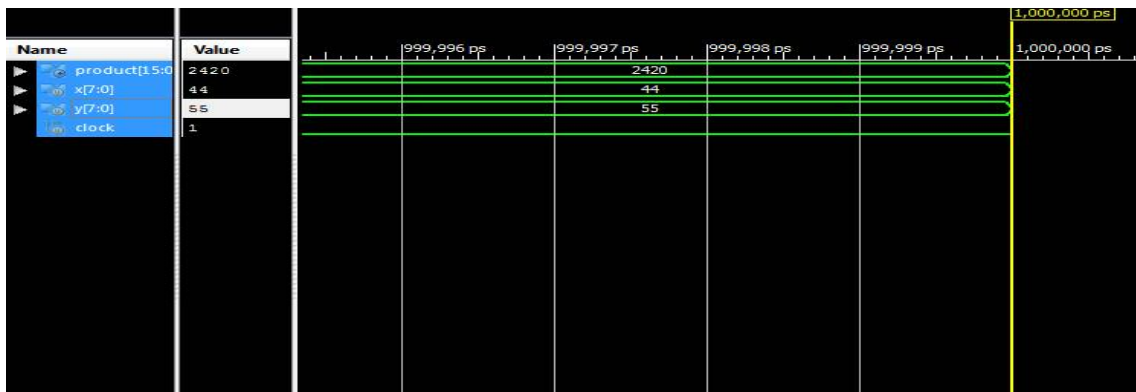


Fig5 :Simulation waveform for 8bit Preferred Fulladder Wallace multiplier



Fig 6:Simulation waveform for 16bit preferred fulladder wallacemultiplier

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Wallace multiplier using	Number of bits	Area( $\mu\text{m}^2$ )	Power(mw)	Delay(ns)
Regular Fulladder	8	69346.41	3.02051448	5
	16	283350.94	21.97437230	8.7
Fulladder using 2 4:1 Multiplexers	8	49704	4.17298814	1.2
	16	1765723.77	129.5553635	21.1
Fulladder using 6 2:1 Multiplexers	8	88056	9.05169993	8.8
	16	385184	74.94016739	11.7
Preferred Fulladder	8	38681.13	1.89007009	0.4
	16	137201.51	8.19221088	1.7

Table 1: Comparison based on area, power and delay

## IV. CONCLUSION

By including modified fulladder in reduction stage of Wallace multiplier, an average area, power and delay reduction will be obtained. The synthesis results show that the preferred wallace multiplier is suitable for low power and small area applications.

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