

# Modeling and Control of Multilevel Inverter with Reduced Number of Power Switches

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**ABSTRACT:** Multilevel inverters (MLI) are mostly used medium-voltage and high-power applications due to attractive features such as low total harmonic distortion (THD) in output voltage, high efficiency, less stress on power switches and low Electromagnetic Interference (EMI). But multilevel inverter requires more number of power semiconductor switches as number of levels increase that increases cost and complexity in control circuit. In this paper, a study of new structure of MLI that uses reduced number of switches as compared to conventional MLI topology is performed. The new MLI structure reduces overall loss, cost and size as compared to conventional MLI. The three phase MLI topology with reduced number of switches is simulated using MATLAB/Simulink. The switching signals are generated using In Phase Disposition carrier based modulation technique for the new MLI. The effectiveness of the three-phase MLI topology has been demonstrated through simulation results.

**KEYWORDS:** Multilevel Inverters (MLI), Circuit topology, Sinusoidal Pulse-Width Modulation, Cascaded H-bridge MLI

## I. INTRODUCTION

Multilevel inverters have drawn more attention due to ability to perform better in medium-voltage high-power applications in recent years. It can provide higher output voltage closer to sinusoidal voltage waveform with lower voltage stress on the power switches. It is also possible to control lower order harmonics by using different modulation techniques [1].

Various types of multilevel inverters are used, but most commonly used are Cascaded H-bridge (CHB) MLI, Flying Capacitors (FC) and Neutral Point Clamped (NPC). They are popular due to their modular structure and ability to generate quality sine wave in output voltage [1]. In comparison with the conventional voltage source inverter, MLI gives lower Total Harmonic Distortion (THD) because of stepped output voltage waveform. The only limiting factor in using MLI is the increase in number of power switches with voltage. Hence, optimal use of switches and reduction of required number of switches have been major area of interest for the research. Another important aspect is to control the MLI. The control strategies based on different multi-carrier modulation techniques are presented in [2-3].

Many topologies that uses less number of switches compared to conventional multilevel topology, have been presented [4-7]. These topologies reduced losses of the inverter for given number of output voltage level.

**J.Rodriguez, J.S. Lai, F.Z.Peng** [1] presents most commonly used topologies like Cascaded H-bridge (CHB), Neutral Point Clamped (NPC) and Flying Capacitor (FC). Other advanced topologies like asymmetric hybrid cells and soft-switched multilevel inverters are discussed. Various modulation techniques like multilevel sinusoidal pulse width modulation, selective harmonic elimination, space vector modulation.

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**Bin Wu [2]** presents basic MLI topologies as well as their control strategies based on different carrier based PWM and Space vector modulation technique.

**L.M. Tolbert, T.G. Habetler[3]** suggests novel carrier-based multilevel PWM schemes which take advantage of special properties available in multilevel inverters to minimize switch utilization. In traditional sub harmonics (SH) modulation and switching frequency optimal (SFO) PWM, the top and bottom switches are switched more often than the intermediate device. A novel method for diode clamped inverter has been demonstrated for SH-PWM and SFO-PWM by varying frequency for the different triangular wave carrier band.

**R.A.Ahmed, S. Mekhief and H.W.Ping [4]**discusses symmetrical and asymmetrical multilevel inverter. Both inverters are very efficient to improve quality of output voltage. Structure of MLI, switching strategies and operating principle of proposed topology are explained. Advantages of using this topology are less number of switches, losses and cost. Only one DC source and two switches are to be added to increase voltage level. The number of output voltage steps in symmetric multilevel inverter is,

$$N_{step} = 2n + 1 \tag{1}$$

Where n is number of DC voltage source.

Fig.1 shows basic structure of symmetrical multilevel inverter [4]. Additional module is added for increasing voltage levels. Each module consists of DC source and two power switches.

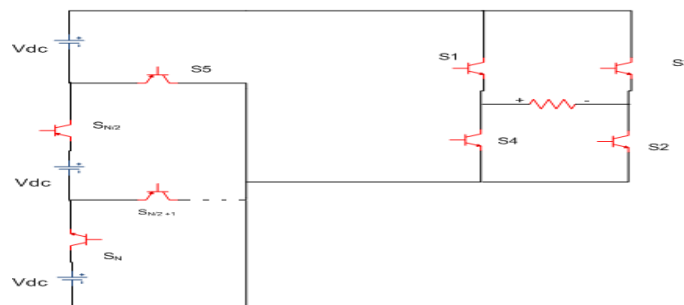


Fig.1 shows basic structure of symmetrical multilevel inverter. [4]

**H.Karaca[5]** presented a new multilevel inverter topology with the reduced number of switches and modulation strategy. This topology consists of level module which is made up of only one DC voltage source and bidirectional switch. This structure uses (m+2) switches and (m-1)/2 DC voltage source to produce m number of voltage level. level module is able to conduct voltage and to block current in both directions. This topology can be shown in Fig.2 [5].

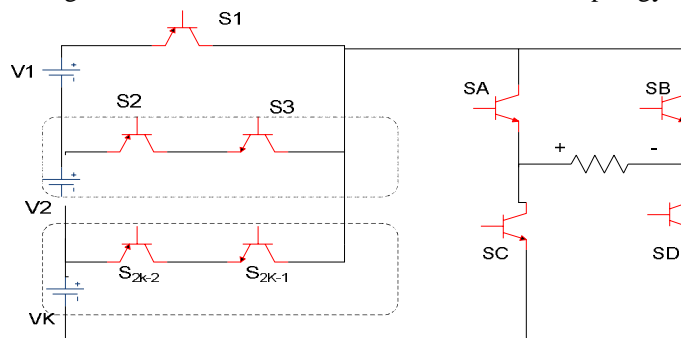


Fig.2 Multilevel inverter with reduced number of switches [5]

**J. James, Vijaykumar D., A. Kirubakaran, S. Umashankar [6]** demonstrated new H-bridge multilevel inverter topology with reduced number of switches. It consists of smaller number of multilevel inverter block connected in series. Fig.3 shows multilevel inverter with reduced number of switches for seven level output.

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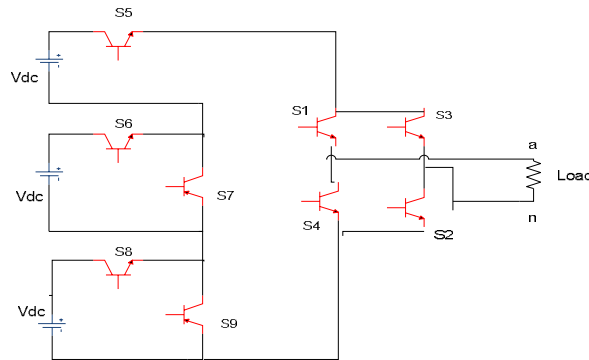


Fig.3 Multilevel inverter with reduced number of switches [6]

**E.Babaei, S.Laali, Z.Bayat** [7] suggested single phase cascaded multilevel inverter, which is consists of series connection of basic units. It is capable to generate only positive levels in output. Different four algorithms are developed to produce even as well odd magnitude of DC voltage at output. Fig.4 shows proposed basic unit which consists of three DC voltage sources and five unidirectional power switches [7]. A new single cascaded multilevel inverter which is comprised of series connection of basic unit is discussed.

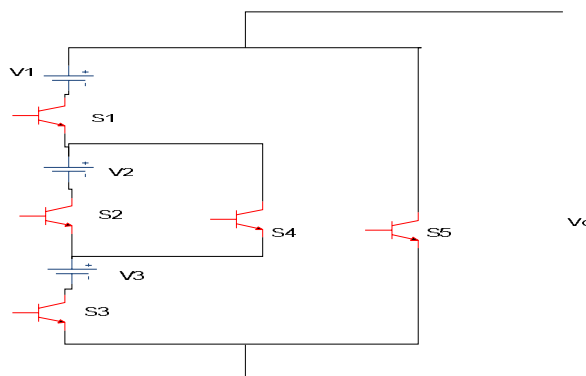


Fig.4 Basic unit of MLI presented in [7]

Based on the study of different MLI topologies [4-7], a new multilevel inverter with reduced number of switches is demonstrated in this paper. The simulation model of the topology is developed using MATLAB/Simulink. The performance of the MLI is analysed using level shifted multicarrier PWM control strategy. The comparative analysis of the MLI topology with conventional H-bridge topologies is presented.

## II. MULTILEVEL INVERTER TOPOLOGY WITH REDUCED NUMBER OF SWITCHES

In most of the MLI topologies, power electronic devices depend upon the voltage level. As voltage level increases, number of power semiconductor switches also increases. It further increases cost, size and complexity in control. To obtain higher voltage level with reduced number of switches, new multilevel inverter topology with reduced number of switches is presented in this paper. Fig.5 shows the structure of three phase five level multilevel inverter with reduced number of switches.

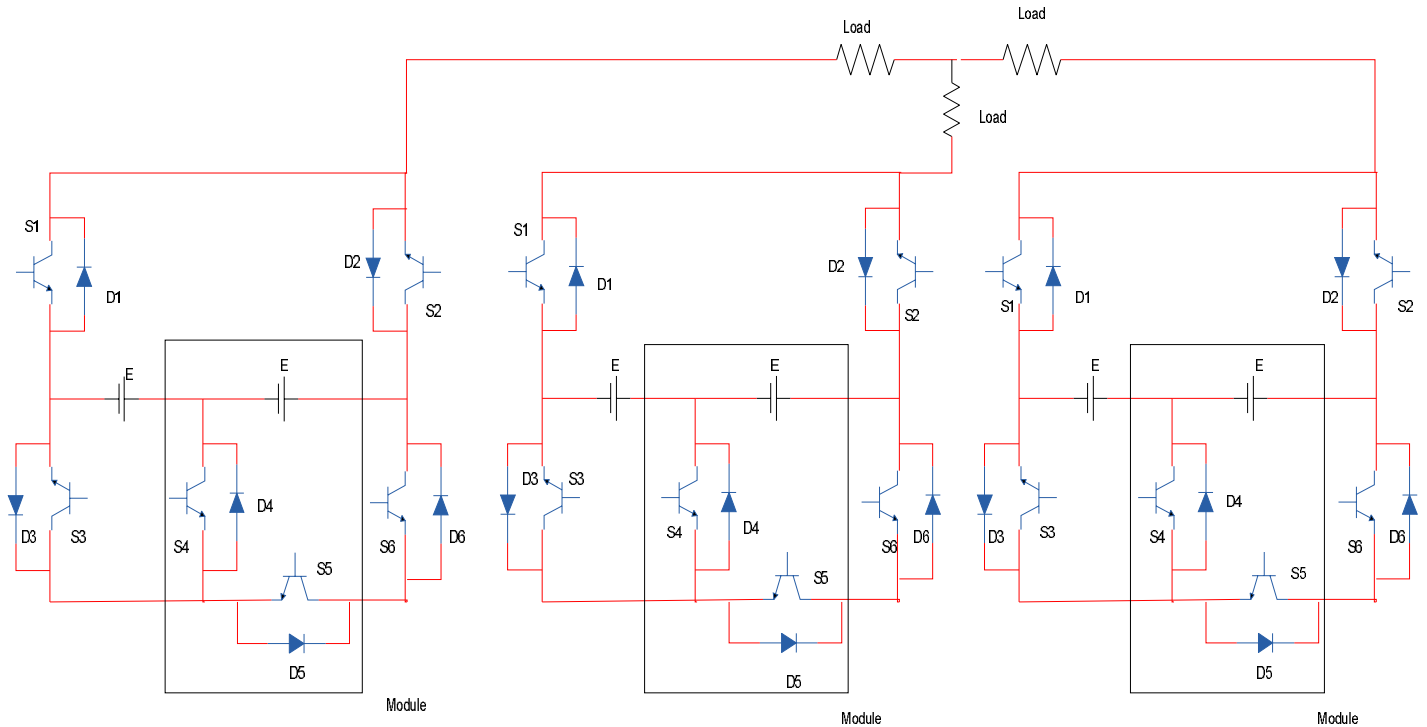


Fig.5 Three-Phase Five level inverter topology with reduced number of switches

The simplified structure of five-level inverter topology for single phase is shown in Fig.6. By using one module as shown in Fig. 6, five levels  $+2E, +E, 0, -E, -2E$  can be obtained. The structure makes use of  $(m-1)/2$  DC voltage sources to produce  $m$  voltage levels. The switching pattern for obtaining five levels is shown in Table 1.

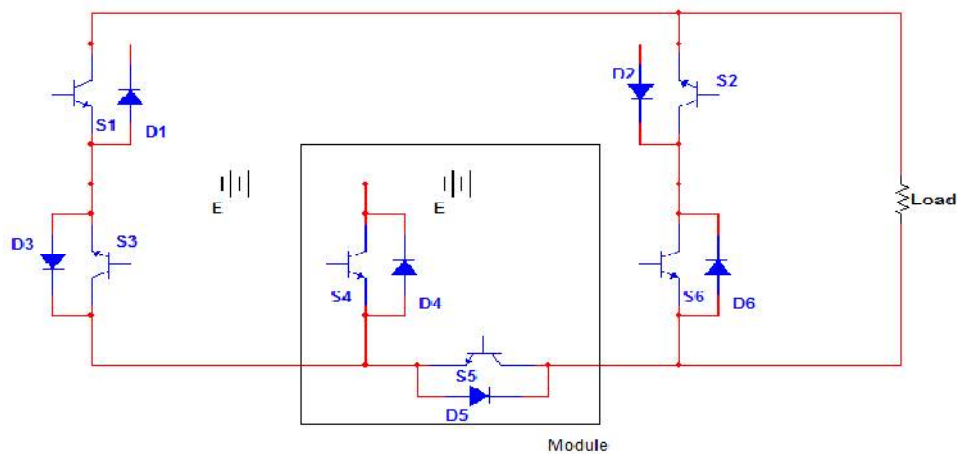


Fig.6 Single phase structure of Multilevel Inverter topology for five levels

For the voltage level  $+E$  and  $-E$ , diodes  $D4$  and  $D5$  conducts. Thus these diodes work as freewheeling diodes and it also carries load currents. By increasing number of module in structure as shown in Fig.6, more level in output voltage

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(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 5, May 2016

can be obtained. As number of module is increased, where the module consists of two switches and one DC source, two additional levels in the output voltage of the inverter are obtained with each additional module.

Table 1 Output voltage and switching states of MLI topology

Sr. No.	Voltage Level	Switches (1=ON, 0=OFF)						Conducting Diodes
		S <sub>1</sub>	S <sub>2</sub>	S <sub>3</sub>	S <sub>4</sub>	S <sub>5</sub>	S <sub>6</sub>	
1	+2E	0	1	1	0	1	0	-
2	+E	0	1	0	0	1	0	D <sub>4</sub>
3	0	0	1	0	0	0	1	-
4	-E	1	0	0	1	0	0	D <sub>5</sub>
5	-2E	1	0	0	0	0	1	-

### III. PWM SIGNAL GENERATION FOR NEW MLI SWITCHES

For switching the MLI inverter, level shifted multicarrier modulation technique is used. For five level inverter, four triangular carrier waves are used. These carriers are compared with reference sinusoidal wave. For three phase inverter, reference sinusoidal wave is 120° apart from each other. Four signals are obtained from the comparison of reference sine wave with level shifted triangular carrier waves as shown in Fig. 7. Using these four signals, gate signals are generated for six switches as per the logic shown in Fig. 7 by using OR gates. Voltage and current measured across load using SCOPE. The Total harmonic Distortion (THD) factor is analysed by FFT analysis.

The Simulink block diagram for obtaining gate signals for six switches are shown in Fig.7.

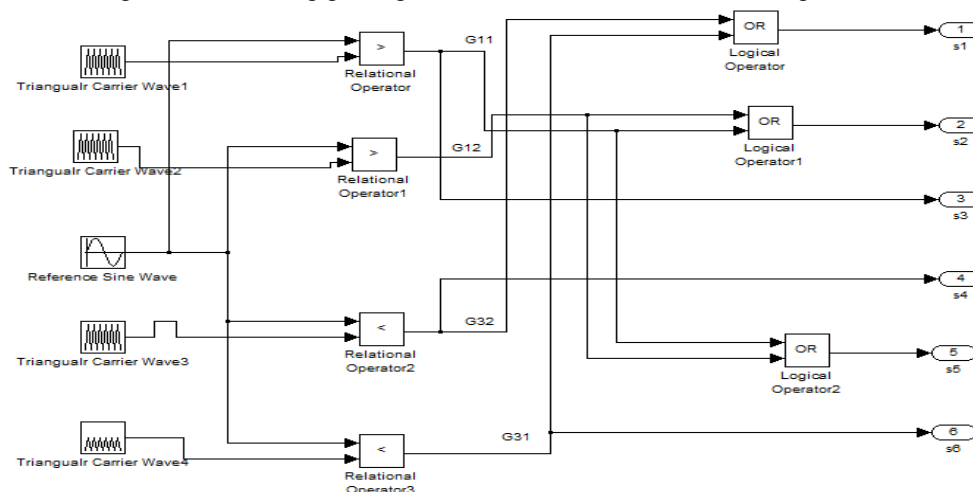


Fig.7 Simulink block diagram for switching signal generation

# International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 5, May 2016

The comparison of number of switches used in conventional H-bridge and novel topology for different levels is shown in Table 2.

Table 2 Switches used for different levels in output voltages

No. of voltage levels	Cascaded H-bridge MLI		Novel Topology	
	3-phase	No. of switches in conduction	3-phase	No. of switches in conduction
	No. of switches		No. of switches	
	$6*(m-1)$		$3*(m+1)$	
5	24	12	18	9
7	36	18	24	12
9	48	24	30	15

From the comparison, it can be seen that for three phase 9-level  $(48-30)=18$  switches can be saved. For producing  $m$  level in output voltage waveform,  $(m-3)$  switches can be reduced as compared to conventional multilevel inverter. Number of switches taking part in conduction also reduces. Reducing number of switches also reduces losses and significant saving in cost.

## IV. SIMULATION RESULTS

The novel topology for three phase five level MLI has been simulated with R load using MATLAB/Simulink by level shifted multicarrier modulation technique as shown in Fig.8.

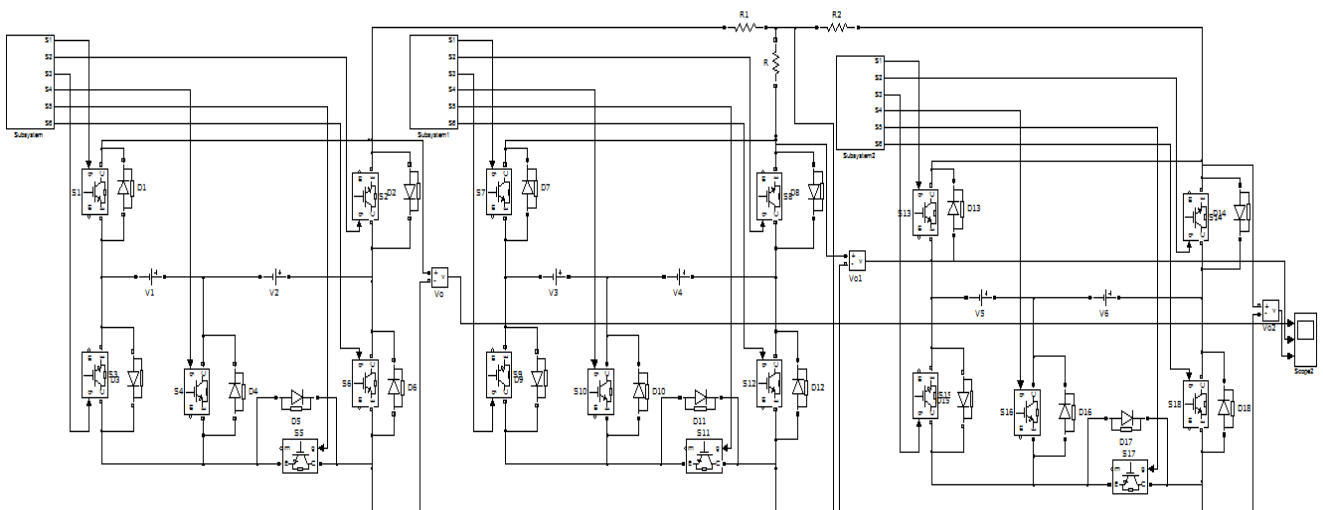


Fig. 8 Simulation model of new MLI with reduced number of switches

The parameters used in simulation for the developed MLI with reduced number of switches are as follow:

- DC voltage source  $E=100$  V
- Resistance of load  $=12 \Omega$
- Inductance of load  $=1$  mH

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Fundamental Frequency = 50 Hz  
Carrier frequency = 750 Hz  
Frequency Modulation Index ( $m_f$ ) = 15  
Amplitude modulation index ( $m_a$ ) = 0.9

The phase output voltage with five levels using In Phase Disposition (IPD) technique with R load is shown in Fig.9.

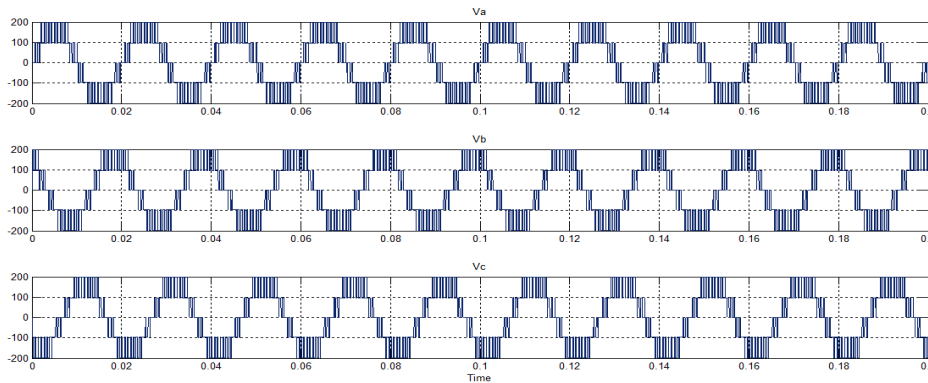


Fig.9 Five-level three phase output voltage with R load

The FFT analysis has been performed in MATLAB for five level output voltage. The Total Harmonic Distortion (THD) is 29.08% as seen in Fig.10.

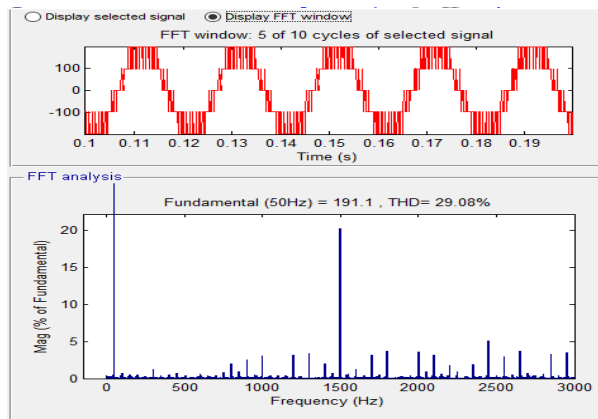


Fig.10 FFT analysis of output voltage

The phase output voltage with five levels using In Phase Disposition (IPD) technique with R-L load is shown in Fig.11

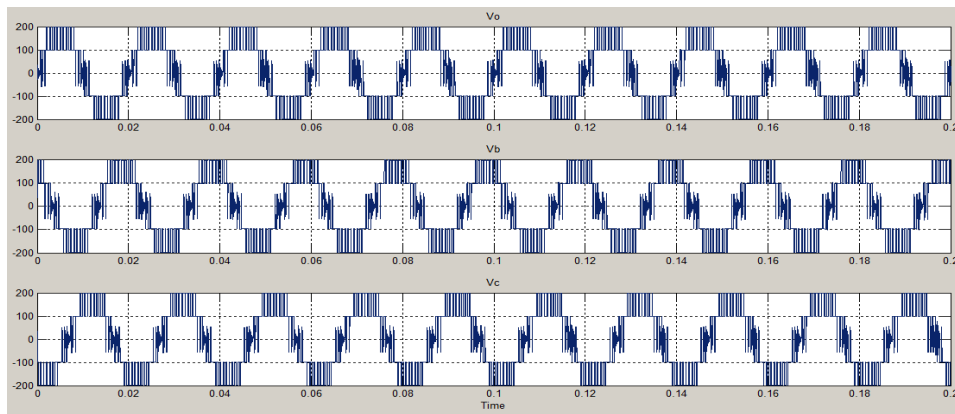


Fig. 11 Five-level three phase output voltage with R-L load

## V. CONCLUSIONS

In this paper, a new multilevel inverter topology with reduced number of switches is presented. A new multilevel topology is developed without using any transformer and capacitors. Hence, it reduces cost, size and losses. Also the structure is modular in which the voltage levels can be easily increased by adding the modules. The comparison of new MLI with conventional Cascaded H-bridge MLI shows reduction in number of switches as the output voltage level increases. With reduction in number of switches, losses can be reduced as well as considering bulk production of units, significant saving can be achieved. The MLI is simulated using level shifted In Phase Disposition multicarrier modulation technique in MATLAB/Simulink and the results validate the new MLI topology.

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