

Implementation of LCD controller IP core on FPGA

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ABSTRACT: As of late, the machines and supplies should be created with fast and light weight to secure business sector in this present competitive world. The development of the implant frameworks of today's commercial enterprises requires the utilization of a display unit, to show the aftereffects of any procedure continuously. The utilization of a LCD board with realistic presentation fills the need viably. These LCD boards require a framework to control the display on it. In this paper, a basic, adaptable and more modern LCD controller is outlined as an delicate IP core for showing the RGB pictures. Likewise, with a specific end goal to aggressively take an interest for the expected changes in item request, mechanical creation machines must be profoundly adaptable and FPGA's are exceptionally suited for satisfying those necessities. Interfacing the LCD boards in parallel to the controller compost, expands the pace. A test on LCD display is performed to check if the controller which is produced is aiding in showing a RGB picture.

KEYWORDS: LCD Controller, Soft IP core, TFT LCD panel, Verilog, Synchronization Signals

I. INTRODUCTION

The improvements in inserted framework innovation has lead to the utilization of more electronic terminals, for example, cell phones, auto route framework and numerous hand held gadgets with LCD show embraced in them. Advanced presentation application has spread to wide zones of medical gadgets, process control, camera, E-book, cars and numerous other. It's nearness gives the client with graphical data and visual impacts. Presentations can trade the paper for future. Display of pictures or messages get more consideration than verbal voice while doing presentation.[1]

The rapid increase in colour graphics in embedded applications has lead to wide accessibility of practical boards extending in thickness from a couple of thousand pixels to a huge number of pixels. The boards are made utilizing a variety of the understood LCD innovation. LCD can be ordered into 2 sorts; Transmissive LCD and Reflective LCD. In transmissive LCD, initiated cells seemed dull while the dormant seemed bright. It was enlightened from one side and saw on the other side. A light is important to enlighten LCD. Reflective LCD's have lower contrast than the previous. It is generally seen by surrounding light reflected in a mirror behind the display. These are regularly utilized as a part of pocket calculator and computerized watches.[2] There must be a gadget to control the display and for this display controllers are to be manufactured.

Display controller controls the display on the display unit. They provide timing and data signals and thereby control the format on the screen. To put up for varying applications, display controller must be flexible enough to augment its applicability and reusability. These can be developed as IP cores on FPGA.

IP core is a reusable unit of logic, cell, or chip layout design that is the intellectual property of one party. They can be used as a building blocks within ASIC chip or FPGA logic designs. In the electronic design industry, they have a profound impact on the design of system on a chip. The types of IP cores are hard IP, soft IP and a firm IP. Hard IP cores are the physical manifestation of the IP design. They are the best for plug-and-play application, and are less portable. Like hard cores, firm cores also carry placement data but are configurable to various application. Soft IP cores are the synthesizable RTL. It is the most flexible one because it exists either as a netlist or as a hardware description language (HDL) code.

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FPGA's are a semiconductor device which can be programmed outside the semiconductor foundry. They contain programmable logic components called "logic blocks" and programmable interconnects. These logic blocks can be programmed to perform function of basic logic gates or more complex combinational functions or simple mathematical functions. They are the reconfigurable devices, generally favoured in prototype building as changes can be made whenever necessary.[3]

The main aim of the project is to design and develop an LCD controller suitable for displaying an RGB image on the 320 x 240 pixel WF35LTIACDNNZ# screen. The main requirement to achieve the above is to first synchronize the clock frequency of the LCD panel with the frequency of the FPGA board, which is to be interfaced and then generate the synchronization signals (horizontal and vertical) necessary for scanning the entire screen of resolution 320 x 240. At last, RGB data extracted from the image is stored in the memory and displayed on the screen.

II. RELATED WORK

A survey on implementation of LCD controller IP core has lead to many observations. It was identified that there are 2 methods of connecting a display . One is video graphics array (VGA) and the other is digital video interface (DVI). VGA was used for cathode ray tube (CRT) displays while DVI was used for LCD display since data is digital at the origin and at the destination. In earlier days, VGA were used to connect even LCD's which required the conversion of data into analog at both source and destination. This was surmounted by the advent of DVI.

In [4], Radi et al. present the design of VGA controller using verilog HDL. They have used cathode ray tube display panel and displayed an RGB image. First they have abstracted an image file in bitmap format using MATLAB and rearranged using Microsoft Excel. The rearranged data are then stored in a MIF file created by using Altera Quartus II compiler software. After that , a VGA controller program written in Verilog HDL using Altera Quartus II compiler software, which will compile, run and simulate the written program. Once the simulation is completed successfully, the program will be burnt into Altera DE2-115 board, which will process the VGA controller program and display the image.

In [5] the geometric shapes with motion is displayed. Design consisted of five blocks namely signal generator, address generator, shape generator, motion controller and generator. Instead of displaying a stored image, geometric shapes are drawn by the shape generator block. The stored row address and column address are given as input to the shape generator. In this module all possible geometric shapes can be coded. The motion controller output is taken as input to shape generator. This uses FSM where the motion for the objects implemented can be generated. Display on the screen is controlled by the Hsync and Vsync signals by the shape generator block. The design was observed and verified in Cadence tool, as a result internal power, switching power and leakage power was observed.

In [6], an efficient hardware architecture for VGA controller which has a high potential to be used in Altera FPGA based system has been designed. The design was validated through real time application demonstrations. Here both image and text character were displayed simultaneously, without using any external RAM memory. The use of on-chip embedded array memory helped to display the features of both image and character on the monitor with resolution of 640 x 480.

A design of a prototype where UART was interfaced with LCD display through FPGA board was proposed in [7] so as to provide flexibility of data which is being displayed directly to LCD. Their main intension was to provide serial communication of keyboard character using USART hyper terminal and display it on HD44780 based LCD controller. For multi UART, two modules were included; configurable baud rate and receiver. For an LCD controller a simple FSM was devised to create a simple controller within the FPGA to output text onto the HD44780 based text LCD. This prototype was tested on cyclone II DEI FPGA board.

III. DESIGN OF LCD CONTROLLER

The LCD controller is designed with a goal to make it suitable for displaying an RGB image on the screen of 320 x 240 pixel WF35LTIACDNNZ# TFT LCD display. It has the capability of displaying graphics with 24 bit RGB (8-8-8) support. This display module is chosen for testing the LCD controller that is proposed in this paper.

A. Block Diagram

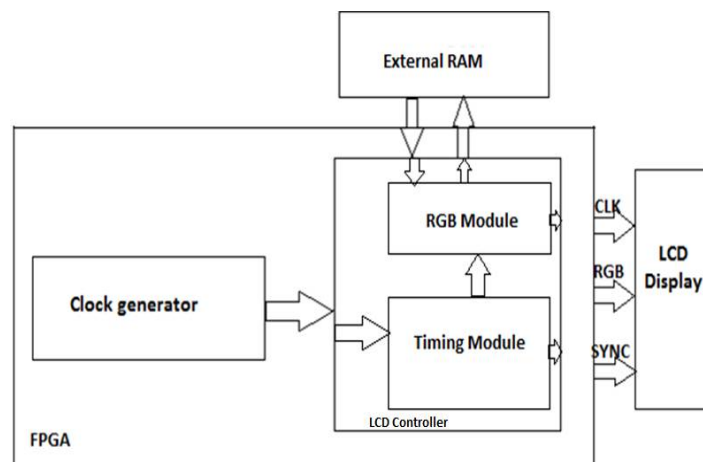


Fig.1 Block diagram of interfacing LCD controller to its display unit

The proposed engineering involves clock generator block, timing generator block, RGB generator block planned on an FPGA chip as shown in figure1. Remotely this proposed controller is associated with outside RAM (230Kb) and interfaced to the presentation unit. The signals generated from the controller block are clock signal of 6.25MHz, RGB signals and at last the horizontal and vertical synchronization signals. A frequency of 6.25MHz is generated from the clock generator obstruct from the input frequency of 100MHz. This 6.25MHz clock frequency shown in figure 4 is fed to timing generator block which will be helpful for generating synchronization signals with respect to the clock frequency. Then these signals are sent to RGB generator module which will send the RGB values to the screen with respect to those signals.

B. Clock frequency generation

The LCD panel requires a frequency of 6.25MHz as per the data sheets of the winstar LCD panel which is selected. The board that is being used is the spartan-6 FPGA board which has a clock frequency of 100MHz. In order to synchronize the clock frequency, a clock generator module is designed in the FPGA which uses that 100MHz clock as input and generates a frequency of 6.25MHz that is necessary. This module uses frequency divider to serve the purpose. Frequency divider by 16 is used. The clock of 100MHz is divided successively as shown in figure 4. This figure also illustrates the simulation waveform obtained from the design of clock generator module.

C. LCD Synchronization Signals

Synchronization signals are the horizontal and vertical signals.

Horizontal synchronization signal is one which scans every row of the display unit. Vertical synchronization signal is the one which scans the entire screen. Horizontal synchronization signal is split into four areas, back porch, front porch, valid data and the sync pulse itself. All these four areas of the horizontal signal are dummy pixel area and the rest of the area of the screen is the area of real image. Vertical Synchronization signal is also split in similar four areas. Scanning process must be performed to locate the position of the these two synchronization signals on the real image

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area. Refresh rate is also defined here, it indicates the rate at which scanning process takes place. Here a refresh rate of 58Hz is considered.

The timing parameter of a winstar display is shown in figure 2. It contains all the timing parameters details of the LCD panel that is being used. The units for all the parameters is also mentioned.

Parameter	Symbol	Min.	Typ	Max.	Unit
DCLK Frequency	1/ tDCLK	–	6.25	10	MHz
Horizontal Period	th	–	408	–	tDCLK
Horizontal Display	thd	320	320	320	tDCLK
Horizontal Back Porch	thb	–	68	–	tDCLK
Horizontal Front Porch	thf	–	20	–	tDCLK
Horizontal Pulse Width	thp	1	–	–	tDCLK
Vertical Period	tv	–	–	–	th
Vertical Display Period	tvd	240	240	240	th
Vertical Back Porch	tvb	–	18	–	th
Vertical Front Porch	tvf	–	4	–	th
Vertical Pulse Width	tvp	1	–	–	th

Fig. 2 Timing parameter of winstar 320 x 240 display

For Horizontal signal timings,

$$\begin{aligned} \text{TOTAL CLOCKS (TH)} &= \text{BACK PORCH (THB)} + \text{VALID DATA (THD)} + \text{FRONT PORCH (THF)} \\ &= 68 + 20 + 320 \\ &= 408 \end{aligned}$$

For Vertical signal timings,

$$\begin{aligned} \text{TOTAL LINES (TV)} &= \text{BACK PORCH (TVB)} + \text{VALID DATA (TVD)} + \text{FRONT PORCH (TVF)} \\ &= 18 + 240 + 4 \\ &= 262 \end{aligned}$$

$$\begin{aligned} \text{MINIMUM CLOCK} &= \text{TOTAL CLOCKS (TH)} \times \text{TOTAL LINES (TV)} \times \text{REFRESH RATE} \\ &= 408 \times 262 \times 58 \\ &= 6.19 \text{ MHz} \end{aligned}$$

IV. EXPERIMENTAL RESULTS

The LCD Controller is designed using verilog and its functionality is verified by simulation using verilog test bench.

The designs of clock generator module and timing generator module is done using verilog hardware description language. Their RTL schematic and simulation waveforms are observed.

The designs are synthesized using RTL synthesis and implemented using Xilinx ISE 14.1 on a Spartan6 XC6SLX4TQG144 FPGA based development board.

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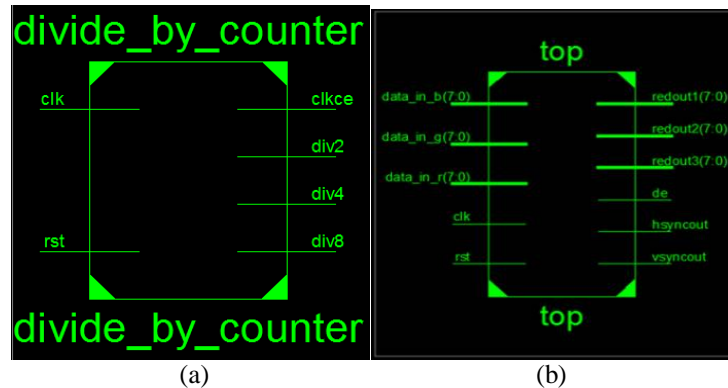


Fig 3: RTL schematic of (a) Clock generator & (b) Top module which includes both clock generator and timing generator module.

RTL schematic of the clock divider and the top module is shown in figure 3. In figure 3(a), clkce is the main output generating the requires frequency of 6.25MHz. In figure 3(b), RGB data input and outputs are shown, along with the synchronization signal outputs. Successive division of input clock frequency is shown in figure 4. Vertical synchronization signal generates a pulse of width 10th (horizontal period) after 240 horizontal counts, indicating that one time scan is completed. Horizontal synchronization signal generates a pulse of width 20tDCLK after 320 clock cycles, indicating one row of the screen is scanned and shown in figure 5 and 6. The simulation results, showing a valid VSYNC pulse and HSYNC pulse at the LCD interface is shown in figure 5, 6and 7.

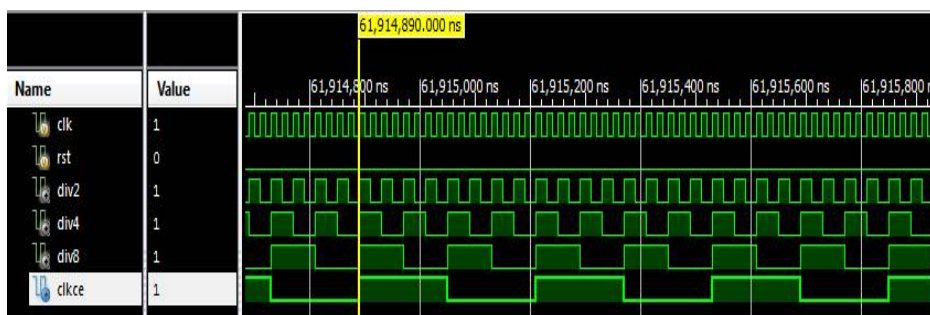


Fig 4 : Simulation waveform of clock generator is observed. 6.25MHz is generated from 100MHz input clock.

When VSYN, DE is high and at positive edge of the clock, read to the RGB block will be assigned and then the RGB data will be read from the external memory and sent to the display panel for display. A delay of one clock cycle can be observed in RGB data transfer and this is shown in figure 5.

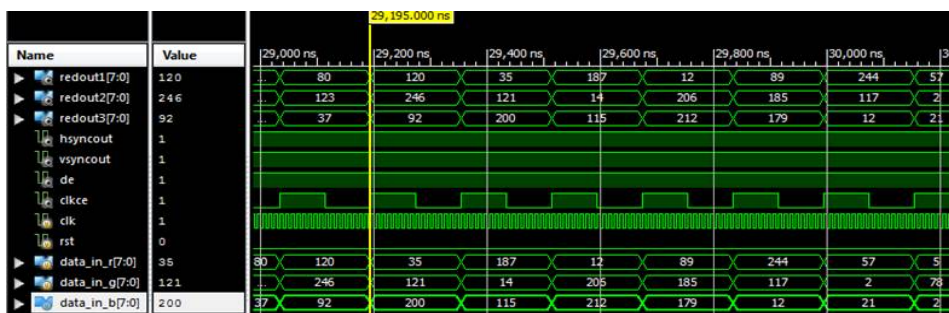


Fig 5 : Simulation waveform of both 6.25MHz clock and synchronization signals (Hsync & Vsync) are generated and observed.

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VSYNC signal generates a pulse of 10 cycles of HSYNC. After this pulse, the VSYNC signal goes high again for 240 cycles of HSYNC. This illustrates that VSYNC signal remains high until all the horizontal rows are scanned and here there are 240 horizontal rows of pixels. Its simulation waveform are shown in figure 6.

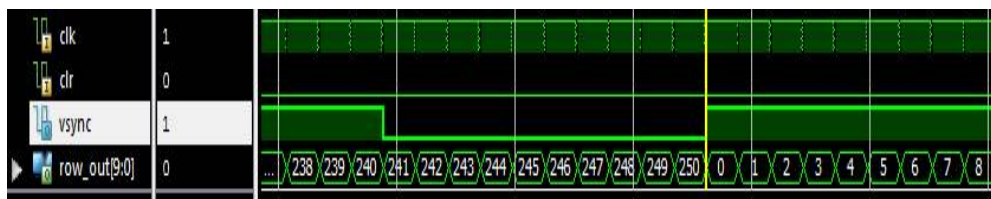


Fig 6: Shows simulation waveform of vertical synchronization signal

HSYNC signal also generates a pulse after scanning each row and its width is equivalent to 20 clock cycles of input clock and is shown in figure 7. HSYNC signal remains high for 320 clock cycles of input clock indicating it remains high until 320 pixels of a row is scanned.

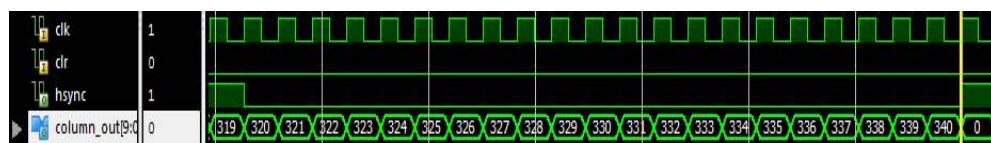


Fig 7 :Shows simulation waveform of horizontal synchronization signal

V. CONCLUSION

A review of host of relevant literature on designing LCD controller as a IP core yields to some important observation that any LCD display interface can be made possible, just outside the manufacturing foundry. IP core is a proprietary module of functionality that meets a certain specification allowing design reusability. They provide the possibility for the user to adjust parameters. Hence, LCD controller as a IP core attains more flexibility. Thus, FPGA based LCD controller are a excellent choice, since, it is easy to be designed and tiny to be used.

The application of Verilog as the design language speed up the whole design process. The suitable coding is developed to achieve the objective in a short time code .

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