

# Timing Diagram to Generate Triggering Pulses for Cascade Multilevel Inverters

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**ABSTRACT:** The multilevel inverters utilization has been increased since the last decade. These inverters are suitable in various high voltage and high power applications due to their ability to synthesize waveforms with better harmonic spectrum and faithful output. This paper presents a study of different types of cascade H-bridge multilevel inverters like 3-level, 5-level, 7-level and 9-level inverters. And also implemented timing diagrams to generate triggering pulses for the IGBT switches of cascade multilevel inverters. The Simulation results are presented using MATLAB/SIMULINK.

**KEYWORDS :** Cascaded H-bridge multilevel inverter (CHB), Timing diagram, triggering pulses, Matlab/simulink.

## I. INTRODUCTION

In high power and high voltage applications, the two level inverters, however, have some limitations in operation at high frequency mainly due to switching losses,  $dv/dt$  and  $di/dt$  stresses in power semiconductor devices and constraint of the semiconductor power device ratings. For high voltage applications two or more power devices can be connected in series to achieve the desired voltage ratings and in parallel to achieve the current ratings. Multilevel inverters[8] can increase the power by  $(m-1)$  times than that of two level inverter through the series connection of power semiconductor devices The cascaded multilevel inverter[2] was first introduced in 1975. Separate DC-sourced full bridge cells were placed in series to synthesize a staircase AC output voltage. The term multilevel began with the three level converters. Subsequently, several multilevel converter topologies have been developed.

## II. RELATED WORK

The concept of multilevel inverters is based on connecting H-bridge inverters in series to get a sinusoidal voltage output. The output voltage is the sum of the voltage that is generated by each cell. The number of output voltage levels are  $2n+1$ , where  $n$  is the number of cells. The switching angles can be chosen in such a way that the total harmonic distortion is minimized. One of the advantages of this type of multilevel inverter is that it needs less number of components comparative to the Diode clamped or the flying capacitor, so the price and the weight of the inverter is less than that of the two types.

### Three- level H-Bridge Inverter

Fig.1 (a) shows Full-bridge or “H-bridge” Voltage Source Inverter. The smallest number of voltage levels for a multilevel inverter using cascaded-inverter with SDCSs is three. To achieve a three-level waveform, a single full-bridge inverter is employed. Basically, a full-bridge inverter is known as an H-bridge[7] cell, which is illustrated in Fig. 1(a). The inverter circuit consists of four main switches and four freewheeling diodes. According to four-switch combination, three output voltage levels,  $+V$ ,  $-V$ , and  $0$  can be synthesized for the voltage across A and B. During inverter operation shown in Fig. 1, switch of  $S_1$  and  $S_4$  are closed at the same time to provide  $V_{ab}$  a positive value and a current path for  $I_o$ . Switch  $S_2$  and  $S_3$  are turned on to provide  $V_{ab}$  a negative value with a path for  $I_o$ . Depending on the load current angle, the current may flow through the main switch or the freewheeling diodes. When all switches are turned off, the current will flow through the freewheeling diodes.

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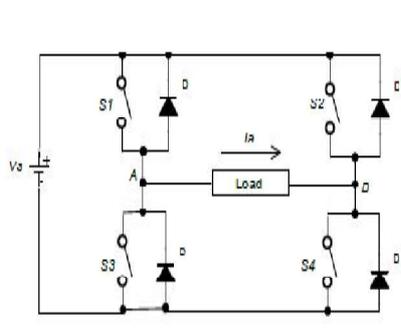


Fig.1(a) Three level H-bridge inverter

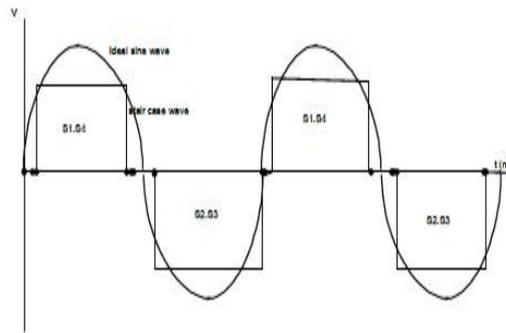


Fig.1(b) Output voltage waveform

The output wave form of three level inverter is shown in fig.1(b). To synthesize a multilevel waveform, the ac output of each of the different level H-bridge cells is connected in series. The synthesized voltage waveform is, therefore, the sum of the inverter outputs. The number of output phase voltage levels in a cascaded-inverter is defined by

$$M=2s+1$$

Where 's' is the number of dc sources. For example, a nine level output phase voltage waveform can be obtained with four-separated dc sources and four H-bridge cells. An *M* level cascaded H-bridge multilevel inverter needs  $2(M-1)$  switching devices where *M* is the number of the output voltage level

### Five-level Cascaded H-bridge multilevel inverter

The single phase cascaded five level inverter[3] topology has been proposed in Fig.2(a) .The circuit consists of eight main switches in two series connected H-bridge configuration S1~S4, and S5~S8. The number of dc sources is two so the output voltage of the cascaded multilevel inverter is

$$V_o = V_{a1} + V_{a2}$$

Where the output voltage of the first cell is labeled  $V_{a1}$  and the output voltage of the second cell is denoted by  $V_{a2}$ . There are five level of output voltage ie  $2V, V, 0, -V, -2V$ .

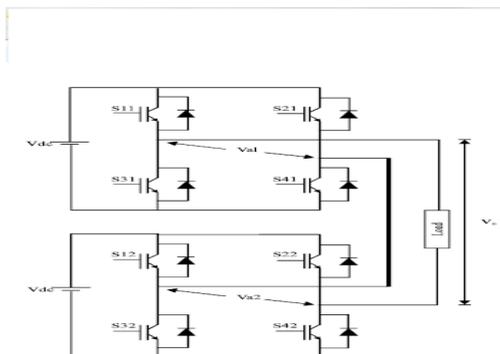


Fig.2(a) 5-level cascade H-bridge inverter

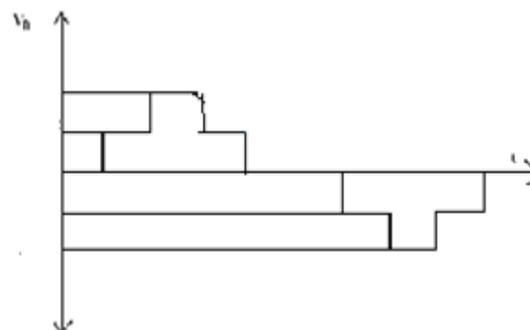


fig.2(b) output voltage waveform

### Seven-level cascade H-bridge multi level inverter

Fig.3 (a) shows a seven level cascaded H-bridge multilevel inverter[6]. The converter consists of three series connected H-bridge cells which are fed by independent voltage sources. The outputs of the H-bridge cells are

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(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 5, May 2016

connected in series such that the synthesized voltage waveform( as shown in fig.3(b)) is the sum of all of the individual cell outputs. The output voltage is given by

$$V=V1 +V2+V3$$

Where the output voltage of the first cell is labelled V1, the output voltage of the second cell is denoted by V2 and the output voltage of the third cell is denoted by V3. There are seven level of output voltage ie 3V,2V, V, 0, -V, -2V,-3V.The main advantages of cascaded H-bridge inverter is that it requires least number of components, modularized circuit and soft switching can be employed.

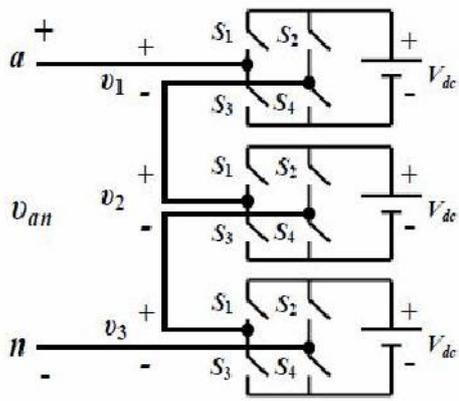


Fig.3(a) 7-level cascade H-bridge inverter

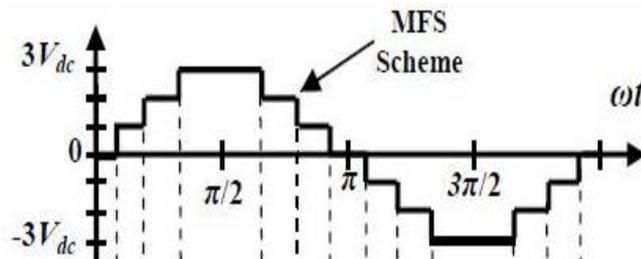


fig.3(b) output voltage waveform

## Nine-level cascade H-bridge multilevel inverter

The nine level converters[5] consist of four series connected H-bridge cells with four separate DC sources as shown in fig.4(a) . The circuit has sixteen main switches in four series connected H-bridge configuration S1~S4, S5~S8, S9~S12 and S13~S16. The output voltage is given by

$$V=V1 +V2+V3+V4$$

Where the output voltage of the first cell is labeled V1, the output voltage of the second cell is denoted by V2 , the output voltage of the third cell is denoted by V3 and the output voltage of the fourth cell is denoted by V4. There are nine level of output voltage ie 4V, 3V, 2V, V, 0, -V, -2V,-3V,-4V

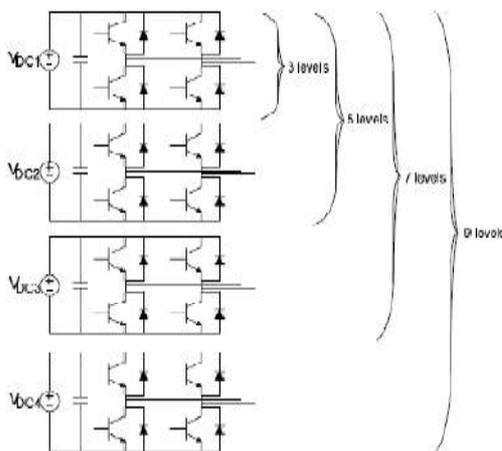


Fig.4(a) 9-level cascade H-bridge inverter

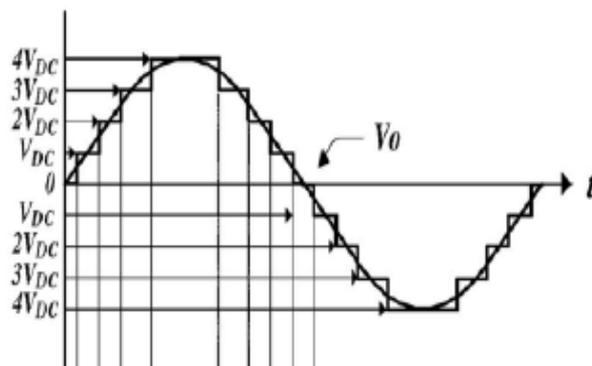


Fig.4(b) output voltage waveform

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## III. TIMING DIAGRAM AND SIMULATION RESULTS OF 3, 5, 7 and 9-LEVEL INVERTERS

### Three-level H-bridge inverter

The simulink model of three level H-bridge inverter is shown in fig-5(a). It consists one dc voltage source, 4 IGBT/DIODE switches and 4 pulse generators. The pulse generators(P1 for S1,P2 for S2,P3 for S3 and P4 for S4) are used to generate the triggering pulses for the switches according to the timing diagram.

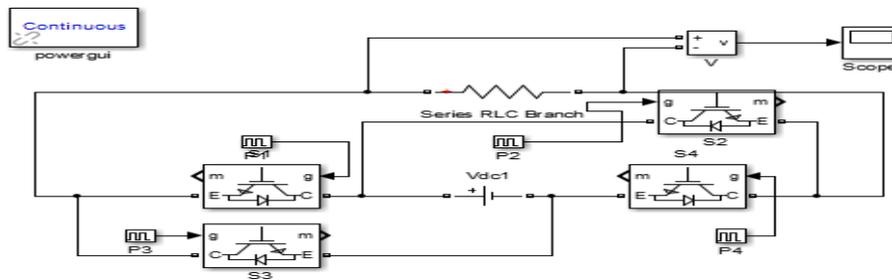


Fig.5(a) Matlab/simulink model of three level H-bridge inverter

Fig-5(b) shows the timing diagram to generate triggering pulses for the four switches based on the voltage level and also see the output waveform of three level H-bridge Inverter. Here P1&P4 pulses for getting positive voltage and P2&P3 pulses for getting negative output voltage .

	VOLTAGE LEVELS			
Time(sec.)	0.005	0.01	0.015	0.02
Angle(Deg.)	90°	180°	270°	360
PULSE NO.	0V	Vdc (50V)	0V	-Vdc (-50V)
P1&P4		25%		
P2&P3				25%
	0V	50V	0V	50V

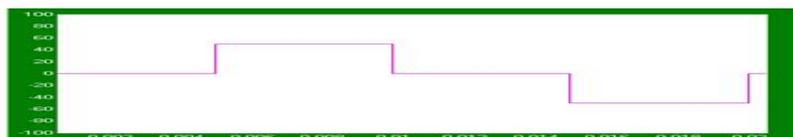


Fig.5 (b) Timing diagram and output waveform of 3-level inverter

### Five-level cascade H-bridge inverter

The simulink model of five level cascade H-bridge inverter is shown in fig-6(a). It consists 8 IGBT/DIODE switches in two series connected H-bridges ,two dc voltage sources and 8 pulse generators. The pulse generators are used to generate the triggering pulses for the switches according to the timing diagram.

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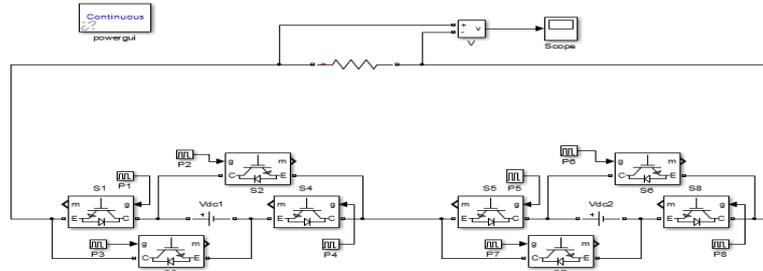


Fig.6 (a) Matlab/simulink model of five level cascade H-bridge inverter

Fig-6(b) shows the timing diagram to generate triggering pulses for the eight switches based on the voltage level and also see the output waveform of five level cascade H-bridge Inverter. Here P1,P4,P5&P8 pulses for getting + 2Vdc voltage, P1,P4 &P8 for getting + Vdc voltage ,P3,P2,P6&P7 for getting -2Vdc and P3,P6,&P7 pulses for getting -Vdc voltage .



Fig.6 (b) Timing diagram and output waveform of 5-level inverter

## Seven-level cascade H-bridge inverter

The simulink model of seven level cascade H-bridge inverter is shown in fig-7(a).It consists 12 IGBT/DIODE switches in three series connected H-bridges ,three dc voltage sources and 12 pulse generators. The pulse generators are used to generate the triggering pulses for the switches according to the timing diagram.

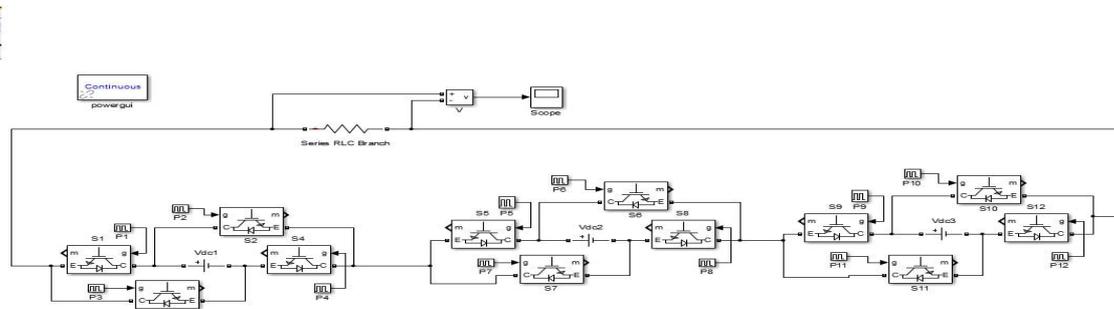


Fig.7 (a) Matlab/simulink model of seven level cascade H-bridge inverter

Fig-7(b) shows the timing diagram to generate triggering pulses for the 12 switches based on the voltage level and also see the output waveform of seven level cascade H-bridge Inverter Here P1,P4,P5,P8,P9&p12 pulses for getting +3Vdcvoltage,P1,P4,P8,P9&P12 for getting +2Vdc voltage P1,P4,P8,P&P12 for getting +Vdc,P3,P2,P6,P7,P10,P11 for getting -3Vdc and P3,P2,P7,P10&P11 pulses for getting -2Vdc voltage and P3,P7,P10&P11 for getting -Vdc.

Time(sec.)	VOLTAGE LEVELS											
	0.001 6	0.0033	0.005	0.0066	0.0083	0.01	0.0116	0.0133	0.015	0.0166	0.0183	0.02
Angle(Deg.)	30°	60°	90°	120°	150°	180°	210°	240°	270°	300°	330°	360°
PULSE NO.	0	V (50)	2V (100)	3V (150)	2V (100)	V (50)	0	-V (-50)	-2V (-100)	-3V (-150)	-2V (-100)	-V (-50)
P1,P4,P8 & P12	Pulse width 41.6%											
P3,P7, P10 & P11							41.6%					
P2							25%					
P5				8.33%								
P6							8.33%					
P9	25%											

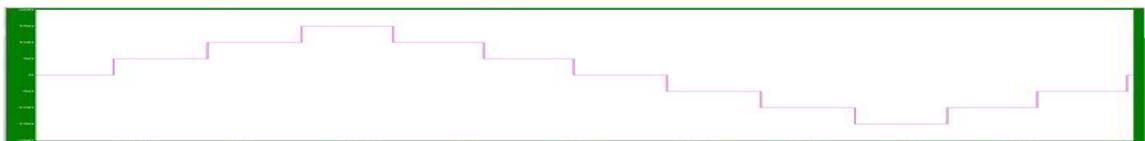


Fig.7 (b) Timing diagram and output waveform of 7-level inverter

### Nine-level cascade H-bridge inverter

The simulink model of nine level cascade H-bridge inverter is shown in fig-8(a).It consists 16 IGBT/DIODE switches in four series connected H-bridges ,four dc voltage sources and 16 pulse generators. The pulse generators are used to generate the triggering pulses for the switches according to the timing diagram..

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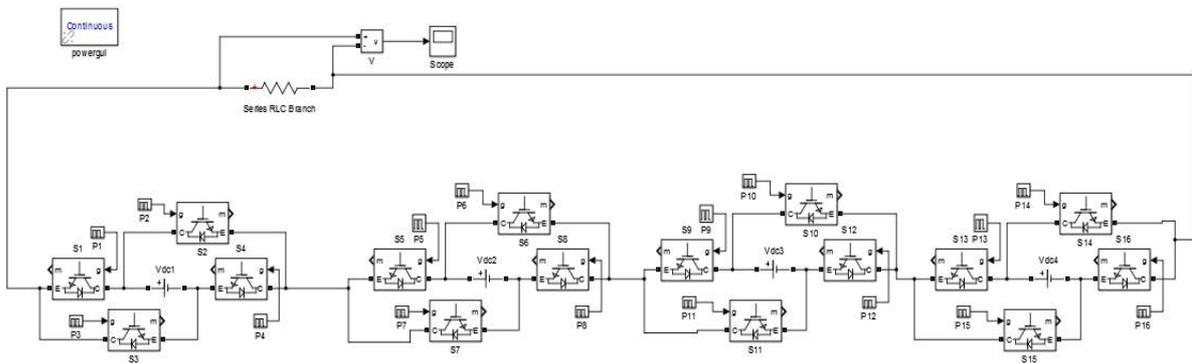


Fig.8 (a) Matlab/simulink model of nine level cascade H-bridge inverter

Fig-8(b) shows the timing diagram to generate triggering pulses for the 12 switches based on the voltage level and also see the output waveform of seven level cascade H-bridge Inverter in fig-8(c).

	voltage level																
Time (sec)	0.0	0.00	0.00	0.00	0.00	0.00	0.00	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.02	
Angle (deg.)	0°	22.5°	45°	67.5°	90°	112.5°	135°	157.5°	180°	202.5°	225°	247.5°	270°	292.5°	315°	337.5°	360°
Pulse no.	0	Vdc	2 Vdc	3 Vdc	4 Vdc	3 Vdc	2 Vdc	Vdc	0	-Vdc	-2 Vdc	-3 Vdc	-4 Vdc	-3 Vdc	-2 Vdc	-Vdc	0
P1,P4,P8,P12,P16	Pulse width 43.75%																
P3,P7,P11,P14,P15									43.75%								
P2									31.25%								
P5					6.2 5%												
P6					18.75%												
P9					18.75%												
P10									6.2 5%								
P13	31.25%																

Fig-8(b) Timing diagram of 9-level inverter

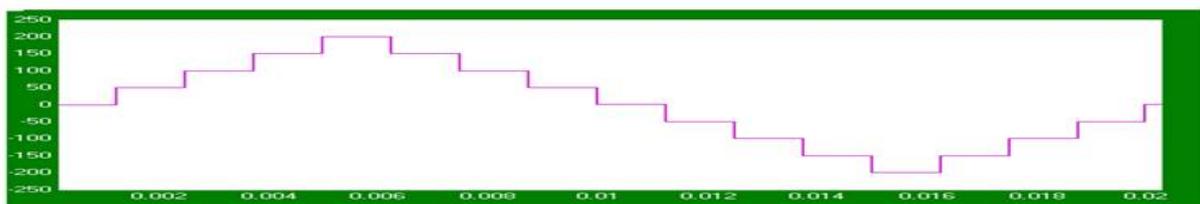


Fig.8 (c) output waveform of 9-level inverter

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## IV. CONCLUSION

From the above discussion and results it can be concluded that the timing diagram gives the clear idea to generate required switching pattern for the cascaded H-bridge multilevel inverters. This paper gives good reference for the beginners, who doing research on the multilevel inverters.

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