

Simulation Analysis of SRAM Cell Structures Using Low Power Reduction Techniques

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ABSTRACT : SRAM is one of the common embedded memory for CMOS IC's and it consists of Bistable latching circuitry to store a bit. Power consumption and speed are the main factors for designing a chip along with the leakage power. The power consumption and speed of SRAMs are some important issues among a number of factors that provides a solution which describes many designs to minimize the consumption of power. Here this article presents the simulation of 6T,8T and 9T SRAM cells using Low power reduction techniques and develops a modified model which provides the consumer with less costs and reduced power delay product. Simulations have been carried out on 90nm at Tanner EDA tool and the overall circuit is verified using Tanner tool.

KEYWORDS : Various SRAM cells, CMOS Logic ,Low power and VLSI

I. INTRODUCTION

Memory Architecture is Random-access architecture and it is same as Asynchronous design. The SRAM IC is read write (R/W) memory circuit that permits the modification as well as their retrieval. The SRAM IC was developed by CDS IC446, cadence IC design environment. The most popular, full CMOS 6-transistor cell configuration was used to design the SRAM memory array. Fewer advantages are high switching speeds while using full CMOS SRAM configuration.

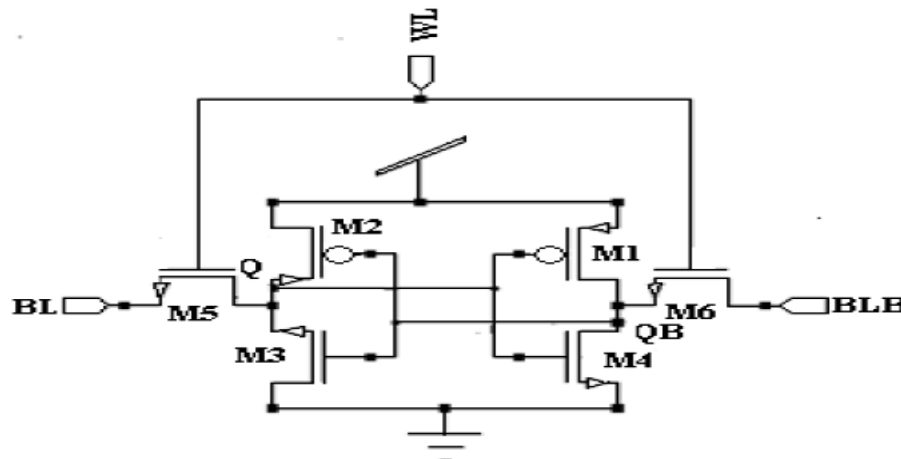


FIGURE 1. 6T SRAM CELL STRUCTURE

II. LOW POWER SRAM

SRAM cell introduces one control signal transistor for controlling these transistors, the below figure shows the write mode SRAM. Due to one more transistors area is increased in comparison to normal approach. This control transistor uses control select signals which are used to properly control the dissipation in power.

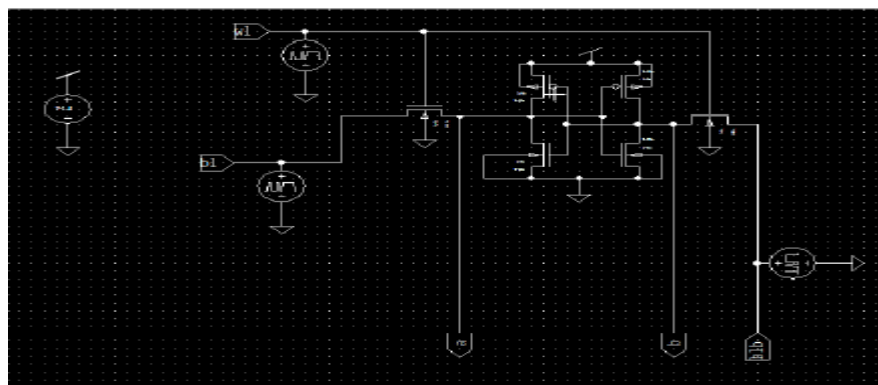


FIGURE 2. 6-T SRAM IN S-EDIT

Figure 3 shows the dual-ported cell (8T-SRAM cell) created by adding two transistors; the read operation can be entirely decoupled from the write operation in an 8T cell by sensing the data through a separate read stack controlled by separate read word lines (RWL).

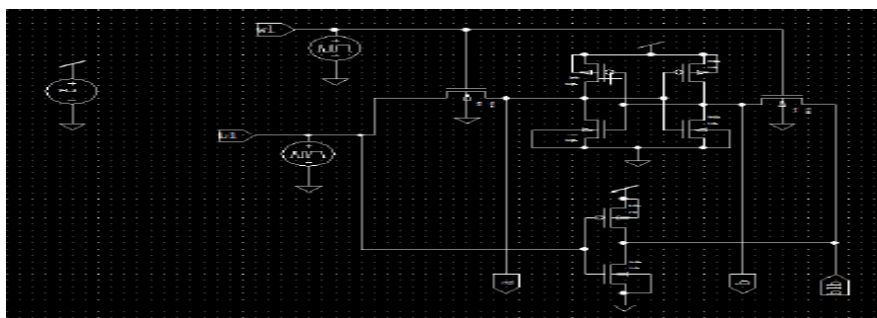


FIGURE 3. 8-T SRAM IN S-EDIT

The Schematic view of 9T SRAM cell, for CMOS technology. The upper sub circuit of the 9T memory is sufficient to have a 6-T with minimum sized devices which is composed of M3,M4,M5,M6,M1 and M2; whereas the write signal (WR) control M5 and M6. The data is stored in upper memory sub-circuit. The Lower sub circuit of the new cell is composed of the bit line access transistors(M7 and M8) and the read access transistor (M9). The 9T SRAM cell completely separates the data from the bit lines during a read operation, The idle 9T SRAM cells are placed in to a super cutoff sleep mode, thereby reducing the leakage power consumption as compared to the standard 6T SRAM cells

A dual-ported cell is created by adding two data output transistors to 6T cell, separation of data retention element and data output element means that there will be no correlation between the read SNM cell and I cell. In this 8T cell has 30% more area and power than a conventional 6T SRAM cell whereas the 9T SRAM cell is different from their structure and various simulation analysis has been made for 9T with other number of

transistors in an SRAM cell. The 9T SRAM Schematic view is shown in the below figure, which is built using Tanner EDA tool using Schematic Edit (S-Edit) to compare their results.

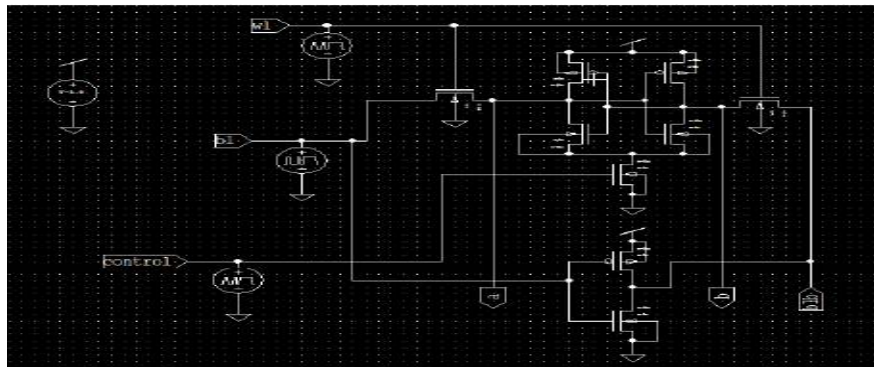


FIGURE 4. 9T SRAM IN S-EDIT

III. SIMULATION ANALYSIS

All the above circuits taken for analysis are simulated using 90nm technology on Tanner EDA tool. To make impartial testing environment all the circuits has been simulated on the same input patterns.

IV. SIMULATION RESULTS

The below figure 5 ,6 and 7 shows output waveforms of different SRAM cells at 90nm technology.

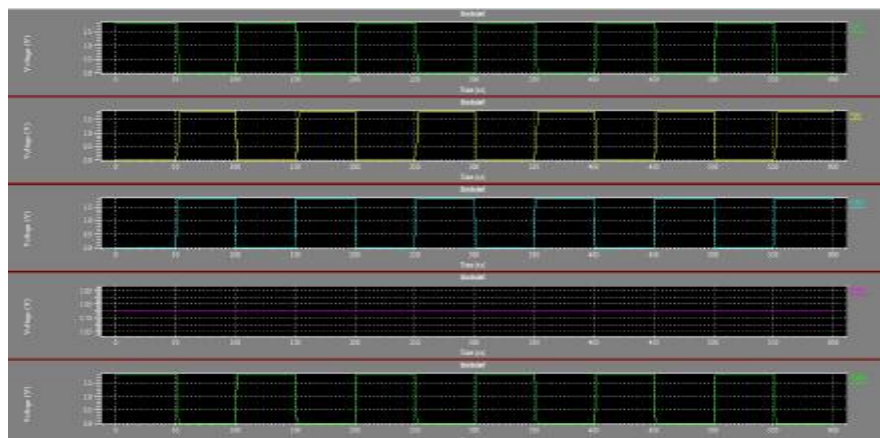


FIGURE 5. OUTPUT WAVEFORM OF 6T SRAM

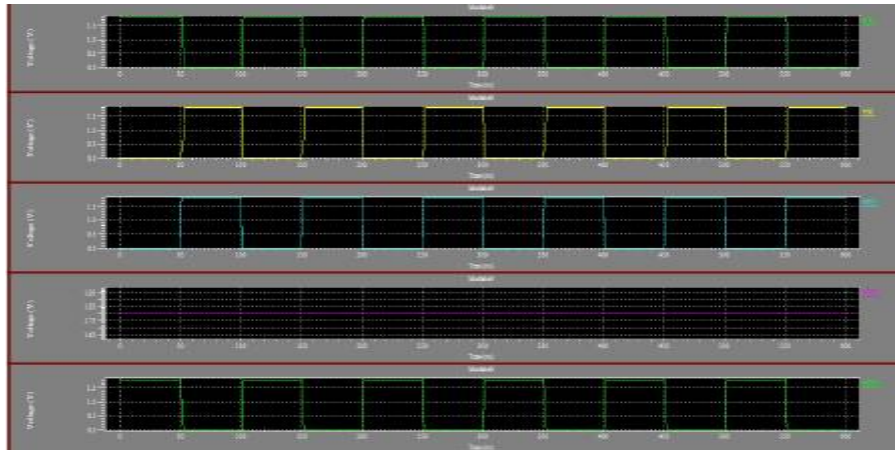


FIGURE 6. OUTPUT WAVEFORM OF 8T SRAM

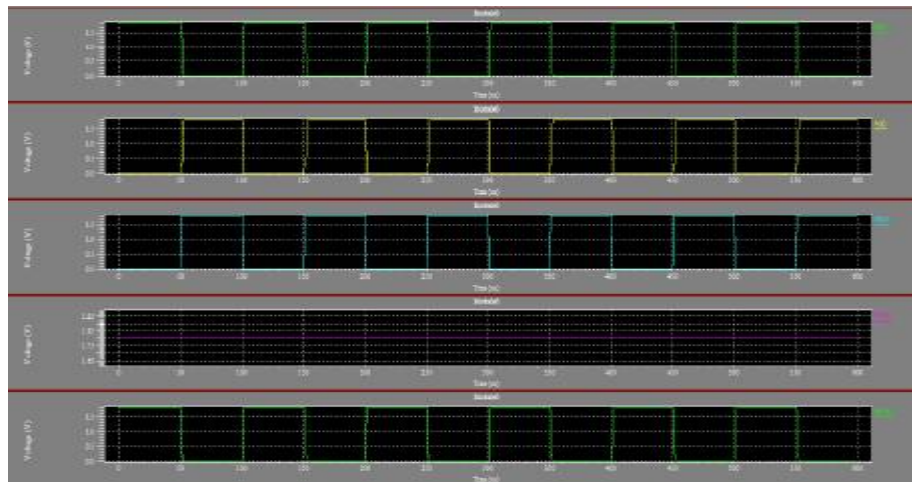


FIGURE 7. OUTPUT WAVEFORM OF 9T SRAM

V. COMPARISON RESULTS

The Power and Delay of different SRAM cells are observed

Design Style	No.of transistors	Minimum length(micro meter)	Avg.power consumption(watts)	Prop. Delay(nano sec)
6T	6	.09	2.3×10^{-4}	1.8×10^{-10}
8T	8	.09	3.3×10^{-4}	2.5×10^{-10}
9T	9	.09	1.8×10^{-3}	1.3×10^{-9}

VI. CONCLUSION

The techniques used to reduce the power dissipation is the reduction of the supply voltage. The power dissipation reduction in SRAMs is not considered only to power supply voltage reduction, but also due to operating frequency and temperature. The Average power consumption of 9T is less when compared to 6T and 8T. To improve their reliability, the lifetime of battery is a prime concern at the cost of speed. The reduction in the power consumption reduces the problem associated with high temperature and also provides an extra advantage in terms of extended battery life.

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