

VHDL Implementation of Genetic Algorithm for Evolutionary Combinational Circuits

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ABSTRACT: Electronic hardware's demands that the simple in architecture, power consumption, speed in operation and should be automatically regenerating the program if the program is failure. Genetic algorithm is one of the evolutionary algorithms. Using evolutionary algorithm we can get the desired program automatically. FPGA configuration bits are perfectly matches with binary bits of evolvable hardware. So evolvable hardware is mainly used to implement the evolutionary algorithm. The reconfigurable FPGA is used to save the time when we redesign the failure program. In this paper we discuss about the evolvable unit for adder.

KEYWORDS: Genetic algorithm (GA), reconfigurable FPGA, evolvable hardware, adder, evolutionary algorithm

I. INTRODUCTION

Artificial intelligence, reconfigurable hardware, autonomous system and fault tolerance are combined and formed evolvable hardware. EHW is mainly used in two areas (i) new solutions are automatically generated (ii). Implement the adaptive devices. Evolvable hardware is used implement the stochastic algorithm. The mainly used to stochastic algorithm is genetic algorithm [1]. Genetic algorithm is designed based on the biological evolution process and use the concepts of natural selection and genetic inheritance. A genetic algorithm maintains candidates of population solution for the problem and it makes evolve by continuously applying the stochastic operators.

Field Programmable Gates arrays are a subset of field programmable devices (FPD) [3]. FPGAs are programmable logic devices that permit the implementation of digital system. FPGAs are the most popular digital reconfigurable devices in the evolvable hardware community. FPGA based implementation of Evolvable Hardware can be divided into two groups. (i) The FPGA serves in the fitness calculation only. The EA (which is executed on a personal computer or a digital signal processor (DSP)) sends configuration bitstreams representing candidate circuit to the FPGA in order to obtain their fitness value. (ii) The entire evolvable system is implemented in an FPGA, where evolutionary algorithm implemented on same chip or separate boards to evolving designs [4].

FPGA are typically composed of an array of uniform logic cells, interconnected through programmable interconnection matrices, which configurable to perform a given function by means of an array of a configuration bitstreams. Each logic cell is composed of combinational and sequential programmable components, whose inputs and outputs are connected to a programmable interconnection matrix [5]. FPGAs are composed of Look-up tables (LUT), configurable logic blocks (CLB) and an interconnection network

II. GA AND VIRTUAL RECONFIGURABLE CIRCUIT

Genetic algorithm is first introduced by "JOHN HOLLAND" in 1975. Genetic algorithm is inspired by the biological evolution process. Generally it uses the concepts of "genetic inheritance" and "natural selection" Initialization: Initially many individual solutions are randomly generated to form an initial population [7]. The population size depends on the nature of the problem, but typically contains several hundreds or thousands of possible solutions. Selection: During each successive generation, a proportion of the existing population is selected to breed a new generation. Individual solutions are selected through a fitness-based process, where fitter solutions (as measured by a fitness function) are typically more likely to be selected.

Fitness: The chromosomes define the structure of the logic circuit. An encoding system is to be representing the structure of combination logic circuit [8]. The length of the chromosomes depends on the size of the entire structure. The number of bits in the chromosomes represents the type of gate. The collection of all individuals of the cell represents a solution. The next step is to generate a second generation population of solutions from those selected through genetic operators: crossover (also called recombination), and/or mutation. Termination: This algorithm terminates when either a maximum number of generations has been produced, or a satisfactory fitness level has been reached for the population.

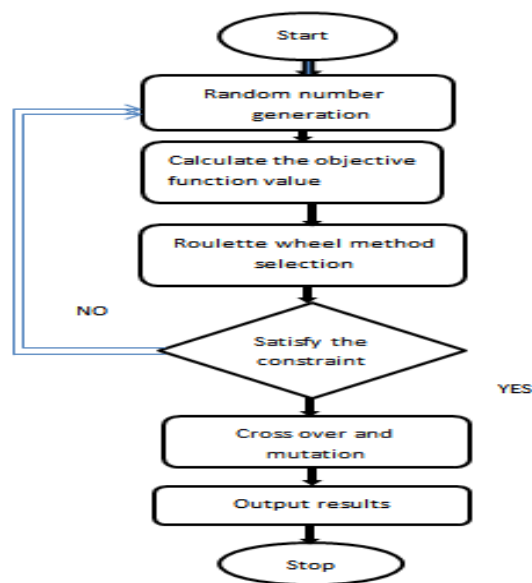


Fig.1. flow chart for Genetic algorithm

Virtual Reconfigurable circuit was introduced by Sekanina.L in 2006. VRC is the combination of software reconfigurable devices and genetic algorithm [9]. The structure of the VRC circuit is determined by downloading the binary bit strings called architecture bits. This is one of the new kinds of reconfigurable platform using the conventional FPGA. Once VRC is uploaded into FPGA the following parts are created at specified positions. (i) An array of programmable elements, (ii) Configuration port, (iii) Configuration memory and (iv) programmable interconnection network [10]. VRC architecture is similar to the Cartesian genetic programming architecture. Multiplexers are used as routing elements. Programmable elements have a number of registers to store the information. Programmable interconnection network is used to connect the programmable elements.

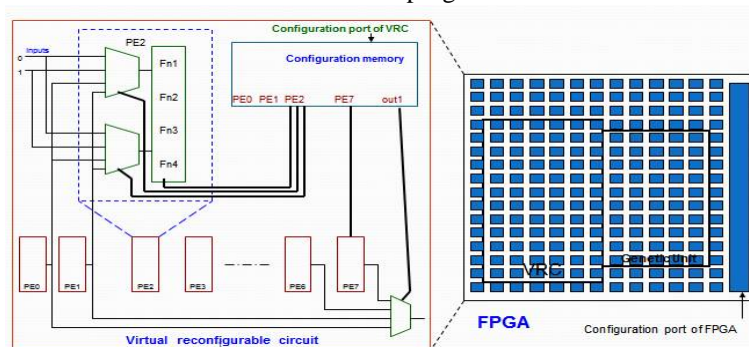


Fig.2. virtual reconfigurable circuit

III. PROPOSED UNIT FOR ADDER

Evolvable hardware is used to increase the speed and performance. Evolvable hardware is mainly suitable for the space missions. The commonly used evolutionary algorithm is genetic algorithm. By using genetic algorithm we can get the desired circuit automatically if the circuit is failure. Evolutionary algorithm works based on the principle of natural evolution and self-adoption

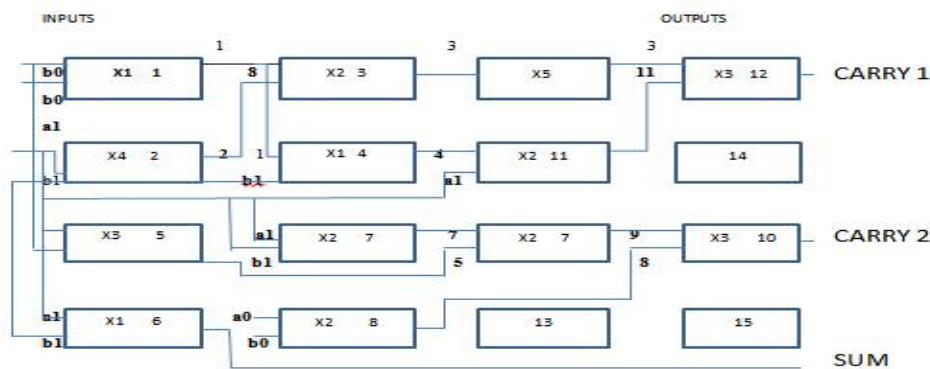


Fig.3 proposed circuit

IV. RESULTS AND DISCUSSION

1. Initialization

The different 44x4 bits outputs are generated for every rising edge clock by using XOR logic. The simulated waveform is shown in fig 4. This random number we considered as initial population of individuals. This random number generation process until termination of Genetic Algorithm (sufficient fitness achieved).

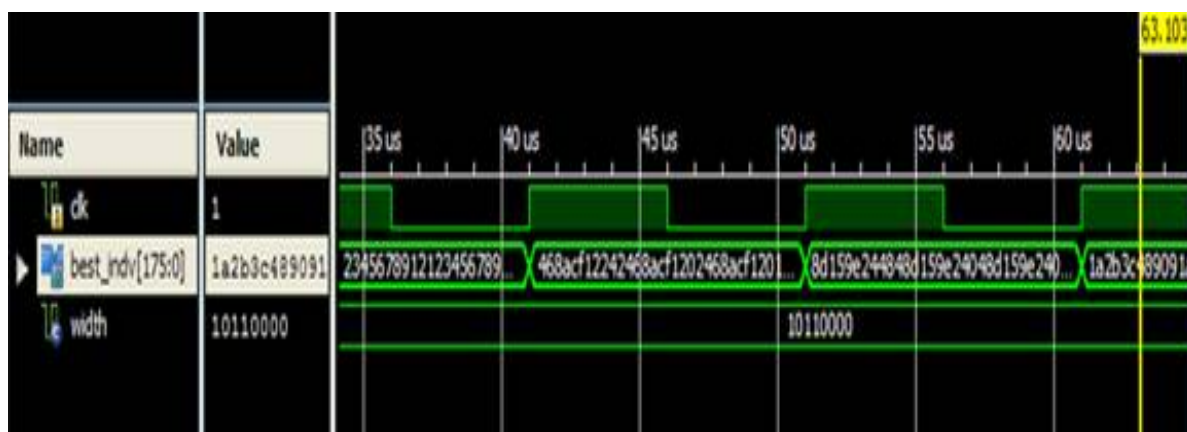


Fig.4.Simulation result for initialization.

2. Crossover

Crossover is an alternative method to generate random numbers. Crossover simulated result shown in fig 8. best_indv signal represents input data and random_pattern represents output data. Single point crossover technique used for to generate random numbers.



Fig.5. Simulation result for crossover

Fitness Calculation Simulated output window is shown in fig 6, here best_indv considered as an input and best_fit representing output, it shows each and every best_indv's fitness status. Pe_indv[15:0] representing Programmable Elements input status. pe_indv_out representing pe_indv output status, inputs[3:0] representing a0,a1,b0,b1 status. Fns [15:0] represents Logical Function condition.

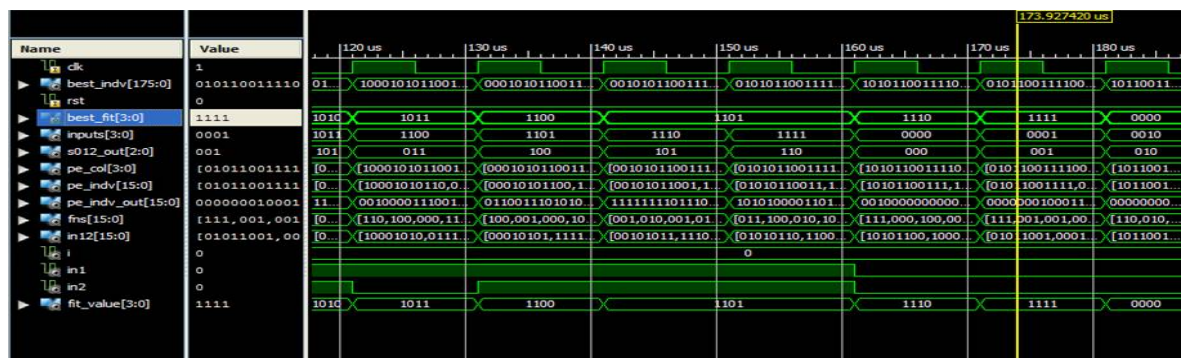


Fig.6. Simulation result for fitness calculation

V.CONCLUSION

Proposed 2-bit adder is designed by using 16 number of PEs. The configuration of every PE is represented in the chromosomes as input1, input2, and function. 11 bits are needed to configure a single PE. The length of the chromosome is $\Lambda=51$ and size of the search space is up to $|C|=10^{11}$. For dynamic adaption EHW using bio-inspired techniques like Genetic Algorithm (GA). Once a 2-bit adder is evolved using genetic algorithm, other combinational logic and sequential logic circuits will be the next step to evolve.

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