

Performance Analysis of 4 Bit & 8 Bit Vedic Multiplier for Signal Processing

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ABSTRACT: Vedic multiplier is hinged on the ancient algorithms. This work is based on all the sutras (formula) in Vedic mathematics. This formula is meant for faster mental calculation than normal multiplication. In general, though the simulation is faster even if implemented in hardware, it consumes more power. This paper presents a technique to modify the architecture of the Vedic multiplier by using some existing methods in order to reduce power and improve signal processing application. Here, different bits are encoded for Vedic multiplier Verilog HDL and synthesized using Synopsys Design Compiler. The performance is compared in terms of area, data arrival time and power with earlier existing architecture of Vedic multiplier. Signal processing involves a lot of multiplications which consumes more time; this can be negligible by the new algorithms. This paper proposes an approach for signal processing using Vedic Mathematics which performs faster multiplication compared to the conventional algorithms such as Booth and Array Multiplication Algorithm. Time required by the algorithms for processing signals are then compared using the experimental results.

KEYWORDS: Fast Multiplication, Nikhilam sutra, Signal processing, Vedic multiplier.

1. INTRODUCTION

Multipliers are an important component in today's image signal and other digital signal processing applications. Technological advancement has brought to design multipliers which makes design with high speed, low power consumption, less area or even combination of them in one multiplier, thus making them suitable for various high speed, low power and compact VLSI implementation. Thus, integrating Vedic mathematics for the multiplier design will improve the speed of multiplication operation in multiplier. A simple digital Vedic multiplier architecture based on the UrdhvaTiryakbhyam Sutra is used. This formula (sutra) was used in ancient India for the multiplication of two decimal numbers in relatively less time. The multiplier architecture is based on UrdhvaTiryagbhyam (vertical and cross-wise algorithm) sutra. The 4x4 multiplication has been performed in a single step in UrdhvaTiryagbhyam sutra [1], whereas in shift and add (conventional) method, four partial products have to be added to get the result. Thus, by using UrdhvaTiryagbhyam Sutra in binary multiplication, the number of steps required to calculate the final product will be reduced and hence there is a reduction in computational time and an increase in speed of the multiplier. Two prominent measurements are associated with multiplication algorithms: latency and throughput of the system. Latency is defined as the real time delay of a computation and the measure of computations can be done during given processing time. The execution time in DSP systems is dependent on multipliers, so we need supreme multipliers. The mathematical operations using Vedic Method are efficient and have requirements; this can be used to improve the computational speed of processors.

This paper describes the design of a multiplier based on Urdhva-Tiryakbhyam sutra (Vertically and Crosswise technique) of Vedic Mathematics using EDA tool. In this paper, the Vedic multiplier brings a change in efficiency of a processor than any other system with improved speed to any digital processor.

II. ALGORITHM

These algorithms which can be applied to various branches of engineering such as computing and digital signal processing[2]. Implementation of Multiplier Using Vedic Algorithm based on the natural principles on which the human mind works effectively than normal mathematical calculation which implied in technology gives better speed to the processor.

These Sutras along with their brief meanings are enlisted below alphabetically.

- 1) (Anurupye) Shunyamanyat- If one is in ratio, the other is zero.
- 2) Chalana Kalanabyham- Differences and similarities.
- 3) Ekadhikina Purvena- By one more than the previous one.
- 4) Ekanyunena Purvena- By one less than the previous one.
- 5) Gunakasamuchyah- Factors of the sum is equal to the sum of factors.
- 6) Gunitasamuchyah- The product of sum is equal to sum of the product.
- 7) Nikhilam Navatashcaramam Dashatah- All from 9 and last from 10.
- 8) Paraavartya Yojayet- Transpose and adjust.
- 9) Puranapuranabyham- By the completion or noncompletion.
- 10) Sankalana- vyavakalanabyham- By addition and by subtraction.
- 11) Shesanyakena Charamena- The remainders by the last digit.
- 12) Shunyam Saamyasamuccaye- When the sum is same then sum is zero.
- 13) Sopantyadvayamantyam- The ultimate and twice the penultimate.
- 14) Urdhva-tiryakbhyam- Vertically and crosswise.
- 15) Vyashtisamanstih- Part and Whole.
- 16) Yaavadunam- Whatever the extent of its deficiency.
- 7) The remainder remains constant
- 8) The first by the first and the last by the last

III. MULTIPLIER ARCHITECTURE

A. Architecture of Vedic multiplier

Processing of images or video signal on Field Programmable Gate Array is complicated, since it needs separate architectures to process the image. To facilitate these operations, Matlab, Simulink and Xilinx system generator tools, which convert the image into suitable formats that are supported by FPGA, are used. An Instrumental role in generating VHDL/VERILOG code in tune with algorithms designed in Simulink[3]. The generated code will be dumped into FPGA and then it performs operations on image. Use of multiplier algorithm in image processing effectively reduces total design time of a system. A multiplier design using Vedic mathematics was presented gives idea for designing the multiplier and adder unit was implemented from ancient mathematics "Vedas". Based on those sutras (formulae), the partial products and sums are generated in single line which reduces the carry propagate from LSB to MSB. The implementation of the Vedic method and digital application to the complex multiplier made substantial reduction in propagation delay and comparison with conventional based architecture and vedic implementation which are most commonly used architectures. The implementation of the Vedic algorithms in DSP process signal based on Vedic mathematics and its implementation on xilinx is shown.

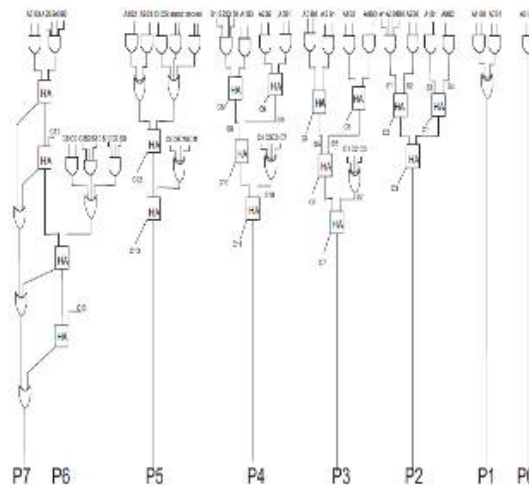


Figure 1: Multiplier architecture

B. Partial Products Equations

Consider two 4-bit

binary numbers $a_3a_2a_1a_0$ and $b_3b_2b_1b_0$. The partial products P_0 to P_7 generated are given by the following equations:

- i. $P_0 = a_0b_0$
- ii. $P_1 = a_0b_1 + a_1b_0$
- iii. $P_2 = a_0b_2 + a_1b_1 + a_2b_0 + P_1$
- iv. $P_3 = a_0b_3 + a_1b_2 + a_2b_1 + a_3b_0 + P_2$
- v. $P_4 = a_1b_3 + a_2b_2 + a_3b_1 + P_3$
- vi. $P_5 = a_1b_2 + a_2b_1 + P_4$
- vii. $P_6 = a_3b_3 + P_5$
- viii. $P_7 = \text{carry of } P_6$

UrdhvaTiryakbhyam Sutra is a general multiplication formula applicable to all cases of multiplication [4]. It literally means "Vertically and Crosswise". The square is divided into rows and columns where each row/column corresponds to one of the digit of either a multiplier or a multiplicand. Thus, each digit of the multiplier has a small box common to a digit of the multiplicand [5]. Each digit of the multiplier is then independently multiplied with every digit. In this paper, image processing operations using Field Programmable Gate Arrays (FPGA). The architecture of 2x2 and 4x4 bit Vedic multiplier modules such that "Urdhva-Tiryakbhyam" (Vertically and Crosswise) sutra(formula) is used to construct an architecture for the multiplication of two binary numbers(any bit). The impact of Vedic multiplier is partial product generation and additions are execute concurrently. Hence, this is well adapted to parallel processing. This feature makes it more effective for binary multiplications. This in turn increase speed and reduces delay.

IV. RESULTS AND DISCUSSION

The time taken for multiplication operation has reduced by employing the Vedic algorithms. The proposed Vedic multiplier architecture exhibits speed improvements[6]. The computational path delay for 4-bit and 8-bit Vedic multiplier is 5.352 ns and 8.751 ns. In this paper, 4x4 bit Vedic multiplier using "UrdhvaTiryakbhyam" Sutra(formula) is implemented in Very High Speed Integrated Circuit Hardware Descriptive Language(VHDL Code). Logic synthesis and simulation was done using EDA (Electronic Design Automation) tool in Xilinx ISE9.2i - Project Navigator and ISim simulator integrated in the Xilinx package respectively. Table displays the comparison of results of the proposed Vedic multiplier with the Conventional multipliers in time

delay (nanoseconds). The combinational path delay obtained for the proposed 4x4 bit Vedic multiplier is 5.32 ns whereas the result of other multiplier are more time consumed than proposed one. Corresponding results of simulation and synthesis have shown below

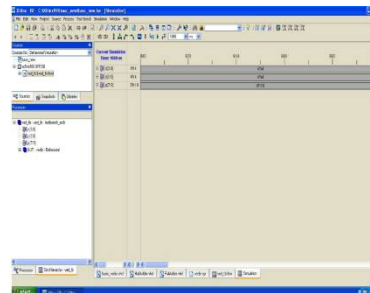


Figure 2: Result of 4-bit multiplier

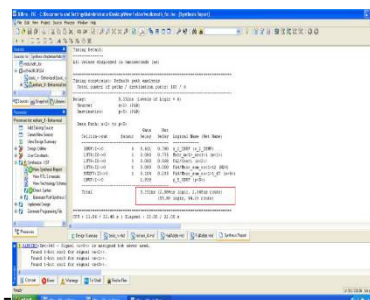


Figure 3: Report of 4-bit multiplier

Synthesis result shows that for 4-bit multiplication maximum combinational path delay 5.352 ns.

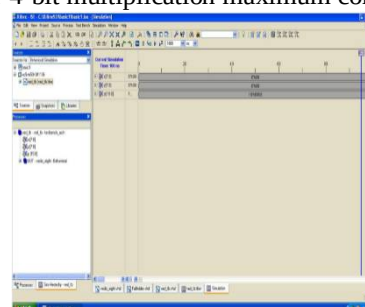


Figure 4: Result of 8-bit multiplier

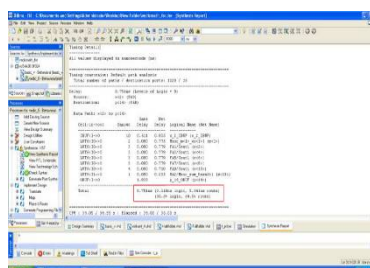


Figure 5: Report of 8-bit multiplier

Synthesis result shows that for 8-bit multiplication maximum combinational path delay 8.751 ns.

Table 1: Comparison of multiplier results

	Vedic multiplier	Booth multiplier	Wallace tree multiplier
4-bit	5.35	7.45	9.33
8-bit	8.75	10.32	12.65

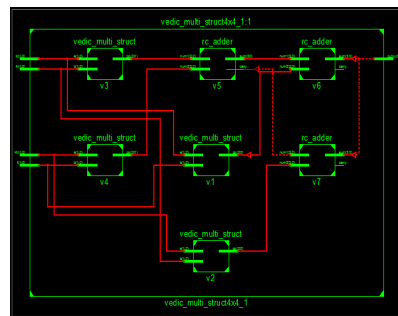


Figure 6, RTL schematic of 4x4 bit Vedic Multiplier

The RTL (Register Transfer Level) of the 4x4 bit Vedic multiplier contains four 2x2 bit Vedic multiplier as `vedic_multi_struct v1, v2, v3, v4` and three 4-bit Ripple Carry Adder as `rc_adde v5, v6, v7` is shown in Figure 6, the simulated results obtained from the figure shown for verification. In behavioral simulation we tested for input bits: -Input value of "0100" (in decimal number system 4) and "0100" (decimal number system 4) as and we get "00001000" as output (decimal number system 8). The inputs of 4-bits are converted into the input of 2-bits. The input for MSB (Most Significant Bit) & LSB (Least Significant Bit) of multiplicand are `kh=01` and `kl=00`, when the input for MSB (Most Significant Bit) & LSB (Least Significant Bit) of multiplier are `lh=00` and `ll=01`. Finally, the output1=00010000, gives the final 8-bit result. However the rest signals establish the intermediate results like partial products (sum & carry).

Vedic Algorithm For Signal Processing Application

The above Vedic algorithm implemented in image processing application to enhance the image quality by Vedic calculations will give a successive variation in timings and power consumption of multiplier device. This type of multiplier increases the efficiency of the overall system or processor. The microprocessors used thus far have standard INTEL architecture that is suitable for conventional mathematical methods. Even Vedic methods have achieved substantial time and power savings. If processor architecture are convenient for Vedic methods designed, then one can further reduce the processing time. Since Vedic algorithms utilize decimal digits directly for their operations, it is considered appropriate to use binary coded decimal (BCD) architectures in place of the binary architecture presently used the world over. VLSI technology can provide the necessary design and simulation tools to develop processors based on BCD architecture. Such processors would be most suitable for implementing Vedic algorithms and may offer further savings in processing time.

V. CONCLUSION

Vedic formulae are based on the fundamentals. It can be used for many applications in Engineering and Technology. This interesting field presents some effective algorithms which can be applied to design of Digital filters. The potential of this field can be used efficiently to solve the real world problems. With use of Vedic multiplier it is possible to reduce area, increase speed, decrease power consumption and to reduce complexity of digital FIR and IIR filters. It is possible to carry out research work on uses of Vedic mathematical algorithms over traditional (existing) methods in FIR and IIR filters that will provide effective results for de-noising of biomedical Signals. FIR and IIR filtering consists of operations like multiplication, addition. By using Vedic sutras fundamental entities of FIR and IIR filters can be implemented to achieve merits like reduced area, fast speed etc.

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