

Quaternary Logic Lookup Table in Standard CMOS

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ABSTRACT: Interconnections are increasingly the dominant contributor to delay, area and energy consumption in CMOS digital circuits. Multiple-valued logic can decrease the average power required for level transitions and reduces the number of required interconnections, hence also reducing the impact of interconnections on overall energy consumption. In this paper, we propose a quaternary lookup table (LUT) structure, designed to replace or complement binary LUTs in field programmable gate arrays. The circuit is compatible with standard CMOS processes, with a single voltage supply and employing only simple voltage-mode structures. A clock boosting technique is used to optimize the switches resistance and power consumption. The proposed implementation overcomes several limitations found in previous quaternary implementations published so far, such as the need for special features in the CMOS process. The experimental results demonstrate the correct quaternary operation and confirm the power efficiency of the proposed design.

KEYWORDS: Field-programmable gate array (FPGA), lookup table (LUT), multiple-valued logic (MVL), quaternary logic, standard CMOS technology.

I. INTRODUCTION

In conventional binary CMOS digital circuits, static power consumption is tightly related to leakage currents, and dynamic power consumption is determined by (1), where C is the capacitance of the nodes being driven and V_{DD} is the power supply voltage.

$$P_D \propto CV_{DD}^2 \quad (1)$$

The CMOS process has evolved by shrinking the transistors (thus reducing C) and employing lower supply voltages (lower V_{DD}), therefore saving power and integrating more functionality into the same area. However, capacitance C also includes the routing capacitance associated with the wires connecting the logic gates. It has been reported that routing is exceeding transistors contributions for latency and power dissipation of designs in modern CMOS processes [1]. An approach to mitigate the impact of interconnections is to use multiple-valued logic (MVL) [3], hence, more information can be carried in each wire, reducing the routing network. Therefore, a single wire carrying a signal with N logic levels can replace $\log_2 N$ wires carrying binary signals. Reducing the routing leads to a direct reduction of the line capacitances and the overall circuit area.

This paper proposes a novel view of MVL circuits through the design of a look up table (LUT) based on the quaternary representation that exploits simple voltage-mode standard CMOS circuits and optimized switches using a simplified clock boosting (CB) technique. The proposed MVL LUT can replace or complement conventional binary logic, since the designed circuit is simple, efficient and we can combine both; i.e., they use the same implementation/fabrication technology.

II. QUATERNARY LOGIC AND LUTS

A quaternary variable can assume four different logic levels. Assuming a rail-to-rail voltage range and equal noise margins for the four logic levels, three different reference voltage values are required, $1/6V_{DD}$, $3/6V_{DD}$, and $5/6V_{DD}$, to determine a quaternary value. Since a quaternary variable (Q) is able to carry twice as much information as a binary variable (B), we have the following relation:

$$|Q| = 2 \times |B|. \quad (3)$$

Therefore, two binary variables may be grouped into one quaternary variable without information loss, merging two nodes into one. It should be noted that there is no direct conversion of binary to quaternary logic gates in conventional CMOS, since the binary circuits use the available power rails to represent the binary symbols. For quaternary logic there are two more intermediate levels, which cannot be obtained directly using the same techniques. On the other hand, viable implementations of quaternary circuits have already been achieved for LUTs, as demonstrated in [9].

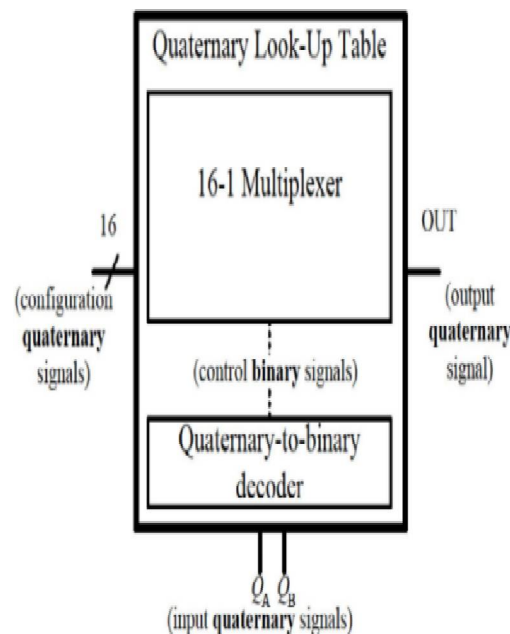


Fig. 1 Proposed quaternary LUT

A LUT is an array indexing operator, where the output is mapped by the input, based on the configuration memory. The configuration values are initially stored in the LUT configuration memory, and according to the input, the logic value in the addressed position is assigned to the output.

The number of possible functions that may be represented in a quaternary LUT is much larger than in a binary LUT with the same number of inputs and outputs. Therefore, apart from reducing the total number of connections, MVL also leads to a reduction of the total number of gates when compared with a binary implementation.

III. PROPOSED QLUT TOPOLOGY AND IMPLEMENTATION

The proposed 2-input 1-output QLUT is shown in Fig. 1. For this given QLUT complexity, 16 quaternary configuration inputs are necessary, one for each possible combination of the two quaternary inputs. The

configuration word defines the reconfigurable quaternary function. In practice, the input signals are used to select which one of the configuration inputs is connected to the output. The proposed QLUT is composed of two main blocks: a 16-1 multiplexer using an array of switches, that establishes a low-resistance path between one configuration input and the output according to the input values; and a quaternary-to-binary decoder, consisting of a 2-bit analog-to-digital (ADC) frontend followed by combinational logic used to generate the control signals feeding the multiplexer. These blocks are described in the following sections.

A. 16-1 Multiplexer: Due to the quaternary nature of its inputs, the 16-1 multiplexer shown in Fig. 1 may be thought of as an analog multiplexer. The output is assumed to be of a capacitive nature and its value is defined by the interconnection network to which the QLUT output is connected.

B. Quaternary-to-Binary Decoder: The 2-bit quaternary-to-binary decoder allows the use of a single row of switches to drive the input configuration signals to the output of the QLUT. To do so, it is necessary to generate 16 control signals, to be applied in the $clk1$ inputs of each switch. These switches are employed to connect one quaternary configuration input to the output. To generate the required control signals, the quaternary variables are decoded into binary, allowing the use of binary logic gates. Thus, an ADC frontend is necessary, considering the analog nature of the quaternary signals.

Q_A	Q_B	x_A	w_A	z_A	x_B	w_B	z_B	$cs(activebit)$
0 ₄	0 ₄	1 ₂	1 ₂	1 ₂	1 ₂	1 ₂	1 ₂	$cs(1)$
1 ₄	0 ₄	0 ₂	1 ₂	1 ₂	1 ₂	1 ₂	1 ₂	$cs(2)$
2 ₄	0 ₄	0 ₂	0 ₂	1 ₂	1 ₂	1 ₂	1 ₂	$cs(3)$
3 ₄	0 ₄	0 ₂	0 ₂	0 ₂	1 ₂	1 ₂	1 ₂	$cs(4)$
0 ₄	1 ₄	1 ₂	1 ₂	1 ₂	0 ₂	1 ₂	1 ₂	$cs(5)$
1 ₄	1 ₄	0 ₂	1 ₂	1 ₂	0 ₂	1 ₂	1 ₂	$cs(6)$
2 ₄	1 ₄	0 ₂	0 ₂	1 ₂	0 ₂	1 ₂	1 ₂	$cs(7)$
3 ₄	1 ₄	0 ₂	0 ₂	0 ₂	0 ₂	1 ₂	1 ₂	$cs(8)$
0 ₄	2 ₄	1 ₂	1 ₂	1 ₂	0 ₂	0 ₂	1 ₂	$cs(9)$
1 ₄	2 ₄	0 ₂	1 ₂	1 ₂	0 ₂	0 ₂	1 ₂	$cs(10)$
2 ₄	2 ₄	0 ₂	0 ₂	1 ₂	0 ₂	0 ₂	1 ₂	$cs(11)$
3 ₄	2 ₄	0 ₂	0 ₂	0 ₂	0 ₂	0 ₂	1 ₂	$cs(12)$
0 ₄	3 ₄	1 ₂	1 ₂	1 ₂	0 ₂	0 ₂	0 ₂	$cs(13)$
1 ₄	3 ₄	0 ₂	1 ₂	1 ₂	0 ₂	0 ₂	0 ₂	$cs(14)$
2 ₄	3 ₄	0 ₂	0 ₂	1 ₂	0 ₂	0 ₂	0 ₂	$cs(15)$
3 ₄	3 ₄	0 ₂	0 ₂	0 ₂	0 ₂	0 ₂	0 ₂	$cs(16)$

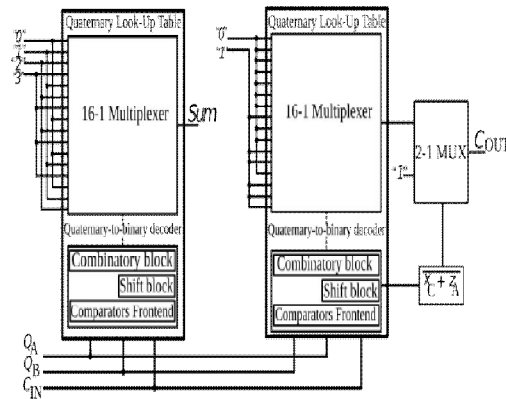
TABLE I: COMBINATIONAL BLOCK LOGIC FUNCTION

Q_A	Q_B	C_{IN}	SUM	C_{OUT}	Q_A	Q_B	C_{IN}	SUM	C_{OUT}
0 ₄	0 ₄	0 ₄	0 ₄	0 ₄	0 ₄	0 ₄	1 ₄	1 ₄	0 ₄
0 ₄	1 ₄	0 ₄	1 ₄	0 ₄	0 ₄	1 ₄	1 ₄	2 ₄	0 ₄
0 ₄	2 ₄	0 ₄	2 ₄	0 ₄	0 ₄	2 ₄	1 ₄	3 ₄	0 ₄
0 ₄	3 ₄	0 ₄	3 ₄	0 ₄	0 ₄	3 ₄	1 ₄	0 ₄	1 ₄
1 ₄	0 ₄	0 ₄	1 ₄	0 ₄	1 ₄	0 ₄	1 ₄	2 ₄	0 ₄
1 ₄	1 ₄	0 ₄	2 ₄	0 ₄	1 ₄	1 ₄	1 ₄	3 ₄	0 ₄
1 ₄	2 ₄	0 ₄	3 ₄	0 ₄	1 ₄	2 ₄	1 ₄	0 ₄	1 ₄
1 ₄	3 ₄	0 ₄	0 ₄	1 ₄	1 ₄	3 ₄	1 ₄	1 ₄	1 ₄
2 ₄	0 ₄	0 ₄	2 ₄	0 ₄	2 ₄	0 ₄	1 ₄	3 ₄	0 ₄
2 ₄	1 ₄	0 ₄	3 ₄	0 ₄	2 ₄	1 ₄	1 ₄	0 ₄	1 ₄
2 ₄	2 ₄	0 ₄	0 ₄	1 ₄	2 ₄	2 ₄	1 ₄	1 ₄	1 ₄
2 ₄	3 ₄	0 ₄	1 ₄	1 ₄	2 ₄	3 ₄	1 ₄	2 ₄	1 ₄
3 ₄	0 ₄	0 ₄	3 ₄	0 ₄	3 ₄	0 ₄	1 ₄	0 ₄	1 ₄
3 ₄	1 ₄	0 ₄	0 ₄	1 ₄	3 ₄	1 ₄	1 ₄	1 ₄	1 ₄
3 ₄	2 ₄	0 ₄	1 ₄	1 ₄	3 ₄	2 ₄	1 ₄	2 ₄	1 ₄
3 ₄	3 ₄	0 ₄	2 ₄	1 ₄	3 ₄	3 ₄	1 ₄	3 ₄	1 ₄

TABLE II: FULL ADDER LOGIC FUNCTION

IV. FULL ADDER CIRCUIT

In this section, we employ the proposed QLUT to implement a full adder. The conventional and direct approach would require four QLUTs to properly implement this function, two QLUTs for each output, sum and carry out, working with the two possible values of the carry in. However, we propose minor modifications to the designed QLUT, which allows the reduction of the number of QLUTs only to two. This is achieved at the cost of a slight increase in binary combinational logic and a 2-1 multiplexer, as shown in F



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increasing power consumption or losing performance. Experimental results were performed on an ASIC implementation of a full adder employing the designed QLUT.

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