

A Unity Power Factor Bridgeless Buck-Boost Converter Fed BLDC Motor Drive

Ayushi Jain¹, Ashok Kumar Sharma², Priyanka Yadav¹PG Student, Department of Electrical Engineering, Rajasthan Technical University, Kota, India¹Associate Professor, Department of Electrical Engineering, Rajasthan Technical University, Kota, India²

ABSTRACT: Targeting a cost effective solution for low power applications, this paper deals with power factor corrected (PFC) bridgeless (BL) buck-boost converter fed brushless direct current (BLDC) motor drive. By varying the dc-bus voltage of the voltage source inverter (VSI), speed of BLDCM is controlled and the latter is electronically commutated for reduced switching losses. For reducing the conduction losses associated with the buck-boost converter, a BL configuration of the buck-boost converter is proposed which offers the elimination of diode bridge rectifier. The proposed PFC-based BL converter is designed to operate in discontinuous inductor current mode (DICM) to achieve an inherent PFC at the ac mains. The obtained power quality indices are under the specified limits of international power quality standard IEC 61000-3-2 over a wide range of speed control. The performance of the proposed BLDCM is simulated in MATLAB/Simulink environment.

KEYWORDS: Bridgeless buck-boost converter, brushless direct current motor, discontinuous inductor current mode, power factor corrected (PFC).

I. INTRODUCTION

The BLDC motor is a three-phase synchronous motor consisting of a stator with three-phase concentrated windings and a rotor with permanent magnets [6], [7]. BLDC motor is referred as an electronically commutated motor, since electronic commutation based on the Hall-effect rotor position signals is used, rather than mechanical commutation. The preference of BLDC motors, over other motors, is due to its high efficiency, high reliability, high ruggedness, low electromagnetic interference (EMI) problems, and excellent performance over a wide range of speed control [1] [2]. Due to its ease, it finds applications in many household appliances, industrial tools, medical equipment, precise motion control, and automation and transportation [3]-[5].

The conventional scheme of BLDC motor drive fed by an uncontrolled rectifier and a dc-link capacitor based VSI used for feeding the BLDCM [8] draws peaky, harmonic rich current from the supply. This results in a poor power factor (as low as 0.7) and high total harmonic distortion (THD) of supply current (as high as 65%) at the ac mains. Such power quality indices are not acceptable by international power quality standard IEC 61000-3-2 [9]. Also, these PQ indices increase the EMI in the power factor correction (PFC) converter. At lower and higher frequencies, the EMI is primarily caused by the conduction and radiation respectively; which causes problems such as skin effect, high overshoot transients, hysteresis loss, eddy current loss, and voltage drop which affect the overall efficiency and performance of the system. Thus, for improving the power quality at ac mains improved power quality converters (IPQCs) are used to reduce such EMI problems [10], [11].

The improved power quality converters designing and the choice of mode of operation is a critical issue as it directly affects the cost and rating of the components used in the PFC converter. The two different modes of operation in which a front-end converter is designed to operate are continuous conduction mode (CCM) and discontinuous conduction mode (DCM) [12], [13]. A voltage follower approach is one of the control techniques, which is used for a PFC converter operating in the DCM. It requires a single voltage sensor for controlling the dclinkvoltage with a power factor correction. Thus, it offers a simpler way to achieve PFC and dc-link voltage control, but at the cost of high stress on PFC converter switch [12], [13]. On the other hand, current multiplier approach offers low stresses on the PFC switch,

but requires three sensors for PFC and dc-link voltage control [12], [13]. Hence, voltage follower control is advantageous over current multiplier control.

II. RELATED WORK

Singh and Singh [20] proposed a buck–boost converter feeding a BLDC motor based on the concept of PWM-VSI for speed control and constant dc link voltage having high switching losses. Singh and Singh [8] also proposed a Cuk converter-fed BLDC motor drive with the concept of variable dc link voltage which reduces the switching losses in VSI. A CCM operation of the Cuk converter has also been utilized requiring three sensors but was not encouraged for low cost and low power rating. For the improvement in efficiency, further, the bridgeless (BL) converters are used which allow the elimination of DBR in the frontend [18]–[24]. A buck–boost converter configuration proved to be best suited among various BL converter topologies for applications requiring a wide range of dc link voltage control. Jang and Jovanović [21] and Huber *et al.* [22] presented BL buck and boost converters, respectively. These can provide the voltage buck [13] or voltage boost [22], [23] which limits the operating range of dc link voltage control. Wei *et al.* [24] have proposed a BL buck–boost converter but use three switches which is not a cost-effective solution. This paper gives a cost effective solution for bridgeless buck–boost converter reducing the number of components.

III. PROPOSED PFC BL BUCK-BOOST CONVERTER FED BLDC MOTOR DRIVE

The proposed BL buck–boost converter-based VSI-fed BLDC motor drive is shown in Fig. 1. The parameters of the BL buck–boost converter are designed such that it achieves an inherent power factor correction at ac mains. It operates in discontinuous inductor current mode (DICM). The dc link voltage of the VSI using a BL buck–boost converter is controlled for adjusting the speed of the BLDC motor. Thus, reducing the switching losses in VSI due to the low frequency operation of VSI for the electronic commutation of the BLDC motor. The performance of the proposed drive is evaluated for a wide range of speed control with improved power quality at ac mains.

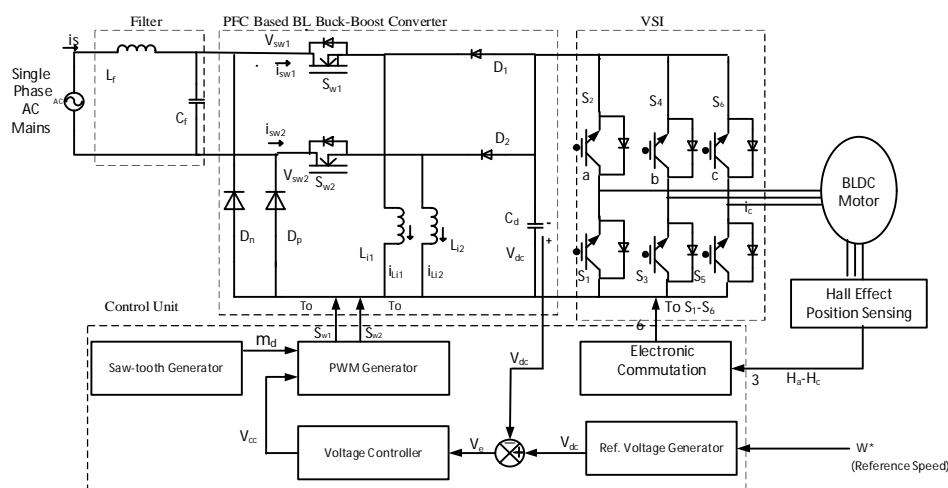


Fig. 1. Proposed BLDC motor drive with front-end BL Buck-Boost converter

IV. OPERATION OF PFC-BASED BL BUCK-BOOST CONVERTER

Operation of the proposed PFC based BL buck–boost converter is classified into two different sections for a line cycle and a switching cycle. Fig. 2((a) to (c) for positive half and (d) to (f) for negative half cycle of supply voltage) shows three different modes of operation in switching cycle.

A) Operation during Complete Line Cycle of Supply Voltage

The proposed scheme of the BL buck–boost converter is designed such that switches $Sw1$ and $Sw2$ conduct for the positive and negative half cycles of the supply voltage, respectively. During the positive half cycle of the supply voltage, switch $Sw1$, inductor $Li1$, and diodes $D1$ and Dp are operated to transfer energy to dc link capacitor Cd shown in Fig. 2(a)–(c). Similarly, during the negative half cycle of the supply voltage, switch $Sw2$, inductor $Li2$, and diodes $D2$ and Dn conduct as shown in Fig. 2(d)–(f). In the DICM operation of the BL buck–boost converter, the current in inductor Li becomes discontinuous for a certain duration in a switching period.

B) Operation during Complete Switching Cycle

For a complete switching cycle of the proposed converter, there are three modes of operation in the positive half cycle of the supply voltage. In first mode of operation, the switch $Sw1$ conducts to charge the inductor $Li1$ and this increases the inductor current $iLi1$ as shown in Fig. 2(a). Diode Dp completes the input side circuitry, and the dc link capacitor Cd is discharged by the VSI-fed BLDC motor. In second mode of operation, switch $Sw1$ is turned off, and the transfer of stored energy in inductor $Li1$ takes place to dc link capacitor Cd until the inductor is completely discharged. The current in inductor $Li1$ decreases till it reaches zero. In third mode, no energy is left in the inductor $Li1$ and hence, it enters discontinuous conduction, i.e. current of $Li1$ becomes zero for the rest of the switching period. At this time, as shown in Fig. 2(c), both switch and diode are not conducting, and energy is supplied to the load via dc link capacitor Cd ; hence, voltage Vdc across dc link capacitor Cd starts to decrease. The operation is repeated when switch $Sw1$ is turned on again after a complete switching cycle. Similarly, during the negative half cycle of the supply voltage, switch $Sw2$, inductor $Li2$, and diodes Dn and $D2$ operate for voltage control and PFC operation.

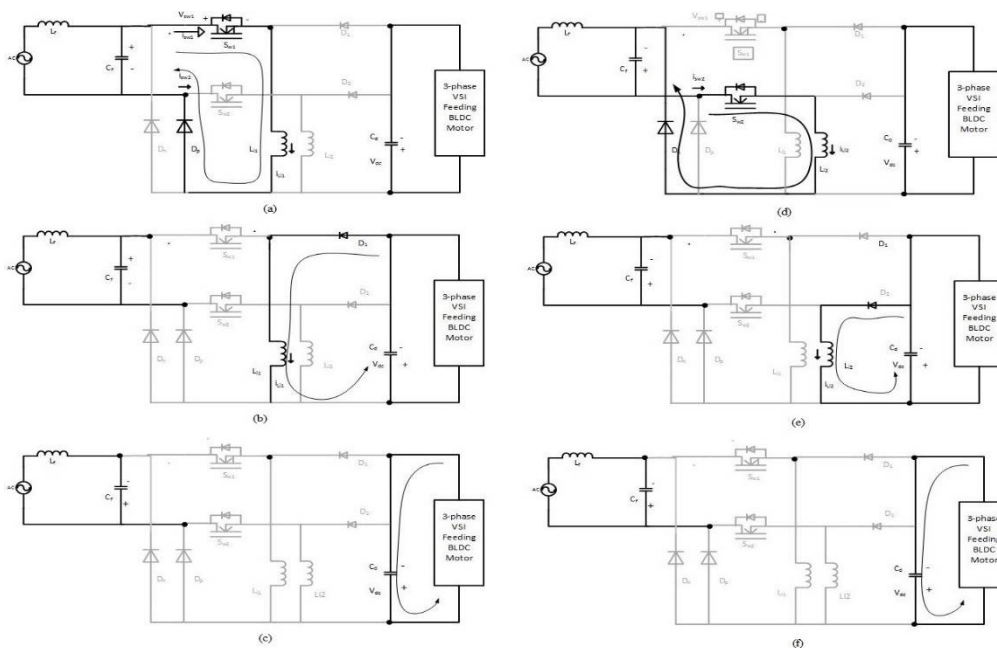


Fig. 2. Operation of the proposed converter in different modes (a)-(c) for a positive half cycle and (d)-(f) for a negative half cycle of the supply voltage

V. DESIGN OF PFC BL BUCK-BOOST CONVERTER

The proposed converter is designed to operate in DICM such that the current in inductors $Li1$ and $Li2$ become discontinuous in a switching period. The DC-link voltage is controlled from a minimum DC-link voltage ($Vdmin$) of 50 V to a maximum value ($Vdmax$) of 200 V. A PFC converter of 350 W (Po) is designed for the required BLDC motor of power rating 251W (complete specification is given in the Appendix).

For input voltage, Vs , with an rms value of 220 V, the average voltage can be calculated as [15]

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 10, October 2016

$$V_{in} = \frac{2\sqrt{2}V_s}{\pi} = \frac{2\sqrt{2} \times 220}{2} \approx 198V \quad (1)$$

The voltage conversion ratio for a buck-boost converter can be governed by following relation [16]

$$d = \frac{V_{dc}}{V_{dc} + V_{in}} \quad (2)$$

This gives us minimum and maximum duty ratio (d_{min} and d_{max}), corresponding to V_{dcmin} and V_{dcmax} , as 0.2016 and 0.5025, respectively.

a) Design of Input Inductors (L_{i1} and L_{i2})

To operate in critical conduction mode in the buck-boost converter, the value of inductance L_{ic1} , is given as [14]

$$L_{ic1} = \frac{R(1-d)^2}{2f_s} \quad (3)$$

where, R is the equivalent load resistance, d is the duty ratio, and f_s is the switching frequency.

For the converter to operate in DICM, the value of L_{ic1} is calculated at the worst duty ratio (d_{min}). At the minimum duty ratio (d_{min}) and minimum dc-link voltage (V_{dcmin}), the minimum power (P_{min}) is given as 90W (i.e., the load power is proportional to the speed, for constant torque). Hence, the value of inductance L_{icmin} , corresponding to V_{dcmin} , can be given as

$$L_{icmin} = \frac{V_{dcmin}^2 (1-d_{min})^2}{P_{min} 2f_s} = \frac{50^2 (1-0.2016)^2}{90 \times 2 \times 20000} = 442.67 \mu H \quad (4)$$

To achieve a discontinuous current conduction, the value of input inductors L_{i1} and L_{i2} must be selected lower than L_{icmin} [19]. Also, a low value of inductance increases the current stress on the PFC converter switch in DICM operation. Therefore, the switching frequency is selected as 20 kHz such that the losses and current stress of PFC converter switches are low, and it also meets the desired performance.

b) Design of DC Link Capacitor (C_d)

For the PFC operation, the supply current (i_s) is in phase with the supply voltage (v_s). Hence, the power input P_{in} is given as [16]

$$P_{in} = \sqrt{2}V_s \sin \omega t * \sqrt{2}I_s \sin \omega t = V_s I_s (1 - \cos 2\omega t) \quad (5)$$

where the latter term corresponds to the second-order harmonic, which is reflected in the dc link capacitor as

$$i_c(t) = -\frac{V_s I_s}{V_{dc}} \cos 2\omega t \quad (6)$$

The dc link voltage ripple corresponding to this capacitor current is given as [16]

$$\Delta V_{dc} = \frac{1}{C_d} \int i_c(t) dt = -\frac{I_d}{2\omega C_d} \sin 2\omega t \quad (7)$$

Here, $\sin(\omega t)$ is taken as 1 for a maximum value of voltage ripple at the dc link capacitor. Hence, (7) can be written as

$$C_d = \frac{I_d}{2\omega \Delta V_{dc}} \quad (8)$$

Now, the calculation of the value of the dc link capacitor is done for the designed value V_{dcdes} with permitted ripple in the dc link voltage (ΔV_{dc}) taken as 3% as

$$C_d = \frac{I_d}{2\omega \Delta V_{dc}} = \frac{P_o / V_{dcdes}}{2\omega \Delta V_{dc}} = \frac{350 / 100}{2 \times 314 \times 0.03 \times 100} = 1857.7 \mu F \quad (9)$$

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 10, October 2016

Therefore, the dc link capacitor with a nearest possible value of 2200 μF is selected for this application. A capacitor required for this application must have a large capacitance per unit volume due to the high value of the capacitance and its operation at relatively high current and low frequency switching (reflection of second-order harmonic). Therefore, electrolytic capacitors are best suited for this application.

c) Design of Filter Parameters (L_f and C_f)

A low-pass LC filter is used to avoid the reflection of higher order harmonics system such that it is not reflected in the supply current. The maximum value of filter capacitance is given as [18]

$$C_{\max} = \frac{I_{\text{peak}}}{\omega_L V_{\text{peak}}} \tan(\theta) = \frac{350}{220 \cdot 314 \times 220 \sqrt{2}} \tan(1^\circ) \quad (10)$$

$$= 410.95 \text{ nF}$$

where I_{peak} , V_{peak} , ω_L and θ represent the peak value of supply current, peak value of supply voltage, line frequency in radians per second, and displacement angle between the supply voltage and supply current, respectively. Hence, a value of C_f is taken as 330 nF. Now, the value of inductor L_f is calculated as follows.

The value of filter inductor is designed by considering the source impedance (L_s) of 4%–5% of the base impedance. Hence, the additional value of inductance required is given as

$$L_f = L_{\text{req}} + L_s \Rightarrow \frac{1}{4\pi^2 f_c^2 C_f} = L_{\text{req}} + 0.04 \left(\frac{1}{\omega_L} \right) \left(\frac{V_s^2}{P_o} \right) \quad (11)$$

$$L_{\text{req}} = \frac{1}{4\pi^2 \times 2000^2 \times 330 \times 10^{-9}} - 0.04 \left(\frac{1}{314} \right) \left(\frac{220^2}{350} \right) = 3.57 \text{ mH}$$

where f_c represents the cut off frequency of the designed filter which is selected as [20]

$$f_L < f_c < f_{\text{sw}} \quad (12)$$

Hence, a value of f_c is taken as $f_{\text{sw}} / 10$.

Finally, a low-pass filter with inductor and capacitor of 4 mH and 450 nF is selected for this particular application.

VI. CONTROL OF PFC BL BUCK-BOOST CONVERTER FED BLDC MOTOR DRIVE

The control of the proposed PFC based BL-buck-boost converter fed BLDC motor drive is divided into two parts which includes the control of the PFC converter for dc link voltage control and the electronic commutation of BLDC motor.

A) Control of the Front-End PFC Converter

A single voltage sensor is required for controlling the dc link voltage for speed control of BLDC motor, and inherent PFC is achieved at the ac mains. A reference dc link voltage V_{dc}^* is generated as

$$V_{dc}^* = k_v \omega^* \quad (13)$$

where k_v denotes the motor's voltage constant and ω^* is the reference speed.

The voltage error generator compares this reference dc link voltage (V_{dc}^*) with the sensed dc link voltage (V_{dc}) to generate an error voltage (V_e), which is given as

$$V_e(k) = V_{dc}^*(k) - V_{dc}(k) \quad (14)$$

where 'k' represents the kth sampling instance.

This error voltage V_e is given to a voltage proportional-integral (PI) controller to generate a controlled output voltage V_{cc} , which is expressed as

$$V_{cc}(k) = V_{cc}(k-1) + k_p \{V_e(k) - V_e(k-1)\} + k_i V_e(k) \quad (15)$$

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 10, October 2016

where k_p and k_i are the proportional and integral gains of the PI controller, respectively. Finally, the PWM signals are generated by comparing the output of PI controller (V_{cc}) with the high-frequency sawtooth signal (m_d), which are given

$$\begin{aligned}
 \text{For } v_s > 0; & \quad \text{if } m_d < V_{cc} \text{ then } S_{w1} = 'ON' \\
 & \quad \text{if } m_d \geq V_{cc} \text{ then } S_{w1} = 'OFF' \\
 \\
 \text{For } v_s < 0; & \quad \text{if } m_d < V_{cc} \text{ then } S_{w2} = 'ON' \\
 & \quad \text{if } m_d \geq V_{cc} \text{ then } S_{w2} = 'OFF'
 \end{aligned} \tag{16}$$

where S_{w1} and S_{w2} represent the gate signals to PFC switches of the PFC converter respectively.

B) Control of BLDC Motor

The electronic commutation of BLDC motor is achieved by the use of hall-effect position sensors which are used to sense the rotor position. A standard commutation technique is used for this trapezoidal back electromotive force (EMF) BLDC motor, where only two stator phases conduct at any given instant of time.

$\theta (^\circ)$	Hall Signals			Switching States					
	Ha	Hb	Hc	S1	S2	S3	S4	S5	S6
NA	0	0	0	0	0	0	0	0	0
0-60	0	0	1	1	0	0	0	0	1
60-120	0	1	0	0	1	1	0	0	0
120-180	0	1	1	0	0	1	0	0	1
180-240	1	0	0	0	0	0	1	1	0
240-300	1	0	1	1	0	0	1	0	0
300-360	1	1	0	0	1	0	0	1	0
NA	1	1	1	0	0	0	0	0	0

Table I. Switching states for achieving electronic commutation of BLDC motor based on hall-effect position signals

VII. SIMULATED PERFORMANCE OF THE PROPOSED BLDC MOTOR DRIVE

The performance of the proposed buck-boost converter fed BLDC motor drive is simulated in MATLAB/Simulink environment using the Sim-Power-System toolbox as shown in Fig. 3. Moreover, power quality indices such as power factor (PF) and THD of supply current are analyzed for determining power quality at ac mains.

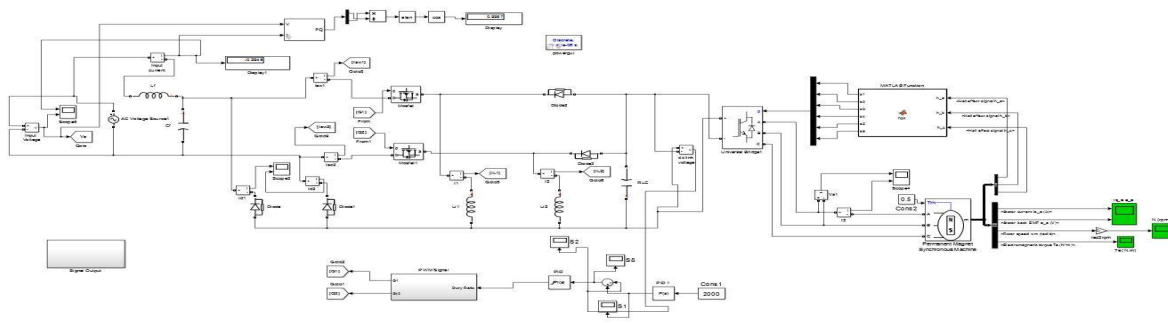


Fig. 3. Simulated Diagram of the proposed BL Buck-Boost Converter fed BLDC motor drive

A. STEADY-STATE PERFORMANCE

The steady-state behavior of the proposed BLDC motor drive for cycles at rated condition (rated dc link voltage of 200 V) is shown in Fig. 8. The performance of the proposed BLDC motor drive at speed control by varying dc link voltage from 50 to 200 V and varying supply voltage is tabulated in Table II and III respectively.

V_{dc} (V)	N(rpm)	THD of I_s (%)	PF	I_s (A)
50	397	8.01	0.9602	0.382
70	620	7.45	0.9687	0.551
90	840	4.61	0.9875	0.698
110	1059	4.24	0.9909	0.813
130	1276	3.88	0.9920	1.019
150	1480	3.85	0.9960	1.192
170	1695	3.78	0.9961	1.298
190	1898	3.69	0.9982	1.499
200	1972	3.58	0.9989	1.523

Table II. Performance of PFC Buck-Boost Converter Fed BLDC motor drive under speed control

V_s (V)	I_s (A)	THD of I_s (%)	PF
90	4.012	1.72	0.9901
110	3.998	1.86	0.992
130	3.014	2.02	0.992
150	2.891	2.34	0.994
170	2.521	3.15	0.998
190	2.021	3.10	0.993
210	1.982	3.53	0.9981
230	1.562	4.23	0.997
250	1.534	4.76	0.998
270	1.523	4.62	0.994

Table III. Performance of BL Buck-Boost Converter fed BLDC motor drive under varying supply voltage

The harmonic spectra of the supply current at rated conditions, i.e., dc link voltages of 200 and 50V , is also shown in Fig. 4, which shows that the THD of supply current obtained is under the acceptable limits of IEC 61000-3-2

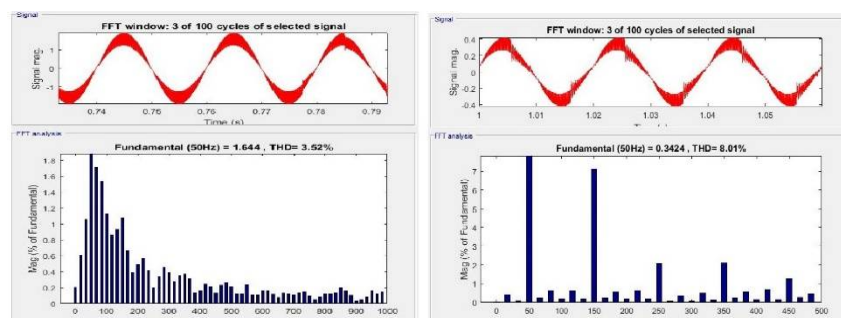


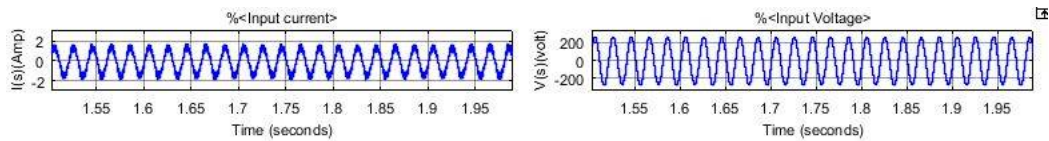
Fig 4. Harmonic spectra of supply current at rated supply voltage and rated loading on BLDC for a DC link voltage of 200V and 50V

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

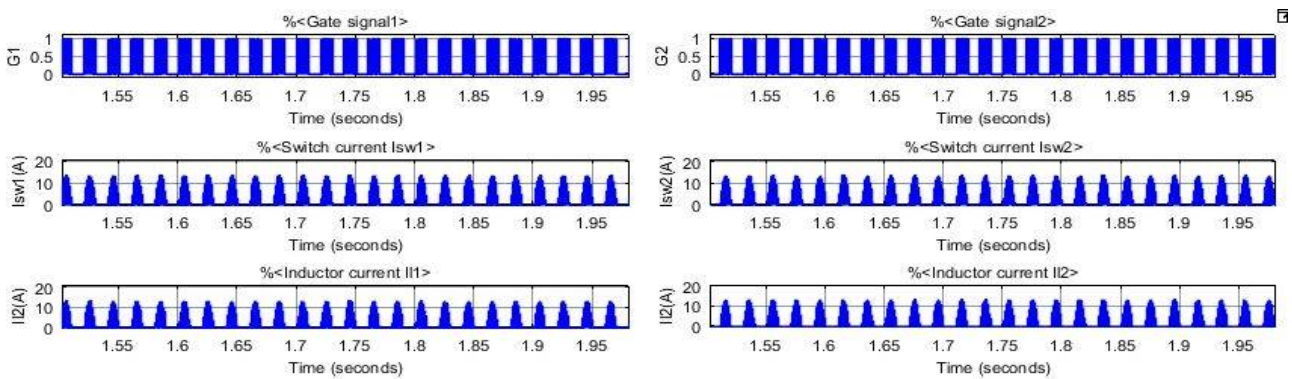
Vol. 5, Issue 10, October 2016

The parameters associated with the BLDC motor such as speed (N), electromagnetic torque (T_e), and stator current (i_a) are analysed for the proper functioning of the BLDC motor and the parameters such as supply voltage (V_s), supply current (i_s), inductor's currents (i_{Li1} , i_{Li2}), and switch currents (i_{sw1} , i_{sw2}) of the PFC BL buck–boost converter are evaluated to demonstrate its proper functioning as shown in Fig.5 (a)-(c)

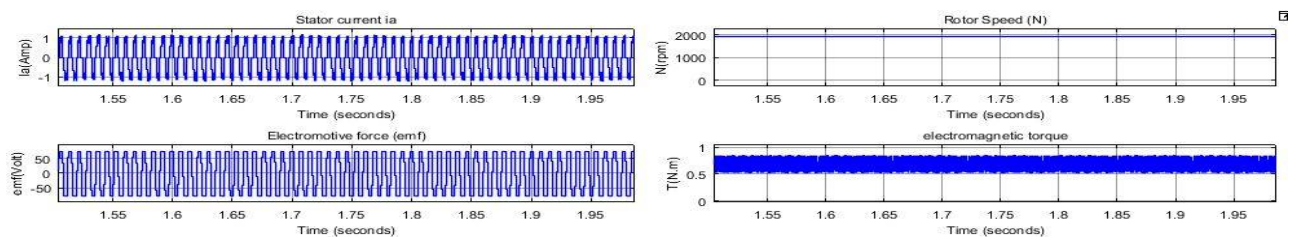


(a)

The DICM operation of the BL buck–boost converter is confirmed by the obtained discontinuous inductor currents (i_{Li1} and i_{Li2}) which can be seen in the Fig 5. (b), the waveform of inductor currents.



(b)



(c)

Fig. 5 Steady-state performance of (a) input supply current and supply voltage, (b) gate signal, switch current and inductor current, and (c) stator current, emf, rotor speed and electromagnetic torque

VI. CONCLUSION

A buck-boost converter-fed BLDC motor drive has been proposed for targeting low-power household appliances. A variable dc link voltage of VSI feeding BLDC motor has been used for controlling the speed. With this PFC converter, three-phase VSI has been operated in low frequency switching mode with reduced switching losses. A front-end converter operating in DICM has been used for dc link voltage control and with PFC at ac mains. Performance of proposed drive has been found quite satisfactory for speed control over a wide range. The obtained power quality indices have been found within the limits of IEC 61000-3-2.

International Journal of Innovative Research in Science, Engineering and Technology

(An ISO 3297: 2007 Certified Organization)

Vol. 5, Issue 10, October 2016

APPENDIX

BLDC Motor Rating: four poles, P_{rated} (rated power) = 251.32 W, V_{rated} (rated dc link voltage) = 200 V, T_{rated} (rated torque) = 1.2 N · m, ω_{rated} (rated speed) = 2000 r/min, K_b (back EMF constant) = 78 V/kr/min, K_t (torque constant) = 0.74 N · m/A, R_{ph} (phase resistance) = 14.56 Ω , L_{ph} (phase inductance) = 25.71 mH, and J (moment of inertia) = 1.3×10^{-4} N·m/A². *Controller Gains:* $k_p = 0.1$, $k_i = 0.01$.

REFERENCES

- [1] C. L. Xia, *Permanent Magnet Brushless DC Motor Drives and Controls*. Hoboken, NJ, USA: Wiley, 2012.
- [2] P. Pillay and R. Krishnan, "Modeling of permanent magnet motor drives," *IEEE Trans. Ind. Electron.*, vol. 35, no. 4, pp. 537–541, Nov. 1988.
- [3] Y. Chen, C. Chiu, Y. Jhang, Z. Tang, and R. Liang, "A driver for the singlephase brushless dc fan motor with hybrid winding structure," *IEEE Trans. Ind. Electron.*, vol. 60, no. 10, pp. 4369–4375, Oct. 2013.
- [4] X. Huang, A. Goodman, C. Gerada, Y. Fang, and Q. Lu, "A single sided matrix converter drive for a brushless dc motor in aerospace applications," *IEEE Trans. Ind. Electron.*, vol. 59, no. 9, pp. 3542–3552, Sep. 2012.
- [5] J. Moreno, M. E. Ortuzar, and J. W. Dixon, "Energy-management system for a hybrid electric vehicle, using ultra capacitors and neural networks," *IEEE Trans. Ind. Electron.*, vol. 53, no. 2, pp. 614–623, Apr. 2006.
- [6] T. Kenjo and S. Nagamori, *Permanent Magnet Brushless DC Motors*. Oxford, U.K.: Clarendon Press, 1985.
- [7] J. R. Handershot and T. J. E Miller, *Design of Brushless Permanent Magnet Motors*. Oxford, U.K.: Clarendon Press, 2010.
- [8] S. Singh and B. Singh, "A voltage-controlled PFC CUK converter based PMBLDCM drive for air-conditioners," *IEEE Trans. Ind. Appl.*, vol. 48, no. 2, pp. 832–838, Mar./Apr. 2012.
- [9] *Limits for Harmonic Current Emissions (Equipment input current ≤ 16 A Per Phase)*, Int. Std. IEC 61000-3-2, 2000
- [10] B. Singh *et al.*, "A review of single-phase improved power quality ac-dcconverters," *IEEE Trans. Ind. Electron.*, vol. 50, no. 5, pp. 962–981, Oct. 2003.
- [11] B. Singh, S. Singh, A. Chandra, and K. Al-Haddad, "Comprehensive study of single-phase ac-dc power factor corrected converters with high frequency isolation," *IEEE Trans. Ind. Informat.*, vol. 7, no. 4, pp. 540–556, Nov. 2011.
- [12] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, "A review of single-phase improved power quality ACDC converters," *IEEE Trans. Ind. Electron.*, vol. 50, no. 5, pp. 962–981, Oct. 2003.
- [13] B. Singh, S. Singh, A. Chandra, and K. Al-Haddad, "Comprehensive study of single-phase AC-DC power factor corrected converters with high frequency isolation," *IEEE Trans. Ind. Inf.*, vol. 7, no. 4, pp. 540–556, Nov. 2011
- [14] A. Emadi, A. Khaligh, Z. Nie, and Y. J. Lee, *Integrated Power Electronic Converters and Digital Control*. Boca Raton, FL, USA: CRC Press, 2009.
- [15] D. S. L. Simonetti, J. Sebastian, F. S. dos Reis, and J. Uceda, "Design criteria for SEPIC and Cuk converters as power factor pre-regulators in discontinuous conduction mode," in *Proc. Int. Electron. Motion Control Conf.*, 1992, vol. 1, pp. 283–288.
- [16] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications and Design*. Hoboken, NJ, USA: Wiley, 2003.
- [17] D. S. L. Simonetti, J. Sebastian, and J. Uceda, "The discontinuous conduction mode SEPIC and Cuk power actor preregulators: Analysis and design," *IEEE Trans. Ind. Electron.*, vol. 44, no. 5, pp. 630–637, Oct. 1997.
- [18] V. Vlatkovic, D. Borojevic, and F. C. Lee, "Input filter design for power factor correction circuits," *IEEE Trans. Power Electron.*, vol. 11, no. 1, pp. 199–205, Jan. 1996
- [19] B. Singh, S. Singh, A. Chandra, and K. Al-Haddad, "Comprehensive study of single-phase ac-dc power factor corrected converters with high-frequency isolation," *IEEE Trans. Ind. Informat.*, vol. 7, no. 4, pp. 540–556, Nov. 2011.
- [20] S. Singh and B. Singh, "Power quality improved PMBLDCM drivefor adjustable speed application with reduced sensor buck-boost PFCconverter," in *Proc. 4th ICETET*, Nov. 18–20, 2011, pp. 180–184.
- [21] Y. Jang and M. M. Jovanovi'c, "Bridgeless high-power-factor buck converter," *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 602–611, Feb. 2011.
- [22] L. Huber, Y. Jang, and M. M. Jovanovi'c, "Performance evaluation ofbridgeless PFC boost rectifiers," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1381–1390, May 2008.
- [23] A. A. Fardoun, E. H. Ismail, M. A. Al-Saffar, and A. J. Sabzali, "New'real' bridgeless high efficiency ac-dc converter," in *Proc. 27th Annu. IEEE APEC Expo.*, Feb. 5–9, 2012, pp. 317–323.
W. Wei, L. Hongpeng, J. Shigong, and X. Dianguo, "A novel bridgelessbuck-boost PFC converter," in *IEEE PESC/IEEE Power Electron. Spec.aConf.*, Jun. 15–19, 2008, pp. 1304–1308.