

Design of Decimal to BCD Code Converter using Reversible logic and QCA

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ABSTRACT: In the field of Quantum computation, the reversible logic and nanotechnology has gathered a lot of attention of researcher's in the recent years due to its low power dissipation quality. Quantum computing has been a guiding light for Bio-informatics, Nanotechnology, optical information computing, low power CMOS design, DNA computing and low power VLSI. In digital system, Code converters are considered to be very essential component and are needed day in and out. Generally, the encoders are utilized in converting a $2n$ bit number to n bit number. In this paper, an optimized design of Decimal to BCD code converter using a new proposed reversible gate i.e. FR gate is proposed. The proposed design offers an improvement of 26.67% and 54% over the existing design in terms of its garbage outputs & Quantum cost respectively. The Proposed gate and Decimal to BCD converter are finally designed & successfully tested using the simulations obtained from QCA designer.

KEYWORDS: Decimal to BCD encoder, Nanoscale reversible gate, Quantum Computing, Quantum-dot Cellular Automata (QCA), Reversible logic.

I. INTRODUCTION

In the recent years, the reversible logic has gained lot of researcher's attention due to its ability of minimizing power dissipation which is the main specification for low power VLSI design. The reversible logic has enormous applications in emerging technologies such as Bio-informatics, Nanotechnology, DNA computing, quantum dot cellular automata, optical computing, optical information processing, quantum computing, etc. In modern circuit designs, researcher's primary concern is to minimize energy dissipation.

R. Landauer proposed that $KT \ln 2$ i.e. approx 2.9×10^{-21} joules of heat energy dissipates for every irreversible operation at the room temperature i.e 300K which is a small value but in the complete system it cannot be neglected [1,2]. This energy dissipates when one bit of data is lost during the circuit operation which reduces the lifetime and overall performance of the circuit. Thereafter Gordon E. Moore predicted that number of components in the circuit of an integrated circuit will become double biennially [3]. C. Bennett asserted that $KT \ln 2$ joules of energy can be avoided to dissipate if the circuits designed are reversible [4].

In addition to proposing the modified designs of reversible logic based circuits, there exist several studies that suggest implementing these designs on QCA (Quantum dot-cellular automata. QCA is a novel nanotechnology that can suppress the complementary metal-oxide semiconductor (CMOS) technology [5] and has potential applications due to its ultra low power consumption, extremely small feature sizes, higher switching frequency, faster speed and higher scale integration [6]. QCA interacts with magnetic or electric field polarization to encode the required information [7].

A.N. Nagamani et al. [8] provide a possible approach to the designs of reversible binary and BCD adders. The proposed adder design is optimized for quantum cost, delay and Gate count. Jadav Chandra Das et al.[5] propounds the design of reversible binary to grey and grey to binary code converter utilizing Feynman gate using QCA. The presented design can be utilized in computer communication to realize the nano architecture which will consume low power. Ali Newaz Bahar et al. [9] proposed a number of reversible logic gates using QCA technology. The proposed designs are compared with CMOS technology and shows reduction in size which is up to 233 times.

Vandana Shukla et al. [10] propounded a design of decimal to BCD encoder using reversible logic gates. The circuit is optimized by minimizing some performance parameters such as number of reversible logic gates, quantum cost and

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garbage outputs of the circuit. Manjula Gandhi et al. [11] presented a modular method to design reversible circuits for Code Converter and Binary Incrementer. The optimized design is evaluated in terms of quantum cost, number of garbage output and number of ancilla bits. Rakshith Saligram et al. [12] propounded a reversible 5421 to binary code converter. The author proposed a new reversible gate, known as MCL. The new design is optimized by reducing the garbage outputs, number of number of gates and number of constant inputs. These designs can further be optimized by reducing number of garbage outputs and Quantum cost.

II. REVERSIBLE LOGIC

In the reversible logic, to prevent the loss of bit in logical operation, the number of inputs & outputs are made equal. Reversible gate is an $n \times n$ gate in which outputs can regenerate inputs, where n is number of inputs or outputs. To minimize the power dissipation, reversible logic gates are used instead of irreversible logic gates. In reversible gates, inputs & outputs are mapped one to one which will conserve energy as there will not be a loss of any bit [13-18].

Reversible logic gates have following characteristics:

1. Total number of inputs and total number of outputs must be identical and outputs can regenerate inputs.
2. Fan-out should be avoided i.e. output should be connected to only one input at a time.
3. Prohibition on closed loop feedback.

In reversible logic garbage outputs are the outputs that are only needed to achieve reversibility in the design and are unused outputs. The total cost of number of primitive gates that are used to form a quantum circuit is known as Quantum Cost. Delay in a reversible logic circuit is maximum number of gates that an input has to elapse or encountered to reach an output terminal. Various reversible gates are designed so far, some basic reversible gates are described below:

1. **NOT gate:** This is a 1×1 reversible gate (as shown in figure 1) and resembles the conventional NOT gate as both the quantum NOT gate and conventional NOT gate satisfy the above criteria for reversibility while the function remains the same of inverting the input supplied to it.



Fig 1: Quantum Representation of NOT Gate

2. **Feynman gate:** This is a 2×2 reversible gate (as shown in figure 2), where 2×2 means 2 inputs and 2 outputs. It is also known as CNOT (Controlled NOT) gate. It is extensively used for fan-out functions as copying gate. The quantum cost of Feynman gate [19] given to be 1.

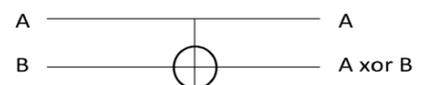


Fig 2: Quantum Representation of Feynman Gate

3. **Toffoli Gate:** This gate is also known as CCNOT gate (as shown in figure 3), is a 3×3 universal reversible gate which requires its two control inputs to be asserted to perform the NOT operation on the third input. The gate is also used as reversible AND gate if control I/P is reset to '0' and a NAND operation if control I/P is set to '1'. The quantum cost of Toffoli gate [20] is 5.

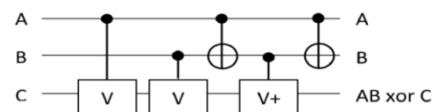


Fig 3: Quantum Representation of Toffoli Gate

4. **Peres gate:** This gate can be said as a variant of the above described Toffoli gate. The Quantum Cost of Peres gate [21] (as shown in figure 4) is affirmed to be 4. Peres gate is widely used as a half adder and a dual-input AND gate.

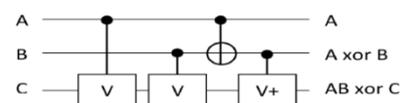


Fig 4: Quantum Representation of Peres Gate

5. **Fredkin Gate:** This is a 3×3 universal reversible gate known (as shown in figure 5) for its controlled swap operation. Controlled Swap is the operation in which inputs interchange its position when the control input is high. The Quantum cost of fredkin gate [22] is 5.

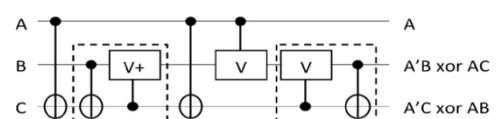


Fig 5: Quantum Representation of Fredkin Gate

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6. **BJN gate:** This is a 3x3 reversible gate designed by Vandana Shukla et al. with a quantum cost of 5 [10]. It's block diagram is shown in the figure 6. The output P and Q is same as input.

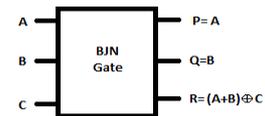


Fig. 6: Block diagram of BJT gate

III. RESEARCH METHODOLOGY

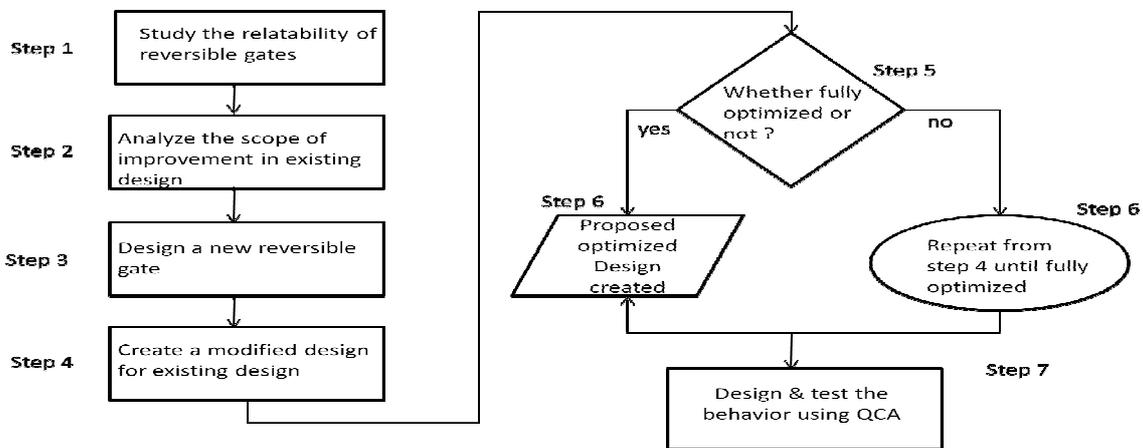


Figure 7: Flowchart of Research Methodology

The research methodology of the work is described by the steps presented graphically in Figure No. 7 below. The figure shows that the design is optimized till the fullest. Further the design is verified using simulation tool i.e. QCA.

Step 1: Relatability of reversible gates

There are many gates like NOT gate, Feynman gate, Toffoli gate, peres gate, Fredkin gate, BJT gate, etc that can be used to create a reversible logic but in proposed design only Feynman and BJT are of our relevance due to the need of XOR operation in the design. The table 1 summarizes the relevant gates that can be used in our design.

Table 1: Relatable Gates

Gates	Relatable Or Not ?
NOT	×
Feynmann	✓
Toffoli	×
Peres	×
Fredkin	×
BJN	✓

Step 2: Analysis of Existing Design

The existing Decimal to BCD Encoder [10] designed using BJT gate offers a Quantum cost of 50 and Garbage Output of 15. The subsequent stages of research methodology will be used to optimize this design further.

Step 3: Design of New Reversible Gate i.e FR Gate

The FR gate is a 3x3 reversible gate which is optimized by reducing quantum cost as compared to the existing gate that is used by the Vandana Shukla et al. in their Decimal to BCD encoder design. The quantum representation of proposed gate is shown in the figure 8.

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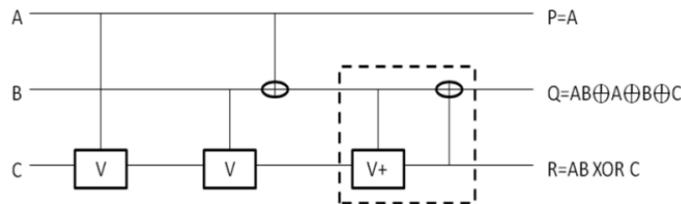


Figure 8: Quantum Representation of FR Gate

Further minimization of output Q in figure 8 can be done as follows,

$$\begin{aligned}
 Q &= AB \oplus C \oplus A \oplus B \\
 Q &= (AB) \oplus A \oplus B \oplus C \\
 Q &= [(AB)'A + ABA'] \oplus B \oplus C \\
 Q &= [(A'+B')A + 0] \oplus B \oplus C \\
 Q &= [AA' + AB' + \oplus B] \oplus C \\
 Q &= [0 + (AB')'B + AB'B'] \oplus C \\
 Q &= [(A'+B'')B + AB'] \oplus C \\
 Q &= [A'B + B''B + AB'] \oplus C \\
 Q &= [A'B + B + AB'] \oplus C \\
 Q &= [B(1+A') + AB'] \oplus C \\
 Q &= (B + AB') \oplus C \\
 Q &= (A+B) \oplus C \\
 \text{Hence, } (AB \oplus C \oplus A \oplus B) &= (A+B) \oplus C
 \end{aligned}$$

Table 2: Truth table showing $B + AB' = A + B$

<u>A</u>	<u>B</u>	<u>B+AB'</u>	<u>A+B</u>
0	0	0	0
0	1	1	1
1	0	1	1
1	1	1	1

After minimization of the output Q, as verified using the results presented in Table 2, the Quantum representation of proposed FR gate is modified. The table 2 describes that the value of the expression $B + AB'$ is equal to $A + B$ as shown in the truth table. After minimization of the expression the quantum representation of FR gate is as shown in the figure 9. Now the output Q becomes $(A+B) \oplus C$.

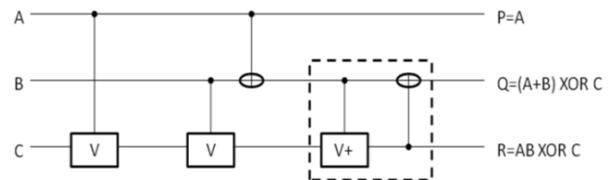


Figure 9: Minimized Quantum Representation of FR Gate

The quantum cost of BJJ Gate is 5, whereas of FR gate is 4.

Whereas, the Feynman gate is simply an XOR gate with 1 quantum cost, but if used individually, it may increase garbage output in circuit & number of gates. Therefore, the use of FR gate in place of BJJ & Feynman is recommended.

Further, the universal nature of FR gate is verified using the truth table presented in Table 3. The table describes that FR gate can behave as OR & AND gate if input $C=0$ and will behave as NOR & NAND if $C=1$. Also, when $B=1$, output Q will act as NOT Gate and R as XOR Gate.

Table 3: Truth table showing working of FR gate

INPUT			OUTPUT			REMARKS
A	B	C	P=A	$Q=(A+B) \oplus C$	$R=AB \oplus C$	
0	0	0	0	0	0	Output Q behaves as OR Gate, and R as AND Gate
0	1	0	0	1	0	
1	0	0	1	1	0	
1	1	0	1	1	1	
0	0	1	0	1	1	Output Q behaves as NOR Gate and R as NAND Gate
0	1	1	0	0	1	
1	0	1	1	0	1	
1	1	1	1	0	0	

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Step 4: Proposed Design 1

The existing design [10] is modified by replacing BJN gates (Quantum cost 5) with FR gate (Quantum cost 4) as shown in figure 10. Thus the modified design optimized in terms of quantum cost. The gates are connected such that minimum gates are employed while designing the converter.

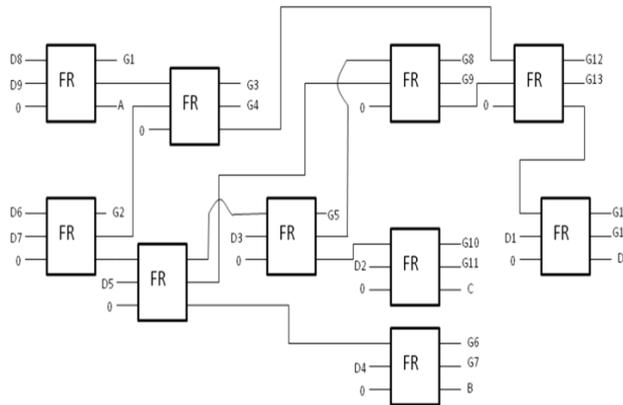


Figure 10: Modified Design-I for Decimal to BCD converter

It is further observed that this Design-I (presented in figure 10) can further be improved by making pairs of inputs (as shown below) and thus the design-I is not considered as the final optimized design.

Step 5: Final Optimized Design

To make the design-I optimized further, following pairs of inputs are combined:

$$\begin{aligned} B0 &= D1 + D3 + D5 + D7 + D9 & B0 &= D1 + D3 + D5 + D7 + D9 \\ B1 &= D2 + D3 + D6 + D7 & B1 &= D2 + D3 + D6 + D7 \\ B2 &= D4 + D5 + D6 + D7 & B2 &= D4 + D5 + D6 + D7 \\ B3 &= D8 + D9 & B3 &= D8 + D9 \end{aligned}$$

$$\begin{aligned} B0 &= D1 + D3 + D5 + D7 + D9 & B0 &= D1 + D3 + D5 + D7 + D9 \\ B1 &= D2 + D3 + D6 + D7 & B1 &= D2 + D3 + D6 + D7 \\ B2 &= D4 + D5 + D6 + D7 & B2 &= D4 + D5 + D6 + D7 \\ B3 &= D8 + D9 & B3 &= D8 + D9 \end{aligned}$$

Along with this, it is pertinent to note that the Decimal to BCD encoder has certain conventions; one of them is to activate only one input at any given time. So to ensure the same, XOR gate (QC=1) shall be used in place of OR gate (QC=4), which will further reduce the quantum cost

to a much extent. The final design is shown in figure 11 which is fully optimized. Here in the design decimal input signals are fed to the FR gates and XOR gates. The Feynman is also used to make a replica of D6+D7 output which helps in optimization of the design. This design is more efficient in terms of Quantum cost, Ancillary inputs and Garbage Outputs as compare to the existing designs.

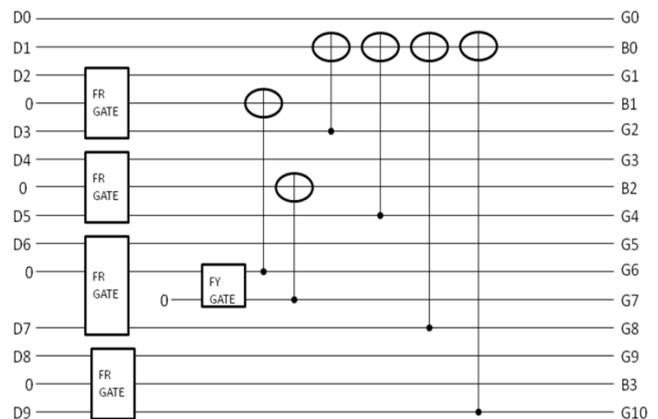


Figure 11: Optimized Design of Decimal to BCD converter

Step 6: As no further optimization scope is there in the final optimized design, the proposed design is to be designed & tested via QCA implementation.

Step 7: QCA Design

In QCA, binary information is encoded and processed by arrays of coupled quantum dots. A quantum cell is like

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square in which four dots are positioned at the corners [8]. Figure 12 shows the logical representation of quantum cell, in which logic 1 is represented by polarization $P = +1$ and logic 0 by $P = -1$ [6, 23].

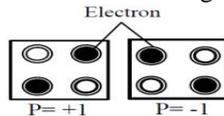


Figure 12: Quantum Cell

In the cell electrons cannot travel outside the boundaries of the cell but can tunnel within a cell from dot to dot. A horizontal row of number of QCA cells is called QCA wire as shown in Figure 13. To propagate the binary signal between adjacent cells electrostatic interactions are used.

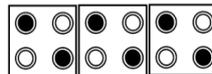


Figure 13: QCA wire

The basic logic element in QCA is the Inverter Gate, as shown in figure 14, which is used to invert the signal. In inverter gate the signal comes inside from the left side and then the signal splits into the two wires which are parallel to each other. At convergence of the two the signal is inverted. QCA Majority Voter i.e. MV (as shown in figure 15) is one of the basic fundamental elements of the QCA having 3 input gates and five cells. MV gate has three input cells i.e. A, B, and C and a cell in the center which is called device cell [24] and provide the output i.e. $Maj(A, B, C) = AB+BC+CA$.

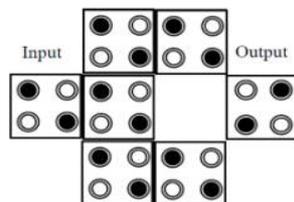


Figure 14: QCA inverter gate

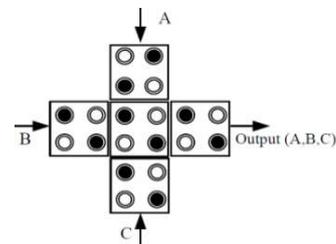


Figure 15: QCA majority gate

The Proposed Gate i.e. FR Gate layout has been designed in the QCA Designer version 2.0.3 tool as shown in Figure 16. The FR gate layout has been designed using 160 QCA cells and the area covered is 0.19 um^2 . The simulation result of proposed gate is shown in Figure 17. The designed layout is verified by the simulation result of the FR gate.

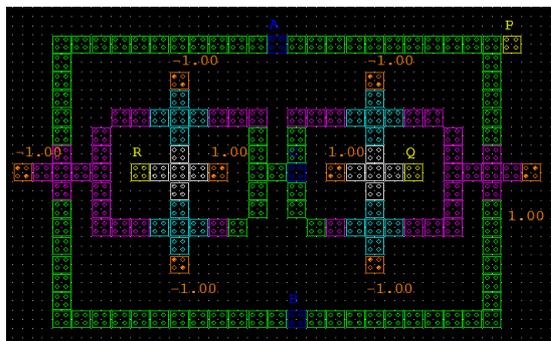


Figure 16: QCA design of FR gate



Figure 17: Simulation result of FR gate design

The Decimal to BCD Code Converter layout is designed by using 147 QCA cells and the area covered by the layout is 0.31 um^2 . The layout of the Decimal to BCD code converter is shown in the Figure 18. To verify the layout

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of the code converter, simulation result of the Code Converter is shown in figure 19. The result verified our design layout.

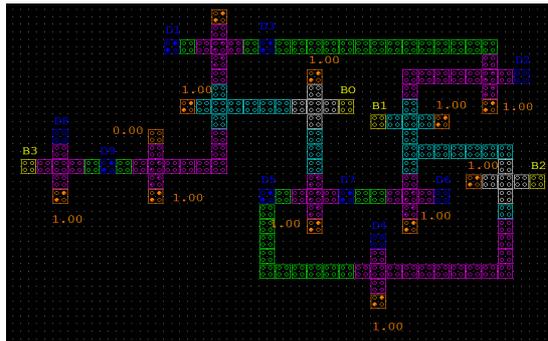


Figure 18: QCA design of Decimal to BCD converter

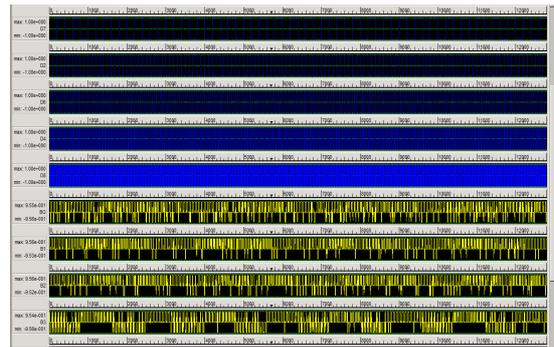


Figure 19: Simulation result of Decimal to BCD converter

IV. RESULTS & DISCUSSIONS

Decimal to BCD code converter is designed using reversible logic and the design is analyzed on the basis of some performance parameters such as quantum cost, number of reversible gates and number of garbage outputs of the proposed circuit in comparison to the existing designs [10]. The comparative analysis of Decimal to BCD code converter using reversible logic is shown in the table 5 below:

Table 5: Comparative Analysis of the Decimal to BCD code converter using reversible logic

Performance Parameters	Total Reversible Gates	Total Garbage Outputs	Quantum Cost	Ancillary Input
Existing Design-I of Decimal to BCD converter (As per base paper, [10])	14	15	Unknown	6
Existing Design-II of Decimal to BCD converter using BJN Gate (As per base paper, [10])	10	15	50	10
Proposed Design of Decimal to BCD converter (using FR Gate)	11	11	23	5

It is observed that the proposed design of Decimal to BCD converter is much better in comparison to the existing designs in terms of its garbage outputs & Quantum cost. It provides an improvement of 26.67%, 54% and 50% improvement over the garbage outputs, Quantum cost and Ancillary inputs.

V. CONCLUSION AND FUTURE WORK

The reversible logic circuits are designed to minimize the power dissipation which ultimately increase the lifetime and speed of the circuit. The researchers are attracted towards reversible logic as it has enormous applications in the emerging technologies. The proposed FR gate has successfully optimized the Decimal to BCD Code Converter and it the same has been verified using QCA. It is therefore suggested that the FR gate can be further utilized to optimize the performance of other converters.

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REFERENCES

- [1] R. Landauer, "Irreversibility and Heat Generation in the Computational Process", IBM Journal of Research and Development, 5, pp.183-191, 1961.
- [2] M.A. Nielsen, I.L. Chuang, "Quantum Computation and Quantum Information", Cambridge University Press p. 13, Cambridge, 2000.
- [3] Gordon E. Moore, "Cramming More Components onto Integrated Circuits," Electronics, pp. 114-117, April 19, 1965.
- [4] C.H. Bennett, "Logical reversibility of Computation", IBM J. Research and Development, pp.525-532, November 1973.
- [5] Jadav Chandra Das and Debashis De, "Reversible Binary to Grey and Grey to Binary Code Converter using QCA" iete journal of research, vol 61, june 2015.
- [6] Lent, C. S., & Tougaw, P. D., "A device architecture for computing with quantum dots", Proceedings of the IEEE, 85(4), 541-557, 1997.
- [7] Angona Sarker, Ali Newaz Bahar, Provash Kumar Biswas, Monir Morshed, "A Novel Presentation Of Peres Gate (Pg) In Quantum-dot Cellular Automata(qca)," European Scientific Journal edition vol.10, July 2014.
- [8] A.N. Nagamani, Nikhil J. Reddy and Vinod Kumar Agrawal, "Design and Analysis of Reversible Binary and BCD Adders", Microelectronics, Electromagnetics and Telecommunications Volume 372 Electrical Engineering Springer India 2016.
- [9] Ali Newaz Bahar, Sajjad Waheed and Nazir Hossain, "A new approach of presenting reversible logic gate in nanoscale," SpringerPlus, 2015.
- [10] Vandana Shukla1, O. P. Singh1, G. R. Mishra1, R. K. Tiwari, "A Novel Approach to Design Decimal to BCD Encoder with Reversible Logic", Proceedings of IEEE, 2014.
- [11] Manjula Gandhi S1, Devishree, Venkatesh, Sathish Mohan, "Design of Reversible Circuits for Code Converter and Binary Incrementer" Int. Journal of Information Technology & Mechanical Engineering – IJITME, 2014.
- [12] Rakshith Saligram Rakshith T.R, "Novel Code Converter Employing Reversible logic," International Journal of Computer Applications (0975 – 8887), 2012.
- [13] M.P Frank, "Introduction to Reversible Computing Motivation, Progress and Challenges", Proceedings of the 2nd Conference on Computing Frontiers, pp. 385-390, 2005.
- [14] A. P. Hatkar, A. A. Hatkar, N. P. Narkhede, "ASIC Design of Reversible Multiplier Circuit", International Conference on Electronic Systems, Signal Processing and Computing Technologies (ICESC), IEEE, pp. 47-52, 2014.
- [15] H.M.H. Babu, L. Jamal, N. Saleheen, "An efficient approach for designing a reversible fault tolerant n-bit carry look-ahead adder", IEEE 26th International SOC Conference (SOCC), pp. 98-103, 2013.
- [16] H. P. Shukla, A. G. Rao, P. Mall, "Design of low power comparator circuit based on reversible logic technology", 1st International Conference on Emerging Trends and Applications in Computer Science (ICETACS), IEEE, pp. 6-11, 2013.
- [17] H. Thapliyal, N. Ranganathan, S. Kotiyal, "Design of Testable Reversible Sequential Circuits", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 21, Issue 7, pp. 1201-1209, 2013.
- [18] M. Morrison, N. Ranganathan, "A novel optimization method for reversible logic circuit minimization", IEEE Computer Society Annual symposium on VLSI (ISVLSI), pp.182-187, 2013.
- [19] R. Feynman, "Quantum Mechanical Computers", Optic News, Vol 11, pp 11-20 1985.
- [20] T. Toffoli, "Reversible Computing" Tech memo MIT/LCS/TM-151, MIT Lab for Computer Science 1980.
- [21] Peres, "Reversible Logic and Quantum Computers", Physical review A, 32:3266-3276, 1985.
- [22] E. Fredkin and T. Toffoli, "Conservative Logic", Int'l J. Theoretical Physics Vol 21, pp.219-253, 1982.
- [23] Meurer, B., Heitmann, D., & Ploog, K., "Excitation of three-dimensional quantum dots", Physical Review B, 48(15), 11488.
- [24] Ma, X., Huang, J., Metra, C., & Lombardi, F., "Reversible gates and testability of one dimensional arrays of molecular QCA", Journal of Electronic Testing, 24(1-3), 297-311, 2008.
- [25] QCADesigner 2.0.3-setup-gtk.exe setup "http://www.mina.ubc.ca/qcadesigner_downloads".

BIOGRAPHY



Kunal Chaudhary received his B.Tech-ECE Degree in 2013 and is now pursuing his M.Tech thesis in the field of Electronics and Communication Engineering from CTIEMT, Jalandhar. His research interests are Digital Design systems, Nanotechnology based system & Quantum Computing.



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