

Process Simulation of Super Junction Power MOSFET

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ABSTRACT: This paper show a simple model for fabrication process of Super junction power MOSFET. The device dimensions, different regions, appropriate materials for each regions etc. are taken from literature to achieve desired property accordingly. The benefit for such type of modelling is to make fabrication process steps easier to understand. On the basis of some specific parameters like on-state resistance, break down voltage etc. a comparative study is also done to illustrate, the basic differences in Conventional Power MOS with Super junction Power MOS.

KEYWORDS: Power MOSFET, Super Junction MOSFET, SILVACO.

I. INTRODUCTION

All the semiconductor devices like diodes, transistors, MOSFETs, JFETs, etc are used as a power devices. Among them all, MOS based power devices are most favourably used. A power MOSFET is a specific type of metal oxide semiconductor field-effect transistor (MOSFET) designed to handle significant power levels. Compared to the other power semiconductor devices, for example IGBT, Thyristor, its main advantages are high commutation speed and good efficiency at low voltages. But there are some mark able problems associated with them. Therefore, V shaped MOS, Double diffused MOS, U shaped MOS, Lateral MOS, Super Junction (SJ) MOS are used as power devices. VMOS has lowest ON-resistance and used at power up to 50V [1][2]. A Super junction Power MOSFET with breakdown voltage of 600V is compared with conventional Power MOSFET in following table I:

Table 1: Conventional Power MOS vs SJ Power MOSFET (600 V)

Parameters	Conventional Power MOS	SJ Power MOS
ON-state Resistance (R_{DS} (ON))	275 M Ω	230 M Ω
Blocking Voltage (BVDSS)	Low	High
Temperature Coefficient	Negative	Positive
Break down voltage	Up to 200V	Up to 1000V
Switching speed/time	High	Low
Conduction Losses	Less	High
Size and Weight	More	less
Cost	Low	High

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The above comprehensive comparison shows that, due to charge balancing mechanism by using of n and p columns, SJ power MOS have low value of resistance, it results low conduction losses. Less area in SJ Power MOS make low value of capacitances also. The combination of low resistance and capacitance values, make less switching time and improved speed. Therefore, SJ power MOS now become favourable device in high frequency applications [3].

II. SUPER JUNCTION POWER MOSFET

In the Super junction (SJ) power MOSFET structure, the heavily doped alternative p-n columns (or p-n pillars) are replaced by the lightly doped drift region of conventional power MOS. These p-n columns have the same doping level, therefore, they have equal amount of positive and negative charges. The numbers of such columns are applications specific. The middle column, for example, in SJ n-MOSFET, where n type doping column is just below the gate, called drift region, used as to form conduction path for charge carriers. By proper choosing the depth, width and doping profile for these regions, we can precisely controlled charges and so as, current due to positive and negative charges. A Schematic diagram of Super junction power MOSFET is shown in figure 1. The opposite sides of source and drain in SJ MOS structure support higher current and voltage.

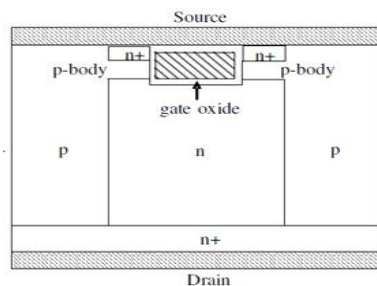


Figure 1: Schematic View of Super Junction Power MOSFET [4]

To obtain the maximum break down voltage, drift region length and width is properly optimized. Electric field distribution in this region also support break down voltage. Uniform electric field increase break down of device [4].

III. DEVICE PARAMETERS FOR SJ MOSFET

The designing of SJ power MOSFET includes drift region engineering, i.e width, depth, doping and isolation from other regions. All dimensions are precisely controlled for particular voltage ratings. Another important design parameter is about trench, which is optimized for break down voltage. The correspond device parameters are mentioned in table 2:[5].

Table 2: Design parameters of SJ Power MOSFET for Simulation

Device Parameters	SJ MOSFET
Cell pitch	12 um
Device height	43um
Device Width	18 um
For each n and p type Pillar height	36 um
For each n and p Pillar Width	6 um
Trench depth	36 um
Epitaxy layer thickness	42 um
N+ source	1 um

From above table, we see that doping of n and p pillars/columns have exactly same doping level. This is charge balancing phenomena where equal amount of positive and negative charges are there. It results best performance in SJ power MOS [6] [7].

IV. SIMULATION & RESULTS

Here super junction Power MOSFET is fabricated by Deep Trench Etching where deep trenches of p type material is fabricated on n-type substrate [8]. The Super junction MOSFET fabrication process is starts with a moderately doped n⁺ - type (100) Si substrate with substrate dopant concentration of As 5x10¹⁸/cm³ .

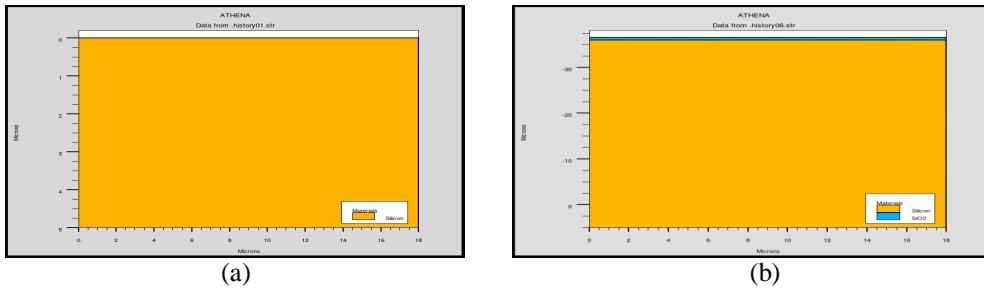


Figure 2: (a) An n-type epitaxial layer (36 um) is deposited on the entire surface, (b) Deposition of Oxide SiO₂

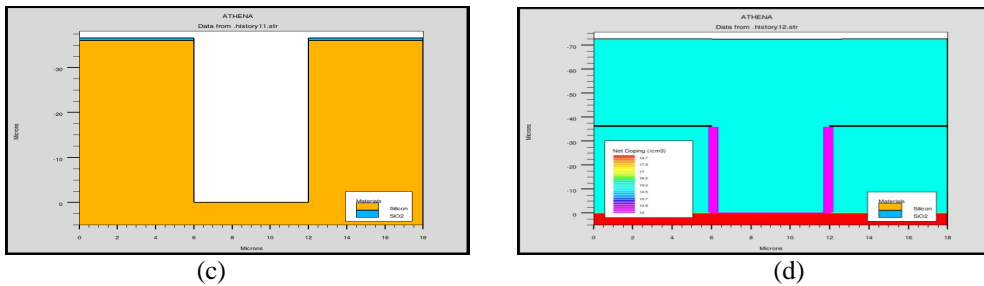


Figure 3: (c) Trench of 36 um were formed by using selective Reactive Ion Etching (RIE), (d), P-type layer was epitaxial grown to fill the trench using conformal deposition.

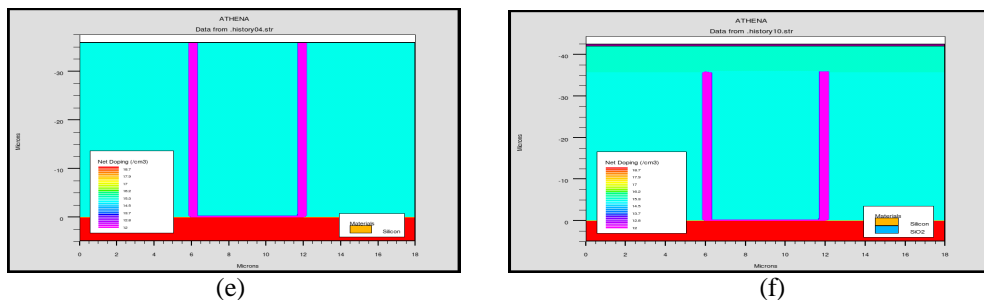
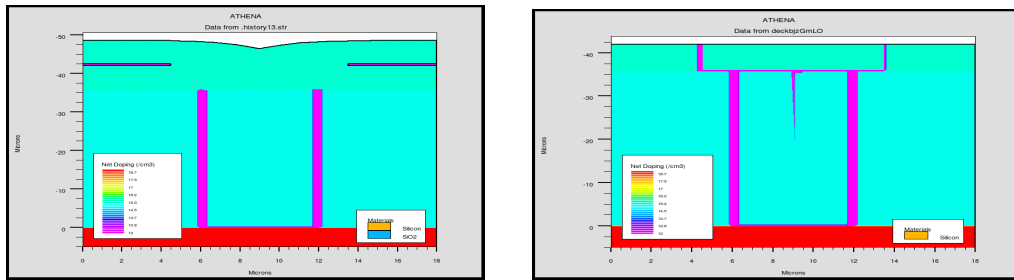


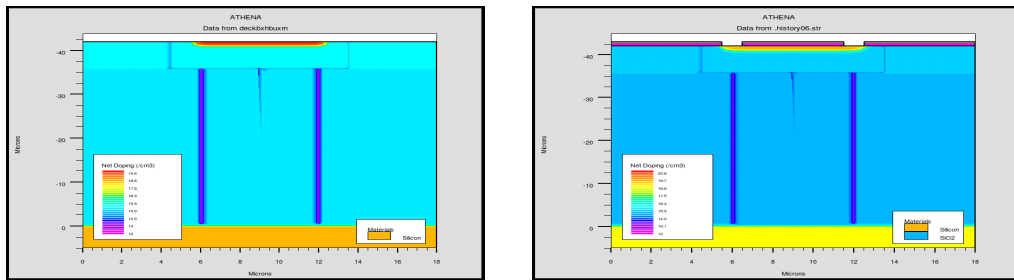
Figure 4 : (e) Etched the entire layer of p type above the oxide layer and then removed all oxide, (f), A 6um thick n-type epitaxial layer is deposited using conformal deposition and a thin layer of oxide is also grown.



(g)

(h)

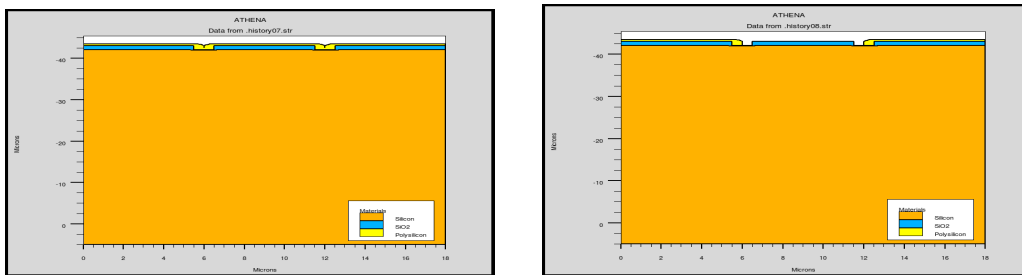
Figure 5: (g) Open a window for making p-type tub and deposition of 6 μm thick P-type layer, (h) Etched the entire top surface of p-type layer and removed all oxide, p-Pillar and n-Pillar were formed.



(i)

(j)

Figure 6: (i) Deposition of oxide and open window for making p^+ region. Implantation of Boron through the window in p-type tub and removed all oxide layer, (j) Deposition of oxide layer and window opening for making n^+ region in p^+ region and n-type impurity atom, phosphorus, are implanted through the window in the oxide and etched whole oxide. And thus the source region is defined [9], [10].



(k)

(l)

Figure 7: (k) Deposition of Poly-Si layer over the entire wafer, (l), RIE for Poly-silicon

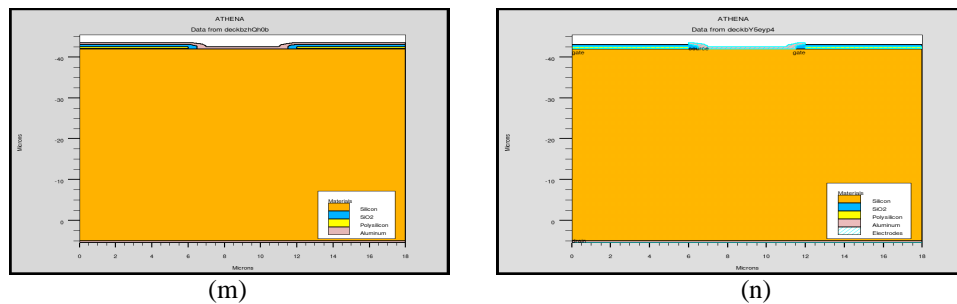


Figure 8: (m) Metallization of Aluminium, (n) Un-Wanted metal is etched and defined the electrodes for Source, Gate and Drain.

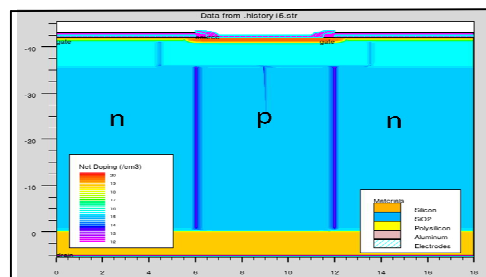


Figure 9: A two dimensional Super Junction MOSFET model

Above figure shows the final model of SJ MOSFET, where n and p columns are placed alternatively, which is differ from Conventional MOS [11], [12].

V. CONCLUSIONS

In conclusions, Super Junction Power MOSFET has been studied and complex fabrications process flow of such device has become simpler by easy going flow in SILVACO. The DECKBUILD tool of SILVACO is used for making this deep trench, n and p columns Super Junction Power MOSFET. For Modelling and simulation, appropriate data collection is very much important. This modelled structure is compared with another super junction power MOSFET which have different specifications and modelling style. This shows good agreement having simpler and more visualize method for model process flow.

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