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## Analysis of Approximate Compressor for Multiplication Using CSLA Sharing CBL

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**ABSTRACT:** In the design of Integrated Circuits, area occupancy plays a vital role because of increasing the necessity of portable systems. Carry Select Adder (CSLA) is one of the fastest adders used in many data-processing processors to perform fast arithmetic functions. In this project, an area-efficient carry select adder by sharing the common Boolean logic term (CBL) is used. After logic simplification and sharing partial circuit, only one XOR gate and one inverter gate in each summation operation as well as one AND gate and one inverter gate in each carry-out operation are needed. Through the multiplexer, the correct output is selected according to the logic states of the carry in signal. The modified design has been developed using Binary to Excess-1 converter (BEC). The new design has reduced area and delay as compared with the regular SQR CSLA design. The result analysis shows that the newly designed SQR CSLA structure is better than the regular SQR CSLA.

**KEYWORDS:** Adder, Carry select Adder (CSLA), Modified CSLA (MCSLA), Square Root CSLA (SQR CSLA), Data processing processors.

### I. INTRODUCTION

In computers and other processors, adders are not only used to perform arithmetic operations such as addition, subtraction but also to calculate other applications such as addresses, table indices etc. Adders are also used in multipliers, in high speed integrated circuits and in digital signal processing to execute various algorithms like FFT, IIR, FIR. Now a days design of low power, area efficient high speed data path logic system are the most important areas of research of VLSI designs.

On the basis of the requirements such as area, delay and power consumption, some commonly used adders are Ripple Carry Adders, Carry Select Adders and Carry Look-Ahead Adders. Even though the design of Ripple Carry Adder (RCA) is compact, but the computation time is longer. Time critical applications make use of Carry Look-Ahead Adder (CLA) to derive fast results but it leads to increase in area.

The aim of this project is to present the design of Carry Select Adder (CSLA) by sharing Common Boolean Logic (CBL). The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independent generation multiple carries and then select a carry to generate the sum. However, the CSLA is not an area efficient because it uses multiple pairs of ripple carry adder to generate partial sum and carry by considering carry input as  $C_{in}=0$  and  $C_{in}=1$ , then the final summation and carry are selected by the multiplexers. An area-efficient carry select adder share the Common Boolean Logic term to duplicate adder cells in the conventional carry select adder. It saves many transistor counts and achieves a low power.

This project is organized as follows: In section II Related work is shown, section III deals with the modified CSLA, section IV Regular SQR CSLA, and Modified SQR CSLA, section V explains the Proposed SQR CSLA using common Boolean logic. Results are analysed in section VI and section VII concludes and tells about future scope.

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## II. RELATED WORK

Ripple Carry Adder consists of cascaded “N” single bit fulladders. Output carry of previous adder becomes the input carry of next full adder. Therefore, the carry of this adder traverses longest path called worst case delay path through N stages. Fig.1 shows the block diagram of 4-bit ripple carry adder. Now as the value of N increases, delay of adder will also increase in a linear way. Therefore, RCA has the lowest speed amongst all the adders because of large propagation delay but it occupies the least area. Now CSLA provides away to get around this linear dependency is to anticipate all possible values of input carry i.e. 0 and 1 and evaluate the result in advance. Once the original value of carry is known, result can be selected using the multiplexer stage. Therefore the conventional CSLA makes use of Dual RCA’s to generate the partial sum and carry by considering input carry  $C_{in}=0$  and  $C_{in}=1$ , then the final sum and carry are selected by multiplexers. The conventional CSLA is area consuming due to the use of dual RCA’s.

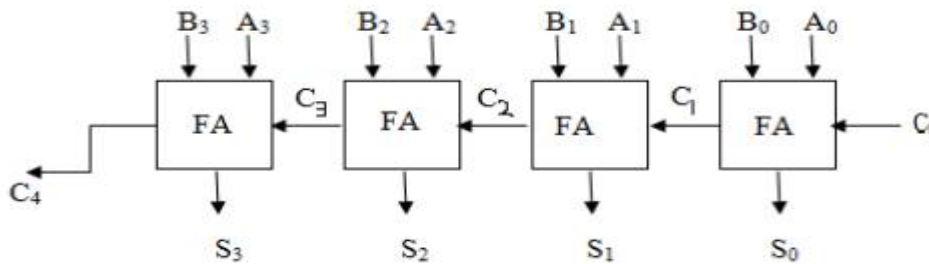


Fig 1: 4-bit Rpple Carry Adder

The basic idea of this work is to use Binary to Excess- 1 converter (BEC) instead of RCA with  $C_{in}=1$  in conventional CSLA in order to reduce the area and power. BEC uses less number of logic gates than N-bit full adder structure. To replace N-bit RCA, an N+1 bit BEC is required. Therefore, Modified CSLA has low power and less area than conventional CSLA. SQRT CSLA has been chosen for comparison with modified design using BEC as it has more balanced delay, less area and low power. Regular SQRT CSLA also uses dual RCAs. In order to reduce the delay, area and power, the design is modified by using BEC instead of RCA with  $C_{in}=1$ . Therefore, the modified SQRTCSLA occupies less area, delay and low power. Further also, the parameters like delay, area and power can be reduced. Fig.2 shows the diagram of 16-bit conventional CSLA. By sharing Common Boolean Logic (CBL), a circuit of SQRT CSLA is proposed. This proposed design is better than all the other adders in respect of area, delay and power consumption.

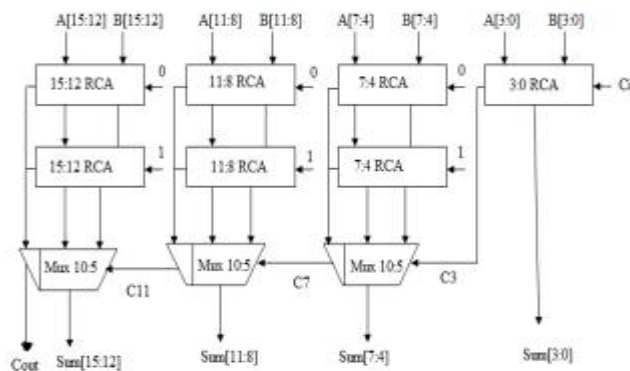


Fig 2.16-bit conventional CSLA

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### III. MODIFIED CSLA

The basic idea of this work was to use Binary to Excess-1 converter (BEC) instead of RCA with  $C_{in}=1$  in conventional CSLA in order to reduce the area and power. BEC uses less number of logic gates than N-bit full adder structure. To replace N-bit RCA, an N+1 bit BEC is required. Therefore, Modified CSLA has low power and less area than conventional CSLA. SQRT CSLA has been chosen for comparison with modified design using BEC as it has more balanced delay, less area and low power. Regular SQRT CSLA also uses dual RCAs. Circuit of BEC is shown in fig 3.

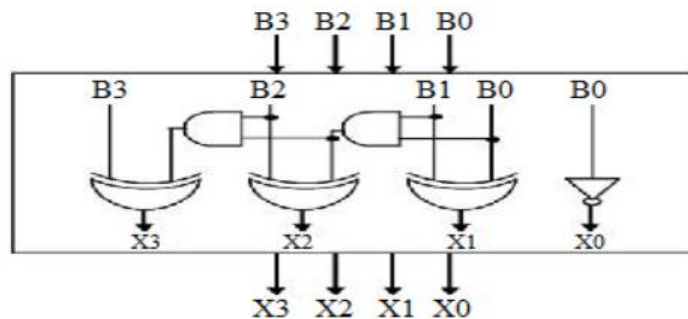


Fig 3: 4-bit Binary to Excess-1 Converter

In order to reduce the delay, area and power, the design is modified by using BEC instead of RCA with  $C_{in}=1$ . Therefore, the modified SQRTCSLA occupies less area, delay and low power. Further also, the parameters like delay, area and power can be reduced. And truth table is shown in Table 3.1. Goal of addition is achieved using BEC together with the multiplexer.

One of the input of 8:4 MUX gets as its inputs (B3,B2,B1,B0) and another input of MUX is BEC output. Boolean expressions of 4-bit BEC are listed below. (Note: symbols ~NOT, &AND and ^XOR).

- $X_0 = \sim B_0$
- $X_1 = B_0 \wedge B_1$
- $X_2 = B_2 \wedge (B_0 \wedge B_1)$
- $X_3 = B_3 \wedge (B_0 \wedge B_1 \wedge B_2)$

Table 1: Truth table of 4-bit binary to excess -1 converter

Binary Logic $B_0 B_1 B_2 B_3$	Excess-1 Logic $X_0 X_1 X_2 X_3$
0000	0001
0001	0010
0010	0011
0011	0100
0100	0101
0101	0110
0110	0111
0111	1000
1000	1001
1001	1010
1010	1011
1011	1100
1100	1101
1101	1110
1110	1111
1111	0000

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The main idea of this work is to use BEC instead of RCA with  $C_{in}=1$  in order to get the reduced area and power consumption of the conventional CSLA. To replace the Nbit RCA, N+1 bit BEC is required. Thus, modified CSLA is designed such that it occupies less area and has low power than conventional CSLA. Block diagram of Modified CSLA is shown in Fig.4.

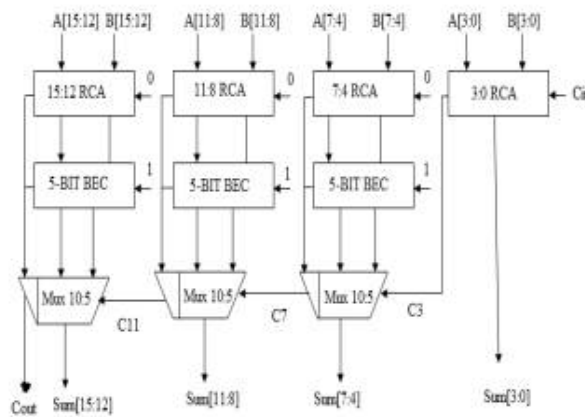


Fig.4. Block diagram of 16-bit modified CSLA

## IV. REGULAR SQRT CSLA AND MODIFIED SQRT CSLA

The structure of 16-bit regular SQRT CSLA is shown in Fig.5. It has five groups of different size RCA. Each group contains dual RCA and MUX. Conventional CSLA has one main disadvantage of high area usage. This advantage can be overcome in Regular SQRT CSLA. So SQRT CSLA is improved version of Conventional CSLA.

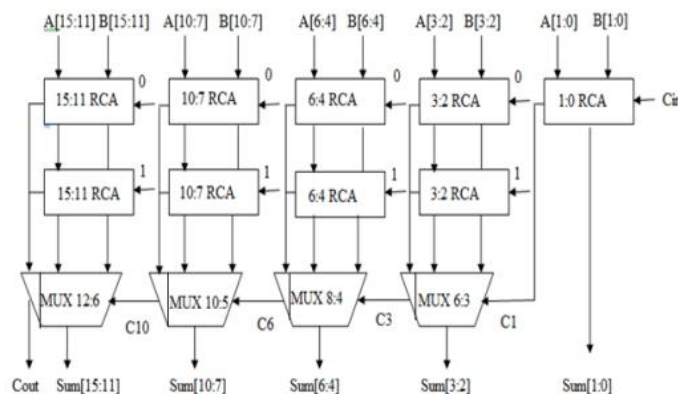


Fig:5 16-bit Regular SQRT CSLA

Time delay of conventional CSLA can be decreased by having one more input into each set of adders than in previous set. This is known as SQRT CSLA. In SQRT CSLA, group3 has two sets of 3-bit RCA. Selection input of 8:4 MUX is  $c_3$ . If  $c_3=0$ , then MUX selects first RCA output ( $C_{in}=0$ ) otherwise second RCA output ( $C_{in}=1$ ) is selected.

Modified SQRT CSLA is similar to that of regular SQRT CSLA, the only difference is we replace RCA with  $C_{in}=1$  with BEC. This replaced BEC performs the same operation as that of the replaced RCA with  $C_{in}=1$ . Fig.6 shows the block diagram of modified SQRT CSLA. This structure consumes less area, delay and power than regular SQRT CSLA because of less number of transistors are used.

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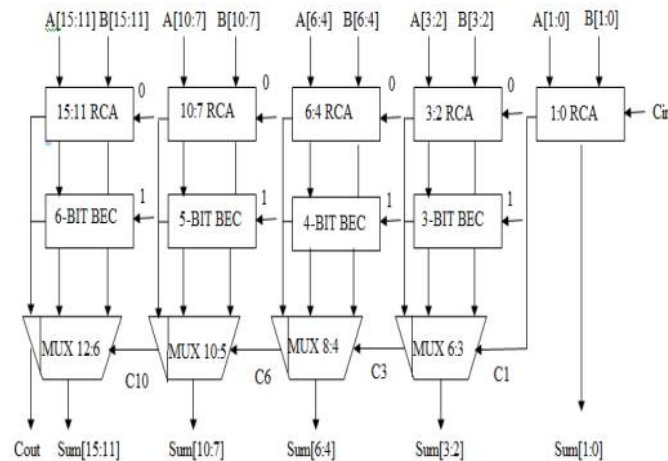


Fig:7 Modified Sqrt CSLA

## V. PROPOSED Sqrt CSLA USING CBL

To remove the duplicate adder cells in the conventional CSLA, an area efficient Sqrt CSLA is proposed by sharing Common Boolean Logic (CBL) term. While analysing the truth table of single bit full adder, results show that the output of summation signal as carry-in signal is logic “0” is inverse signal of itself as carry-in signal is logic “1”. It is illustrated by red circles in Table 2. To share the Common Boolean Logic term, we only need to implement a XOR gate and one INV gate to generate the summation pair. And to generate the carry pair, we need to implement one OR gate and one AND gate. In this way, the summation and carry circuits can be kept parallel.

Table 2 Truth table of CSLA using CBL

$C_{in}$	A	B	S0	C0
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

This method replaces the Binary to Excess-1 converter add one circuit by common Boolean logic. As compared with modified Sqrt CSLA, the proposed structure is little bit faster. Internal structure of proposed CSLA is shown in Fig.7.

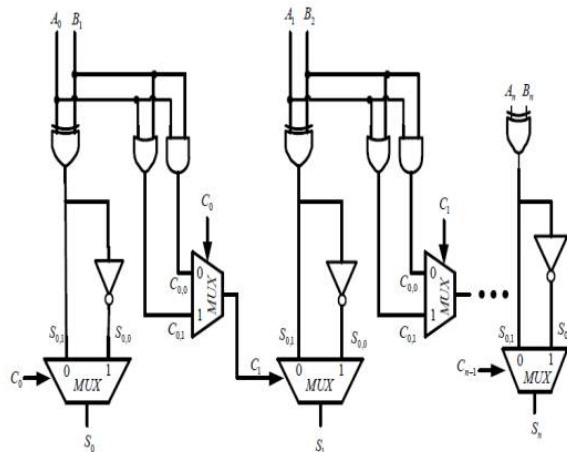


Fig.7 Internal structure of the proposed area-efficient carry select adder is constructed by sharing the common Boolean logic term

In the proposed Sqrt CSLA, the transistor count is trade-off with the speed in order to achieve lower power delay product. Thus the proposed Sqrt CSLA using CBL is better than all the other designed adders. Fig.8 shows the block diagram of Proposed Sqrt CSLA.

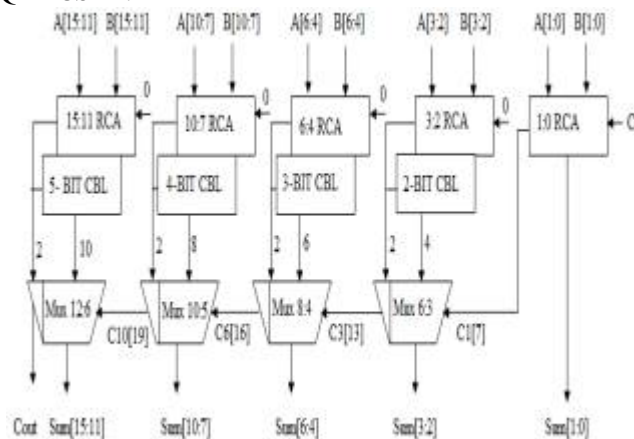


Fig. 8 16-Bit Proposed Sqrt CSLA using Common Boolean Logic

## VI. EXPERIMENTAL RESULT

This work has been developed using Xilinx tool. Table 3 shows the comparison between the various adders like conventional CSLA, Modified CSLA, regular Sqrt CSLA, modified Sqrt CSLA and proposed Sqrt CSLA for 8-bit, 16-bit, 32-bit and 64-bit. The parameters on which they are compared are area, delay and power. Fig. 10 depicts that the proposed Sqrt CSLA has less number of gates and hence less area. Fig.9 shows the adder circuit for delay comparison. The results compared in Fig. 12 shows that the power consumption of proposed Sqrt CSLA is reduced. It is clear that power, area and delay of proposed Sqrt CSLA for 8-bit, 16-bit, 32-bit and 64-bit is reduced as compared to other adders.

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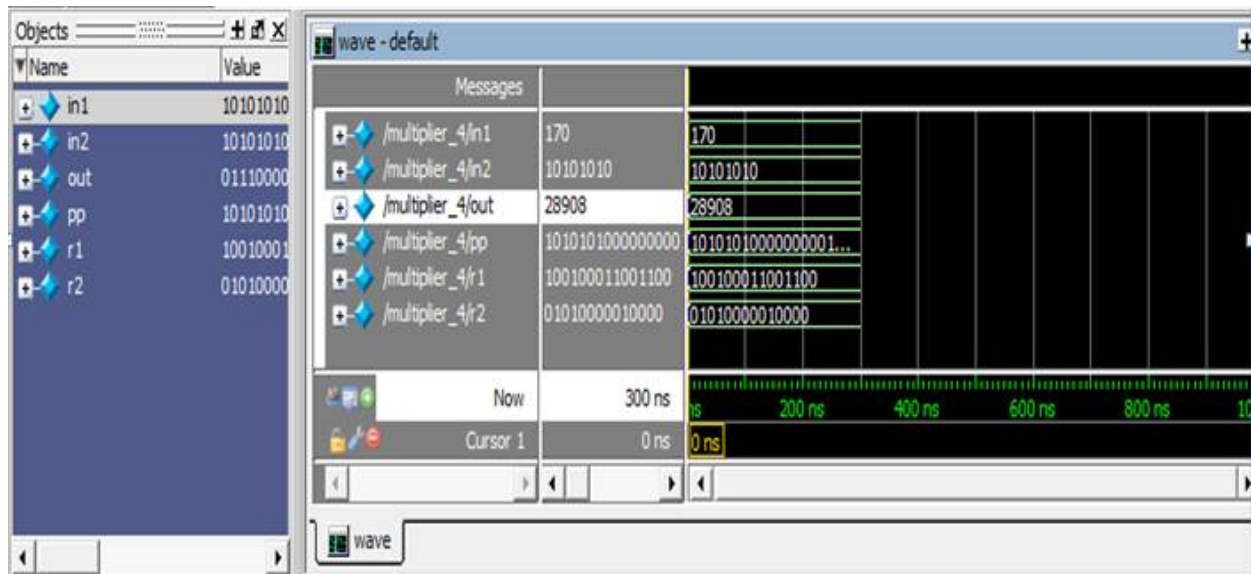


Fig.9 Simulation of Sqrt CSLA sharing CBL

Table 4 Area, Delay, Power comparison of Sqrt CSLA using CBL

Word Size	Adder	Area (No. of gate count)	Delay (ns)	Power (mW)	Power Delay Product (pWs)
8-bit	Conventional (Dual RCA)	200	14.46	94.48	1366.36
	Modified (with BEC)	167	16.63	86.92	1445.47
	Regular Sqrt (Dual RCA)	144	11.92	193	2300.56
	Modified Sqrt(with	132	13.69	180	2464.2

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	BEC)				
	Proposed SQR T(with CBL)	111	11.15	119	1326.85
16-bit	Conventional (Dual RCA)	480	19.81	94.63	1874.90
	Modified (with BEC)	381	21.59	81.38	1757.48
	Regular SQR T (Dual RCA)	348	16.15	315	5087.25
	Modified SQR T(with BEC)	291	18.77	268	5030.36
	Proposed SQR T(with CBL)	276	15.48	177	2739.96
32-bit	Conventional (Dual RCA)	1040	30.51	95.01	2899.42
	Modified (with BEC)	809	32.65	79.81	2605.79
	Regular SQR T (Dual RCA)	698	28.97	553	16020.41
	Modified SQR T(with BEC)	762	34.44	448	15429.12
	Proposed SQR T(with CBL)	552	26.23	321	8419.23
64-bit	Conventional (Dual RCA)	2160	51.92	95.49	4958.222
	Modified (with BEC)	1665	54.01	79.25	4280.292
	Regular SQR T (Dual RCA)	1592	52.82	860	45425.2
	Modified SQR T(with BEC)	1498	64.61	745	48134.45
	Proposed SQR T(with CBL)	1104	47.74	555	26495.7

## VII. CONCLUSION AND FUTURE SCOPE

Power, delay and area are the constituent factors in VLSI design that limits the performance of any circuit. This work presents a simple approach to reduce the area, delay and power of CSLA architecture. The conventional carry select adder has the disadvantage of more power consumption and occupying more chip area. The proposed SQR T CSLA using common Boolean logic has low power, less delay and reduced area than all the other adder structures. It is also little bit faster than all the other adders. In this way, the transistor count of proposed SQR T CSLA is reduced having less area and low power which makes it simple and efficient for VLSI hardware implementations.

This work has been designed for 8-bit, 16-bit, 32-bit and 64-bit word size and results are evaluated for parameters like area, delay and power. This work can be further extended for higher number of bits. New architectures can be designed in order to reduce the power, area and delay of the circuits. Steps may be taken to optimize the other parameters like frequency, number of gate clocks, length etc.



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