

Capacitive Sensor with Transducer Using Frequency Modulation for Seismometer

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ABSTRACT: Among the multitude of sensors, the capacitive sensor is one of the best to detect the displacement. Several kinds of vibrations sources may cause destruction of the civilian infrastructure such as earthquakes, explosions... To study seismology or seismic prospection needs an adequate sensor. A capacitive sensor design is proposed. The sensor used a pendulum system. One of the two capacitor plates is joined to the fixed holder, and the other one is joined to the mobile element. The vibrations detected are converted into electrical signal by using a transducer. The transducer is based on using frequency modulation (FM) system. A CMOS circuit phase locked loop is used for the transducer circuit base.

KEYWORDS: Transducer, frequency modulation, seismometer, capacitive sensors, PLL.

I. INTRODUCTION

In seismometer, the signal period to detect an event can be over 100 seconds [9]. Our new seismic broadband sensor uses the capacitive sensor technical. Therefore, the frequency modulation is used for the transduction system with a variable capacitor. One of the two plates is joined on the fixed holder; the other one is linked on the mobile unit with the seismic mass (pendulum).

The previous system uses the capacitance variation of a variable capacitor [10]. A high frequency (HF) alternative signal with opposition phase is applied on the two plates fixed on the built. A mobile plate moves between the fixed plates. The phase of the resultant signal is picked out for the measurement [8].

This study elaborates a capacitive sensor that two capacitors plates are provided, with transducer using frequency modulation technical. Studying the capacitive sensor requires to determine the sensitivity output demodulation versus plates capacitor displacement, the FM modulator characteristics and the transducer time response. Thus a CMOS 4046 Phase Locked Loop (PLL) circuit is used.

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II. RELATED WORK

II-1- CAPACITIVE SENSOR

A capacitive sensor is a device that two conductive plates are separated by a small distance [1]. If a current flows, a positive charge q will be collected on the one plate of the capacitor. A balancing charge will be present on the other plate to preserve the neutrality charge. A voltage potential proportional to q appears between the two plates. $v = \frac{d}{\epsilon A} q$ Where A is the area of the plates, d is the distance of their separation, ϵ is the permittivity of insulating layer ($\epsilon_0 = 8.85 \text{pF/m}$ for vacuum). The quantity $C = \frac{\epsilon A}{d}$ is the capacitance of the capacitor measured in Farads (F). The charge $q = Cv$ [1] [2].

II-2- THE MODULATOR

The modulating signal modifies the carrier frequency in modifying the signal phase [11]. It uses the frequency modulation technical: The carrier amplitude still constant then the frequency varies with the modulating signal rhythm [12].

The frequency modulated signal expression is [12] [13] [14]:

$$s(t) = A_p \cos[\omega_p t + 2\pi k \int u(t) dt]$$

$u(t)$ is the modulating signal, k the modulator sensitivity expressed in Hz/A_m (A_m modulating signal amplitude), ω_p the carrier instantaneous frequency. The instantaneous phase:

$$\varnothing(t) = \omega_p t + 2\pi k \int u(t) dt$$

If the modulating signal is a sinusoid, the carrier instantaneous phase is:

$$\varnothing(t) = \omega_p t + A_m \frac{k}{\omega_m} \sin \omega_m t$$

Where ω_m is the instantaneous modulating signal frequency. The instantaneous frequency

$$f_s(t) = f_p + k \cdot A_m \cos \omega_m t$$

The frequency deviation

$$\Delta f_s(t) = k \cdot A_m$$

The phase deviation or modulation index δ

$$\Delta \varnothing_s = \frac{\Delta f_s}{f_m} = \delta$$

The modulator is composed by the PLL Voltage Controlled Oscillator (VCO) (CD4046) and the capacitor C_1 is composed by two plates described above.

The figure 1 shows the VCO schema presented in the CD4046 circuit illustrated by the datasheet [5] [7]. The VCO output is on the pin 4, the plate capacitor is inserted on the pin 6 and pin 7, the VCO input (voltage control) is on the pin 9 and the voltage demodulated is on the pin 10.

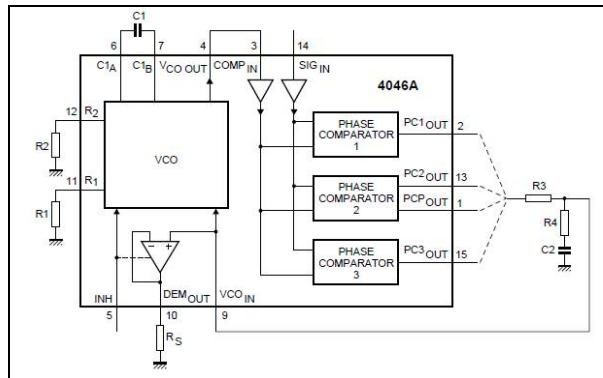


Figure 1: CD4046 circuit schema (4046 datasheet [5] [7]). It contains the VCO and three phase comparators.

II-3- THE TRANSDUCER

The function of this module is to extract the modulating signal. We use the synchronic detection technical. This technique consists to generate a signal with the same frequency and phase as the carrier signal. An intermediate signal is obtained by the product of the generated and the carrier signal. To get the modulating signal, the intermediate signal is filtered by a low pass filter [13] [15] [17].

If $s(t)$ is the signal modulated by $u(t)$:

$$s(t) = [1 + ku(t)]. A_p \cdot \cos \omega_p t$$

The intermediate signal is:

$$s_i(t) = s(t) \cdot \cos \omega_p t = [1 + k \cdot u(t)]. A_p \cdot \frac{1 + \cos 2\omega_p t}{2}$$

After filtering with low pass filter, the term with $\cos 2\omega_p$ will be eliminated, only the term with $u(t)$ still remain. Consequently, the carrier signal and the generated signal must be rigorously in phase. With the PLL system, we can synthesize a signal rigorously in phase with the carrier signal.

In figure 2, we can find the PLL synoptic. There are three functional blocs: A phase comparator, a low pass filter, a VCO. The phase comparator output voltage is u_r , the result of u_e and u_s phases shifting. This signal (u_r) is filtered by a low pass filter to get u_f . The VCO voltage control is u_f .

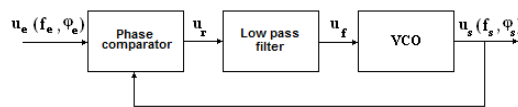


Figure 2: PLL synoptic composed by a phase comparator, a low pass filter, a VCO.

- Phase comparator:

Every time, this module compares the instantaneous phase ϕ_e of a periodic signal on its input with the VCO instantaneous phase. The output delivers an average signal dependant of the phase shift between the two signals in input [14] [16]. The PLL is locked when $f_e = f_s$. The output voltage expression is [17]:

$$u_r = K_D \cdot f(\phi_e, \phi_s)$$

K_D is the comparator gain in V/rad.

The 4046 circuit uses three kinds of phase comparator. The choice was based on design flexibility and the compatibility of CMOS technology with the applications [4].

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- Low pass filter:

The harmonic signals present on the output must be eliminated by a low pass filter. An average signal will be covered. Only the direct current (DC) signal is covered [13] [15] [16].

- VCO:

The VCO runs at a set frequency f_0 called center frequency when there is no signal input $u_e(t)$. When an input signal $u_e(t)$ is applied, the comparator compares the phases and the frequencies of the input signal $u_e(t)$ and the signal delivered by the VCO $u_s(t)$. An error voltage $u_r(t)$ is generated and proportional to the phases and the frequencies difference of the input and VCO signal. An average signal u_f is delivered on the low pass filter output; it is applied to the VCO control voltage. The signal $u_r(t)$ is used to reduce the frequencies difference [3] [6].

The frequency lock range is defined with the VCO characteristic shown in figure 3. The centre frequency f_0 corresponds to $VCO_{IN} = \frac{1}{2} V_{DD}$; the frequency locked range is defined with $2f_L = (f_{max} - f_{min})$ [3]. The offset frequency is $f_{off} = f_0 - 1.6 f_L$ [5].

The figure 3 shows the VCO frequency characteristic operating with offset. The center frequency is f_0 , corresponding with $V_{cc}/2$. The frequency lock range is $2f_L = (f_{max} - f_{min})$, where f_{max} corresponds to $VCO_{in} = (V_{cc} - 0.9V)$ and f_{min} corresponds to the $VCO_{in} = 0.9V$, offset frequency is $f_{off} = f_0 - 1.6f_L$ [5].

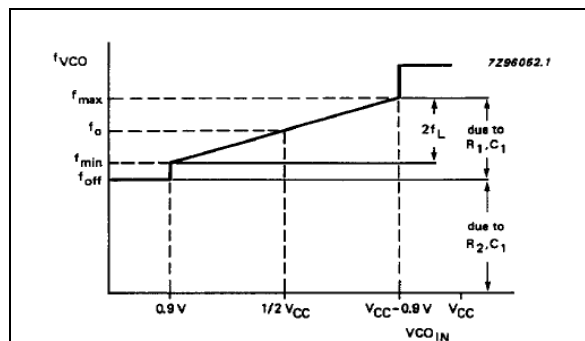


Figure 3: VCO frequency characteristic (74HC/HCT4046 datasheet Philips) [5]. It presents the VCO frequency vs VCO in (voltage control)

The figure 4 presents two charts using to determine the PLL components. To select R_1 , R_2 , C_1 , give f_0 and $2f_L$, R_2 and C_1 are determined by using the chart on figure 4a. The chart on figure 4b is needed to determine R_1 [7].

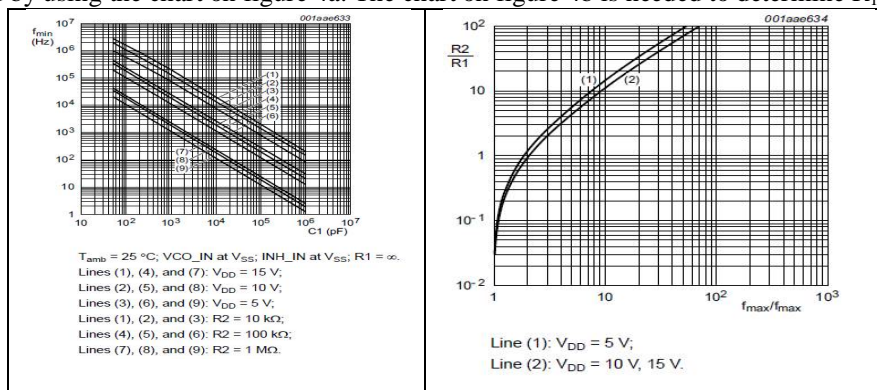


Figure 4: a- Typical frequency offset as a function of C_1 ; b- Typical ratio R_2/R_1 as function of the ratio f_{max}/f_{min} (Charts by HEF4046 datasheet NXP Semiconductor) [7]

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The CMOS circuit CD4046 is used as demodulator. The figure 1 shows the electronics assembly for the CD4046 [5] [7].

The signal input uses as reference is a signal stabilized by quartz. It is applied on the pin 14. We use the XOR gate for the phase comparator. The modulating signal is covered at pin 10.

III. SENSOR DESIGN

A mechanical system supports the capacitor plates. One plate is fixed on the mobile element and the other one mounted on the immovable element. A displacement (d) between the two plates produces a variation of the capacitance ($C = \frac{\epsilon A}{d}$) [1]. This capacitor is coupled to the CMOS 4046 PLL circuit. It is used as C_1 in figure 1. A displacement variation produces a VCO frequency variation. On the input signal (pin 14 CD4046) is applied a reference signal by a quartz oscillator. When the PLL is locked to the reference signal, the pin 10 (V_{demod}) provided a demodulator voltage output of the VCO input. This signal is used to reduce the frequencies difference between the input signal (pin 14) and the VCO frequency [3]. The displacement variation of the mobile plate will be interpreted with the demodulation signal output variation.

The characteristics of the sensor are exposed in the next part: Sensitivity (modulator and transducer), modulation index, time response.

IV. EXPERIMENTAL RESULTS

- Sensitivity

The figure 5 shows the modulator response frequency (kHz) with respect to the displacement (mm). On the figure 5 (a) the response on the displacement range between [0.2; 3.0] mm is shown. On the figure 5 (b) the displacement range [0.2 ; 1.0] mm is considered. In this range the sensitivity is better (31.12kHz/mm).

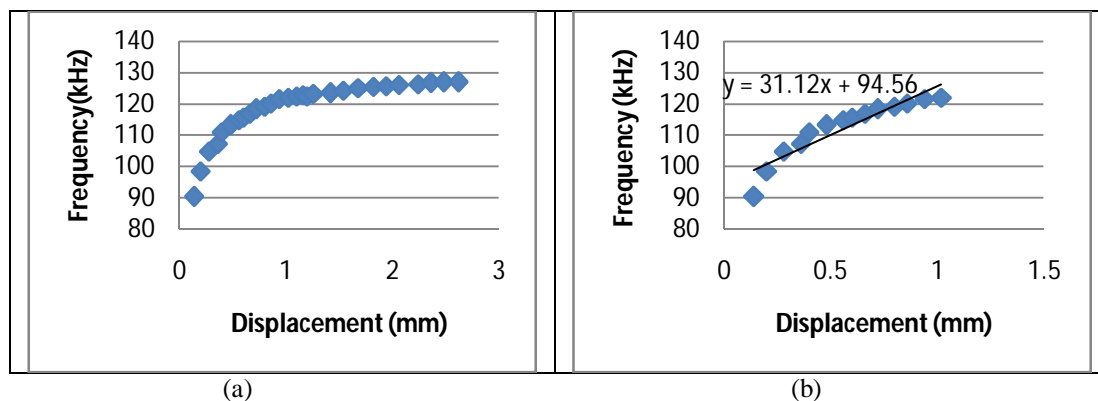


Figure 5: Sensitivity VCO frequency vs displacement. In (a) is presented the sensitivity with the full scale displacement, in (b) is selected the displacement zone where the sensitivity is better [0.2 ; 1.0] mm

The figure 6 shows the transducer demodulation (V) with respect to the displacement (mm). On the figure 6 (a), the demodulation versus displacement response between [0.5; 3.0] mm is represented. The figure 6 (b) represents the demodulation versus displacement response in the range [0.5; 1.0] mm. In this range, the sensitivity is better and the response is linear.

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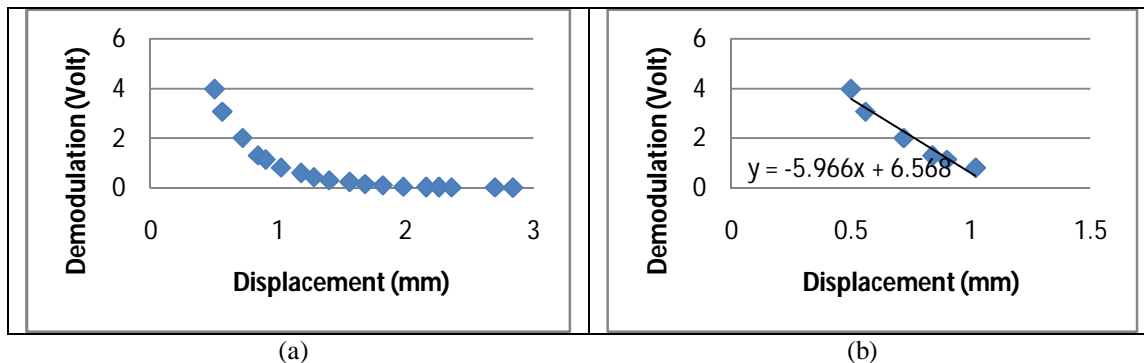


Figure 6: Curve representing the demodulation (V) vs the displacement (mm). In (a) is presented the sensitivity with the full scale displacement, in (b) is selected the displacement zone where the sensitivity is better [0.2 ; 1.0] mm

By regression:

$$f(d) = 31.12 d + 94.56$$

$$V(d) = -5.966d + 6.568$$

In these equations, d is in mm and f in kHz: the modulator sensitivity is expressed in Hz/m, and the transducer sensitivity in V/m, then:

$$\text{modulator sensitivity} = 31.12 \cdot 10^6 \text{ Hz/m}$$

$$\text{transducer sensitivity} = 5966 \text{ V/m}$$

- Modulation index

$$\Delta\phi_s = \frac{\Delta f_s}{f_m} = \delta$$

With the value range [0.5 ; 1.0] mm, the minimum displacement is $d_1 = 0.5 \text{ mm}$, corresponds to $f_1 = 110.12 \text{ kHz}$, the maximum displacement is $d_2 = 1.0 \text{ mm}$, corresponds to $f_2 = 125.68 \text{ kHz}$, then $\Delta f_s = 7.78 \text{ kHz}$. The maximum modulating signal frequency is $f_m = 100 \text{ Hz}$ (see below). Then the modulation index is $\delta = 77$

Carson relation gives the spectrum band width: $B = 2(1 + \delta) \cdot f_m$ [13] [14]

With the above values $B = 15600 \text{ Hz}$

We get a wide band modulation (WBM).

The displacement $d_1 = 0.5 \text{ mm}$ corresponds to the demodulation $V_1 = 3.585 \text{ V}$, the displacement $d_2 = 1.0 \text{ mm}$ corresponds to $V_2 = 0.602 \text{ V}$. The maximal amplitude of the modulating signal is 2.983 V peak to peak.

- Time response

The figure 7 shows the transducer time response. Above is represented the command signal, below we can find the transducer response. The time response is the difference of the end of the time signal output and the end of the command.

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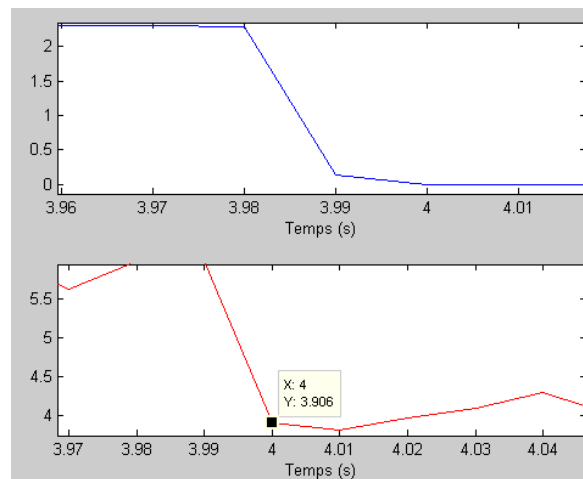


Figure 7: Above the signal command, below the transducer response

Considering the figure 7, the time response is 0.01s.
The modulating signal frequency cannot be over 100Hz.

V. CONCLUSION

- Two linear zones could be considered. The first is in the range [0.5; 1.0] mm, the second zone is in the range [1.2; 2.8] mm. The first zone presents the best sensitivity. It will be used for the sensor.
- An amplifier with a low noise and a gain equal to 13.4 is needed to get the same sensitivity as STS1 sensor sensitivity (80.000 V/m) [8].
- The time response knowledge is necessary because it limits the modulating signal frequency.

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