

# Xilinx Based Simulation of Line detection Using Hough Transform

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**ABSTRACT:** In auto focusing camera sensors line detection is main job that has to be done in less time. Hough Transform provide fast and accurate line detection in given Images. Basic type of Hough Transform is fast and efficient in small scale images. In this paper provides Xilinx simulation details of basic type of Hough transform. Hough transform algorithm is first simulated in MATLAB and then it is verified on Xilinx 13.2 design suite. Maximum image size can be of resolution 512X512.

**KEYWORDS:** Line detection, Voting Algorithm, Xilinx Simulation.

## I. INTRODUCTION

This system uses Normal representation of a line. The parametric equation of Hough transform is given by equation  $\rho = X \cdot \cos\theta + Y \cdot \sin\theta$  [2]. Here  $\rho$  and  $\theta$  are the parameters of line to be found by Hough transform. Image is captured by camera which is color image, it is converted to binary feature image using MATLAB functions. When this binary feature image is represented firstly in x-y plane shown in fig. 1.

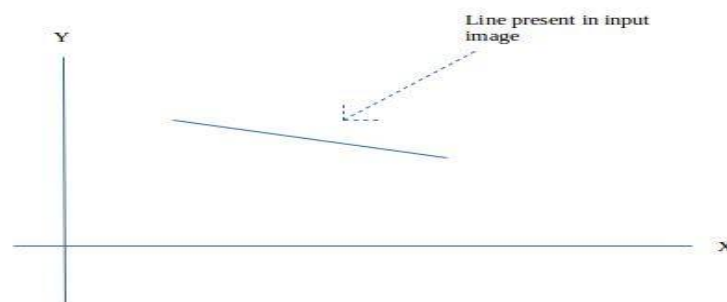


Fig. 1. Image shown in X-Y plane

Each pixel of image in x-y plane have some x-y co-ordinate value. By putting each x-y co-ordinate value in equation one,  $\rho$ - $\theta$  plane is obtained. Suppose a line is present in X-Y plane, each and every point of that line is transformed to Sinusoidal curves in  $\rho$ - $\theta$  plane. These sinusoidal curves intersect at common point in plane, That point have some  $\rho$ - $\theta$  value. This  $\rho$ - $\theta$  are parameters of a line present in  $\rho$ - $\theta$  plane shown in fig. 2. This  $\rho$ - $\theta$  plane is represented using matrix called as vote matrix, here one ( $\rho$ ,  $\theta$ ) value of  $\rho$ - $\theta$  is considered as one vote. Element of vote matrix getting maximum votes is nothing but parameters of line present in input image [2]. Xilinx 13.2 software is used for simulation and Verilog Module is used. Paper is organized as follows. Section II gives related work done on line detection using Hough transform before this system's algorithm for line detection using Hough transform. Section III describes complete steps of Xilinx simulation of this system. Section IV explain voting algorithm of Hough Transform. Section V gives this system's algorithm [3] [4] [6]. Results obtained in Xilinx simulation are explained in the section VI.

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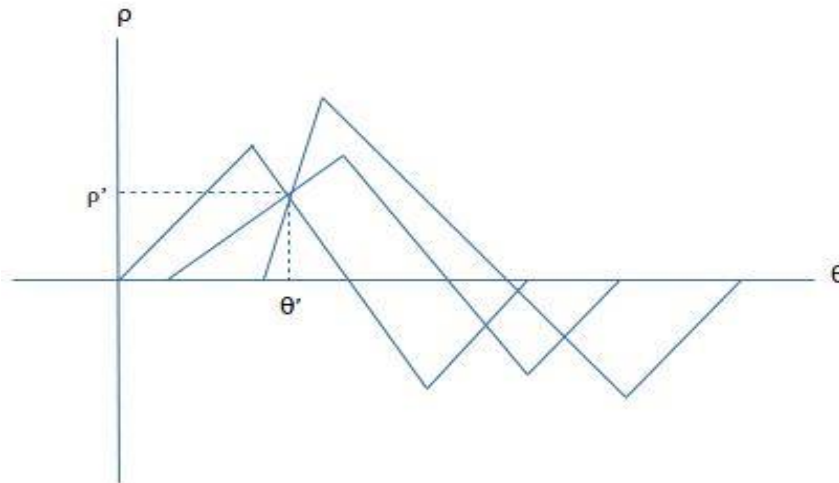


Fig. 2. Image shown in  $\rho$ - $\theta$  plane

## II. RELATED WORK

Hough Transform have more computations, other line-detection schemes such as gradient-based Hough transform and kernel-based transform. These systems require fewer computations than Hough transform, but they still require a high-end CPU, which is often unavailable in practical applications, or special hardware devices to achieve real-time performance. The gradient-based Hough Transform has been implemented in special hardware, but kernel-based Hough transform, which adopts a link-list data structure, is difficult to implement efficiently in hardware. There has been some research to implement the Hough Transform on special hardware, such as graphic processors, scan line array processors, and pyramid multiprocessors. However, these devices are unsuitable for low-cost embedded systems [2]. One straightforward method to implement Hough Transform is using multipliers. However, multipliers are less available on low-end FPGAs. Hence, some researchers implement Hough transform using a coordinate rotation digital computer (CORDIC) or a simplified CORDIC algorithm such as the multiple sector algorithm. CORDIC is an arithmetic technique developed by Volder to solve trigonometric problems by rotating a vector in small angles until the desired angle is achieved. The CORDIC algorithms for FPGA are surveyed in. CORDIC could implement the Hough transform using only shifters and adders rather than multipliers. FPGA platform is proposed to implement Hough transform by using hybrid-log arithmetic. Distributed arithmetic (DA) architecture is proposed to implement Hough transform with shift-add operations [2]. But it also requires multiple iterations to obtain one in the parameter space. An accumulator-based architecture is proposed. This system gives simulation of Hough transform using locality property on FPGA using Xilinx.

## III. XILINX SIMULATION

In Xilinx simulation software create new project and select proper FPGA hardware device. Now if image is of 512x512 size then you will have maximum rho value 725, 92160 multiplications and 46080 additions, so according to that you have to select hardware device. This system uses XC6SLX45 spartan-6 device for simulation. This system uses internal Register bank memory of XC6SLX45 to store Input image. Input image which is in binary form is stored firstly according to proper address of register bank memory in always block itself, After that Hough transform voting algorithm is executed. Pixels having zero intensity values are skipped in voting algorithm and only nonzero feature pixels of input image are given to voting algorithm. Vote for each feature pixel is calculated and stored in vote matrix. Internal registers of XC6SLX45 devices are used as vote matrix. At the end of voting algorithm vote index of vote

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matrix getting maximum votes for that particular angle are nothing but the final parameters of a line present in an input image.

### IV. SYSTEM ALGORITHM

1. Initialize all votes to zero
2. Perform voting procedure and store votes in Registers
3. for all feature points (x, y) of input image perform vote algorithm
4. now image can be any where in x-y plane between angles  $0^\circ$  to  $90^\circ$  means for every  $0^\circ \leq \theta \leq 90^\circ$
5. calculate rho value using equation one
6. Round rho value to integer using equation  $\rho' = \text{round}(\rho)$
7. Let rho value obtained is 670 and index of vote matrix [670,0] will get one vote because angle in loop now is  $0^\circ$
8. increase vote of  $\rho, \theta$  value obtained in voting algorithm using equation votes  $(\rho', \theta') = \text{Votes}(\rho, \theta) + 1$
9. Finally index of vote matrix  $(\rho', \theta')$  getting maximum votes are the output of the system
10. Block programming of Verilog is used in simulation code
11. Firstly input and output ports of the system are given
12. Then signal flow direction and data-types of I/O ports are given
13. Registers, wires, global variables and constants variables are defined
14. Cardiac core 4.0 is used to find sine and cosine values of input angles as well as maximum rho value
15. always block is defined which repeat itself at positive edge of system clock
16. All loops used in code are initialized
17. Then voting procedure is given in code and votes are stored in registers

### V. EXPERIMENTAL RESULTS

Complete steps of system's code is explained in section IV along with voting algorithm. Firstly system algorithm is simulated in MATLAB R2012a. First image shown in fig. 3 is given as input, Then voting algorithm is performed. Final vote matrix called here as Hough Matrix is shown in second image of fig. 3. Final rho and angle value  $(\rho', \theta')$  obtained from voting algorithm is given further to MATLAB Standard functions for finding lines with exact location in given image. Final output image is constructed with output parameters obtained in voting algorithm, shown in third image of fig.3.

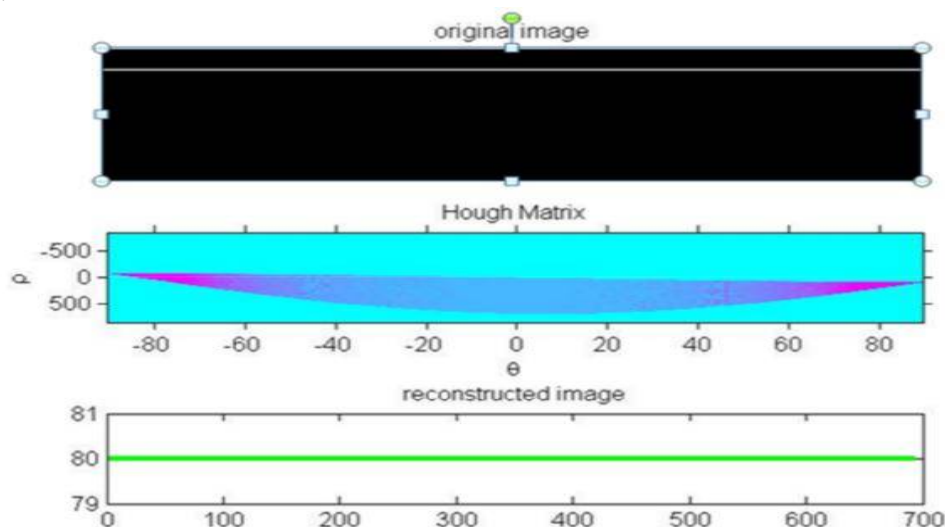


Fig. 3. MATLAB Simulation results

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Table one shows MATLAB simulation results, Image shown in fig. 3 is given as input and final rho value obtained is 774 for angle 90°. Third and fourth row gives details computations of voting algorithm.

Parameters	Values
$\rho$ Value	774
$\theta$ Value	90°
Additions in lac's	2.48
Multiplications in lac's	12.44

Table 1. Computation results

After verifying the voting algorithm of this system in MATLAB it is simulated in Xilinx. Fig. 4 shows schematic diagram of UUT. It shows input ports, system clock, signal flow, output ports and various blocks used in system.

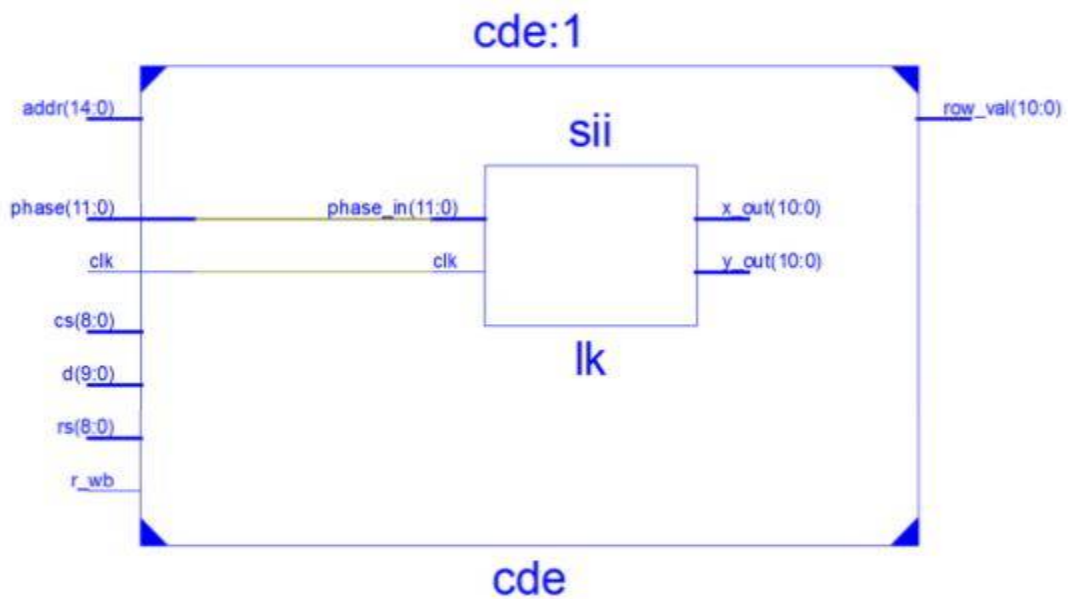


Fig. 4. Schematic diagram

System code is written using Verilog module and it is synthesized. Then implement design operation is performed after that timing constraints are generated. System clock chosen is of 20 ns. Timing details are given in table 2.

Met	Constraints	Check	Worst Case Slack	Best case achievable	Timing Errors	Timing Score
Yes	Autotimespec constraints for clock net clk_BUFPGP	SETUP HOLD	0.392 ns	3.509 ns	0	0

Fig. 5. Timing constraints diagram

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Table 3 gives details about device utilization of this system. This values are taken from synthesis report generated after synthesis of code. Values shown here are used values out of total available devices in XC6SLX45.

Devices	Used Values
Slice Registers	516
Slice LUTs	601
LUT-FF pairs	468
Bonded IOBs	13
Buffers	1

Table 2. Device Utilization

Input binary image obtained from MATLAB preprocessing of size 20x2 is stored first in distributed register bank memory and then voting algorithm is executed in always block of code. System analysis values are given in table 3. Maximum image size that can be processed is of 512x512. Total distributed register bank memory used by this system for input image is of 2315 MB and totla time required in synthesis is 3.509 ns.

Parameters	Values
Maximum image size	512x512
Distributed memory used in synthesis	2315 MB
Total time required in synthesis	3.509 ns

Table 3. System analysis

## VI. CONCLUSION

Hough transform is used to detect various shapes in an image. Xilinx simulation result is obtained and FPGA can be used to provide real time implementation of Hough transform. This system can process maximum images size of 512x512. Images with complex image size require more Computations and processing time so this system is useful for images with small sizes.

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