

Design and Implementation of 2.4GHz MMIC Power Amplifier Using ADS Software

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ABSTRACT: This paper contends the design of MMIC power amplifier for wireless application by using 0.15 μ m GaAs Power Pseudomorphic High Electron Mobility Transistor (PHEMT) technology with a gate width of 100 μ m and 10 fingers at 2.4GHz. The 2.4GHz power amplifier can be applied for wireless applications such as Wi-Fi and WPAN. Software ADVANCED DESIGN SYSTEM (ADS) is used to simulate schematic and layout of the power amplifier in order to obtain the best performance of the power amplifier.

KEYWORDS: Power Amplifier, MMIC, Lumped components, WIN components and ADS

I. INTRODUCTION

A Typical MMIC or RFIC design flow is to start with topology analysis with respect to specifications.

Table.1: Operating conditions

Parameter	Value
V_{dd}	2.5 to 3 V
V_{bias}	-1 to 0 V
Impedance matched Z_{in}/Z_{out}	50 Ω

Table.1 shows the operating conditions for the design of power amplifier at 2.4GHz. Table II shows the different parameter values to be met after the simulation of the final layout to ensure the design to be perfect.

Table.2: Parameter values

Parameter	Value
Higher Linear Gain	24 dB – 30 dB
Power Gain at 1 dB Compression Point	22 dB – 29 dB
Pout at 1 dB Compression Point (P1dB)	24 dBm – 33 dBm
PAE at 1 dB Compression Point	15% – 26%
3rd order Intermodulation (IM3) ($\Delta f = 10$ MHz, Pout = 17 dBm)	35 dBc – 47 dBc
High Linearity, OIP3	-
Drain Current, Idd at 1 dB Compression Point	350 mA - 1000 mA
Input Return Loss S(1,1)	- 10 dB(Min)

II. BLOCK DIAGRAM

The design approach is one of the major issues in modelling any power amplifier mostly when more than one amplifier is part of the design. There are three different kinds of topologies push-pull amplifier, balanced amplifier and interstage amplifier. In this case as output power was not very high and most the important concern was to have output as linear as possible and chip size as small as possible, push-pull power amplifier designs was not taken into consideration as they are known for high output power and high efficiency. Similarly balanced power amplifiers are good choice for having low VSWR at input as well as output i.e. good matching still this configuration was not used as it will only increase both the chip size and the complexity of the circuit by adding some quadrature hybrids for having balanced signals which is at time hard to achieve, and also good matching was possible without them. Hence the new approach was implemented in interstage topology to achieve good linearity and also small size.

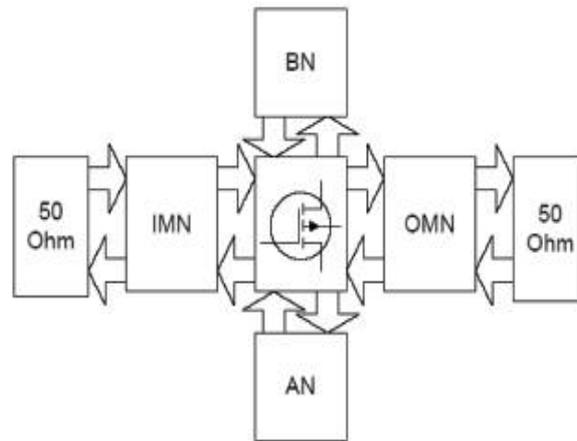


Fig.1: Block diagram

III. DESIGN PHILOSOPHY

The design of each sub-circuit components of the PA was first done using ideal lumped elements. Those ideal elements were replaced using the corresponding models from WIN design kit. Resistors and capacitors were easy to synthesize, but inductors had to be carefully modelled using an iterative tuning process. Connection of these WIN foundry components were accomplished using tee, taper, bend and micro-strip transmission line also available in WIN design kit.

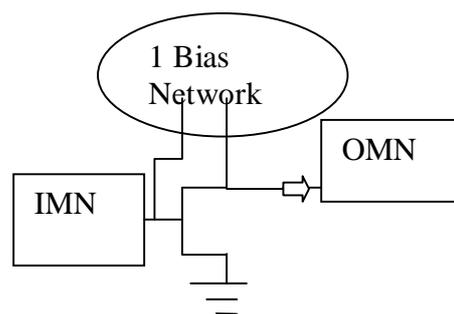


Fig.2: Single Stage Power Amplifier Topology

Amplifier

Operating point: The Fig.3 shows the I-V characteristics when V_{ds} is swept from 0V to 7V, but in the final stage of design the amplifier was biased at $V_{ds} = 3V$ and $V_{gs} = -0.9V$.

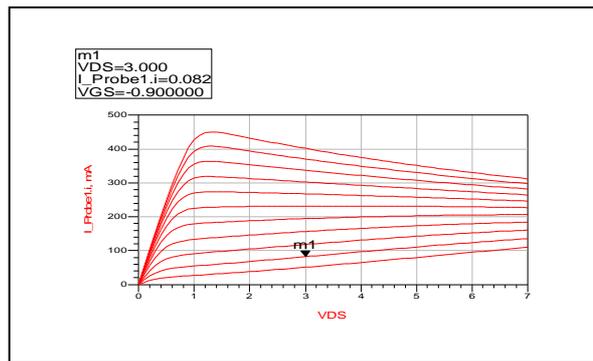


Fig.3: I-V characteristics

Matching Network: The matching network was designed to work over a large bandwidth. Both input and output matching network is designed for amplifier.

Biasing Network: The biasing network includes DC feed and DC blocks in parallel leading to the ground. After tuning and optimizing the circuit this DC feed and block at the gate bias became the part of the matching network.

Feedback Loop Circuitry: The transistor PHEMT was provided with feedback with a resistor and a capacitor. The capacitor is used to block the DC through the feedback it reduces the power added efficiency but less power is wasted by thermal dissipation. The main purpose includes this feedback network is to stabilize the output.

Results: The result are observed in the below figures. The output power obtained was above the required and well within the linear region so the driver stage gave a high gain which made the task easier for the amplifier to produce required output power within the linear region with less clipping in the output voltage.

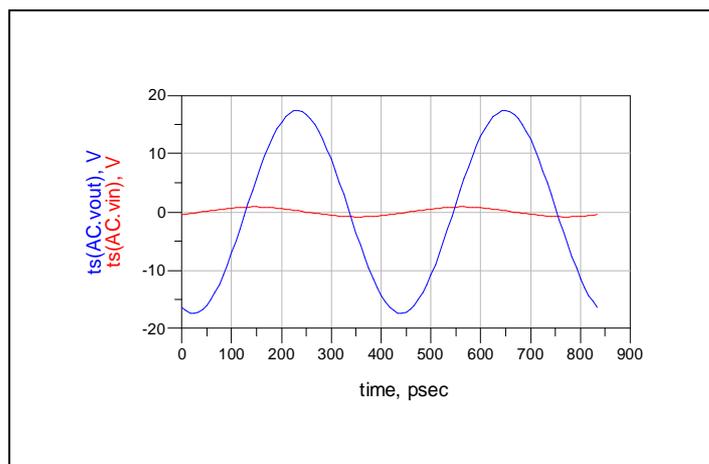


Fig.4: Vin v/s Vout

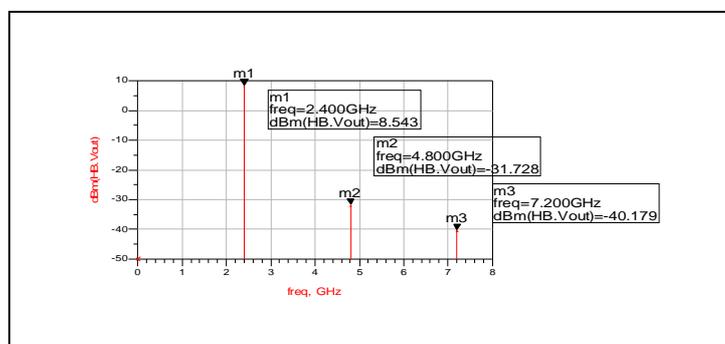


Fig.5: Harmonic Spectrum

The output voltage (V_{out}) is shown in the [Fig.5 for fundamental harmonics and as we can see second harmonics are well suppressed to -31dB compared to the fundamental.

IV. POWER AMPLIFIER CIRCUIT

After the design for amplifier was completed, the following job was just to build a schematic including lumped components. Input impedance and output impedance of the amplifier are measured in ADS and matching network is designed using lumped-elements. Lumped elements are replaced with WIN components in the matching network. Good results are observed after tuning the matching network consisting of capacitors and inductors. Table.3 shows the observed results after testing the pre-layout schematics. Micro-strip line, tee and m-corn, are used and better simulation results can be observed after tuning of the post-layout, which can be seen in Table.3 compared with pre-layout.

Table.3: Summary of power amplifier performance

Parameter	Post-layout
S(11)	-10.5
S(22)	-9.65
S(12)	-15.82
S(21)	8.39
Stability factor	1.23

V. SCHEMATIC RESULTS

When the amplifier stage is connected with the micro-strip transmission lines, tee and M-corn the entire power amplifier can be simulated for small signal and large signal performance.

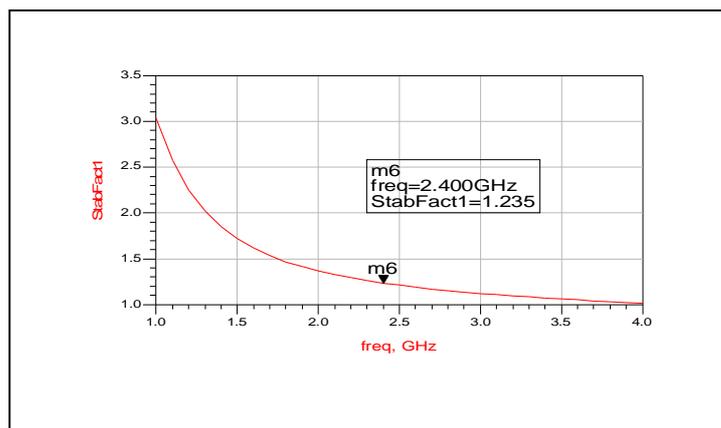


Fig.6: Stability Factor

Fig.8 shows the power amplifier is unconditionally stable over the bandwidth.

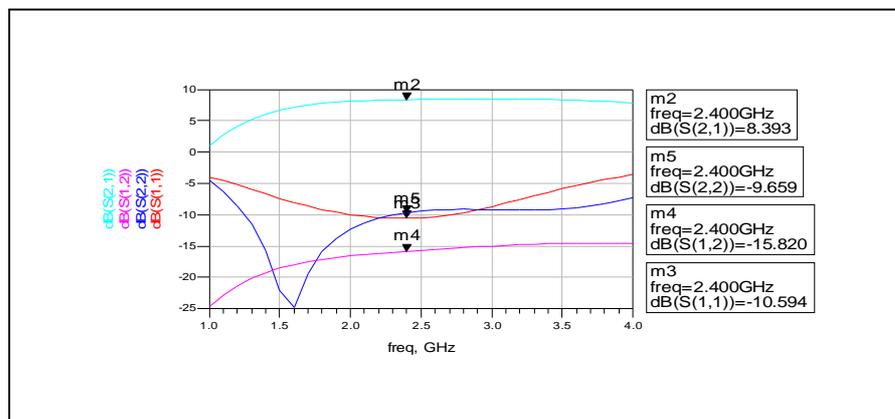


Fig.7: S parameters

The simulated performance of the amplifier was very encouraging. Fig VIII shows the s-parameters for the amplifier.

VI. FINAL LAYOUT

We use PHEMT process which is based on a 100 μ m GaAs substrate thickness. The layout is shown in Fig.9.

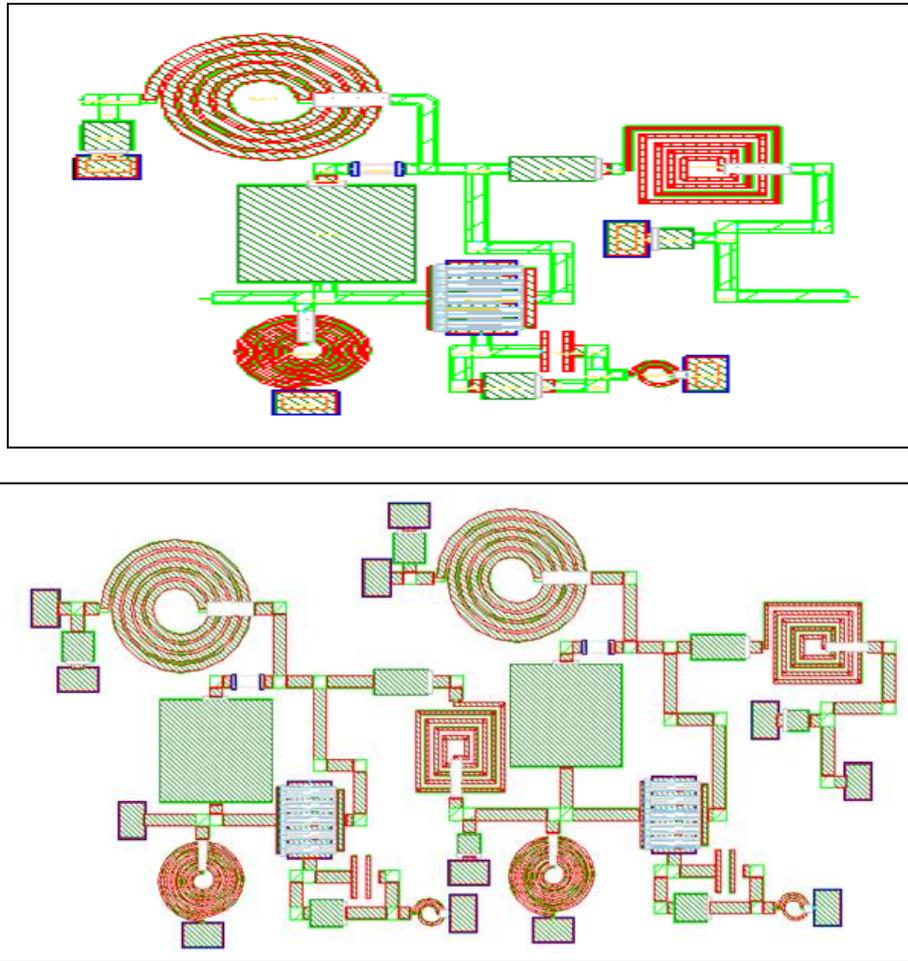


Fig.8: Final Layout of Two Stage Amplifier

The main features of the layout are

- Tee
- M corn
- Air bridge capacitor
- Round air bridge cross inductor
- Square air bridge cross inductor
- TFR (Thin Film Resistor)
- MESA resistor
- Double metal micro strip line

VII. TEST PLAN

In order to measure the power amplifier after WIN foundry fabrication it is necessary to place DC needle probes to provide individual bias to the gate and drain of the transistor, RF probes will come in from the top and left side of the chip for input and output, respectively.

VIII. CONCLUSION

After the successful completion of design, the following conclusion is observed.

The chip size is small but can be reduced further. Increasing the NOF (Number of Fingers) or gate width can increase the linearity of output power. In this work, MPA operating at 2.4 GHz respectively were designed for wireless

application by using 0.15 μ m GaAs Power Pseudomorphic High Electron Mobility Transistor (PHEMT) technology with a gate width of 100 μ m and 10 fingers. Software ADS was used in the designing process. It has been demonstrated that at a 3.0 V drain voltage, the amplifier has achieved 17.265 dB small-signal gain S₂₁, input and output return loss of 16.310 dB and 14.418 dB, P_{1dB} of 14.862 dBm with 12.318% power-added efficiency (PAE) for 2.4 GHz power amplifier. The designed MPA are in unconditionally stable condition due to the stability factor for the MPA are higher than 1 at the whole range of frequency. The die sizes of the amplifiers from the layout design are 1 mm x 2.08 mm MPA respectively.

IX. FUTURE SCOPE

The design of single-stage amplifier can be extended to two-stage amplifier design to meet the specification still more efficiently. In order to improve the performance of the system and achieve a higher output power, the matching system should be designed in a specific way. So an interesting future work would be to improve the ADS model of the transistor by extracting its parameters and bias characteristics and then to redesign the power amplifier which should lead to a good improvement in the power performance.

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