

Low Power Testing Techniques for IP Core-based SOC: A Survey

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ABSTRACT: Power and energy consumption is the major issue for the current generation in VLSI testing. This may lead to severe hazards to the circuit reliability. While considering the modular design approach in SOC it has increased the test power issue. Low power is very much essential because of its cost, performance variation and some technology related problems. The most common problem is, it reduces the life of battery when online testing is considered. This paper deals with the survey of testing in VLSI circuits using both internal and external testing. Also the available low power testing techniques are recognized for their IP core-Based SOC.

KEYWORDS: IP core-Based SOC, LFSR architecture, ATPG algorithm.

I. INTRODUCTION

For the design and test engineers the power consumption is the major problem. The aspects to decrease the amount of power consumption during the process of normal function mode, the power consumption problem is increased further during the process of testing. Normally the circuit perhaps consume 4 to 8 times power during test mode when compared to normal mode. Thus semiconductor industry is often expecting for low power testing techniques.

The modular design approach is widely suitable for SOC in order to reduce the cost and time for end users. This paper is categorised as follows. Section 2 describes the various process that results in high power consumption during test. Section 3 gives various types of low power testing techniques. Section 4 contains adaption of each types with respect to IP core-Based SOC. Section 5 gives the clear conclusion of low power testing survey.

II. LOW POWER TEST

ASIC or SOC always needs non destructive test which clears all the power constrains that are described in the design phase. The other method using the theorem of current testing, larger the amount of power consumption during test than during functional mode. This section explains the causes and effects of this type of power consumption.

A. CAUSES OF HIGH POWER CONSUMPTION

There are several causes that usually results in problem of more test power consumption. From these problems the main causes are described below.(i) In the toggle rate the test efficiency will have high correlation so during test mode the switching activity is more or increased than normal mode.(ii) The increased energy and power dissipation is acquired by using SOC parallel testing. (iii) The design for testability(DFT) in the circuit is to reduce the complexity of test which is always idle during normal operations whereas intensively used in the process of testing mode.

B. EFFECTS OF HIGH POWER DISSIPATION

The high power dissipation effects during the test will reduce the life IC's. It also affects the cost, reliability, autonomy, performance variation, yield related issues. The various other types of effects of high power

consumption are as follows. (i) Due to high power dissipation the growing need of at-speed testing can be minimised. This does not affect the stuck at fault test but delay fault becomes tedious process. (ii) After the process of wafer etching in functional testing of the die the unpackaged bare die will have low power or heat dissipation. (iii) The electro migration causes the erosion which leads to failure of the circuit.

III. LOW POWER TESTING TYPES

A. LOW POWER TESTING TECHNIQUES FOR INTERNAL TESTING

3.1.1.LFSR Architecture

The linear feedback shift register (LFSR) is used to reduce the power consumption in testing process. The test pattern generator and response checker are the important component of built in self test (BIST) architecture which uses LFSR as a main component .

3.1.2. Useful vector generation

Many unused pattern which do not involve fault dropping are the reasons of wastage of energy in LFSR and CUT. In order to minimize energy consumption, the state transition of LFSR should be modified by designing mapping logics. so that all the useful vectors are obtained for the exact sequence. The state transition of the LFSR are usually obtained with respect to exact sequence in modification of LFSR tuning.

3.1.3. Memory using different testing strategy

In the literature the reordering of read and write access are obtained in the reduction of various transition technique in memory testing. If the current accessed row bank is pre charged other than pre-charging the entire memory array. This process is called low power test mode which will result in required power saving for the pre charge. The result is calculated in the memories 130 and 90 nm technologies. With the use of virtually zero overhead the required power reduction can be achieved.

B. LOW POWER TESTING TECHNIQUE FOR EXTERNAL TESTING

3.2.1. Ordering technique

In order to decrease the switching power the researchers have widely found the test vector type of reordering technique. Reordering based on hamming distance is explained in paper [14]. To minimize switching activity during testing is done with the help of artificial intelligence. Vector ordering is processed using Girard's approach.

3.2.2.ATPG Algorithm in low power

In external testing the reduction of power consumption is achieved by ATE (Automatic Test Equipment). In test data set the number of transition is required for this method. To examine the signal dependency and to form circuit partition the novels can chain division algorithm is used. The classical D- Algorithm is a constrained version of high and low frequency effect in the test sequence. The ATPG reduces the growth of test pattern count when it is compared with detection number. When the reduction number increases the peak number decreases.

3.2.3.Exploring do not care bits

ATPG usually contains a large uncompact test data which is called as do not care bits. This propose the low power launch off capture transition test. This method gives an average increment in the dynamic power and leakage power. This is widely used in ATPG in order to reduce the consumption of power. It presents a trade off in dynamic and static power consumption.

IV. LOW POWER TESTING TECHNIQUE IN IP CORE-BASED SOC

In IP core based SOC BIST plays a major role since it is the most favourable testing method. Testing allows design of intellectual property of preservation. ATPG or fault simulation are not well suited for IP cores.

A. CHARACTERISTICS OF POWER REDUCTION SUITABLE TO IP CORE BASED SOC

The characteristics of power reduction that is suitable for IP core based SOC are as follows. (i) It cannot be dependent on the knowledge of internal structure of design. (ii) The modification of internal design is strictly prohibited. (iii) The addition of hardware equipments as per requirement without any change in the available I/O pin configuration is possible. (iv) The hardware should deal with ready to test sequence compared to the test architecture. (v) The net list of design testing tools like ATPG or fault simulation should not be the main source. The available techniques are compared with the above characteristics

B. MEMORY USING DIFFERENT TESTING STRATEGY

The memory using different testing strategies can be executed only if memories required. Since it is based on the memory it cannot be used for functional blocks.

C. ORDERING TECHNIQUES

The implementation of this method (i) The hardware should deal with ready to test sequence compared to the test architecture. (ii) Test data is required for test sequence. (iii) It is done without the influence of internal details of design. (iv) Additional hardware is required to reorder the test pattern sequence. (v) Internal structure modification cannot be done.

D. EXPLORING DO NOT CARE BITS

This method is implemented by (i) Additional hardware is not required. (ii) it is done without the influence of internal details of design. (iii) internal structure modification cannot be done. (iv) It requires detailed test sequence which is a test data set. (v) It always uses test data bit sequence compared with test architecture or test vector sequence.

V. CONCLUSION

This survey paper clearly explains about low power testing technique for IP core-based SOC. In this paper first the causes and the effects of the high power consumption is discussed which is followed by various types of low power testing techniques which includes both internal and external testing. Then the characteristics of IP core-Based SOC is discussed. Each available category in reduction of power of is compared with this ideal model. From this characteristics it is concluded that "ordering technique" and "exploring do not care bits" are best suited technique for IP core-Based SOC since other method required internal details of circuit.

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