

FPGA Remote Wireless Automatic Meter Reading System Based On Bluetooth

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ABSTRACT: The traditional method of energy meter billing is a long outdated, inefficient and time consuming one. It was replaced long back with the new and a better efficient method of metering. The paper here presents an innovative system which is an up gradation to the latest energy metering method yet to be implemented also along with the designing of a access to the billing information from anywhere round the globe. The communication takes place through Bluetooth module wirelessly. The date will be present in the computer having a Bluetooth dongle. It will be the billing location. The meter readings are sent time to time from the electricity meter having the Bluetooth to the billing location. Accordingly the data is also periodically updated. The entire system is designed using VHDL coding in FPGA and is implemented using Lab VIEW.

KEYWORDS: Energy meter, Bluetooth module, VHDL coding, FPGA Spartan 3E, Lab VIEW.

I.INTRODUCTION

The electricity delivery systems of most countries were built almost 100 years ago, where electricity travels hundreds of thousands of kilometers from central power plants to consumers with major energy losses. The structure of the current power grid is not well suited to meet the future energy demand. Hence, the SG has become one of the most important items on the agenda of many governments and utilities, since it is the key to increasing the recognition of the current problems and meets the electricity demand. Traditional power grids are being transformed into Smart Grids (SG) using advanced information control and communication technologies to offer higher reliability, security and efficiency in power systems. Smart Grid consists of smart meter for Home Energy Management via energy efficient communication technology. To support both dynamic pricing and a two-way flow of electricity between homes (or micro grids) and smart meters are being widely deployed. In Compared to conventional analog meters, smart meters measure power consumption at a much finer granularity.

Currently, the electricity meters are installed on consumer's premises and the consumption information is collected by meter-readers on their fortnightly or monthly visits to the premises. Meters in the past, and today in a few countries are electromechanical devices with poor accuracy and lack of configurability. Theft detection is also a challenge. This method of billing is also not suitable for the electricity supply company because it gives inaccurate account of the overall electricity consumption in Manuscript received Recent developments in this direction seem to provide opportunities in implementing energy efficient metering technologies that are more precise accurate and error free.

The proposed methodology overcomes the disadvantages of the existing technology by developing efficient home energy management using smart meter architecture. In this method to design energy efficiency, and low complexity of smart meter for home energy management using smart grid communication based FPGA. The new architecture of FPGA implementation of smart meter is one method reading and processing consumed energy data of each home appliance automatically with computer and communication and also gives the accurate account of the overall electricity consumption through main wireless communication protocol,

Bluetooth is chosen as lower layer communication protocol. With these applications, the standard is optimized for low data rate, low power consumption, security and reliability.

II. BLOCK DIAGRAM OF FPGA ENERGY METER READING SYSTEM

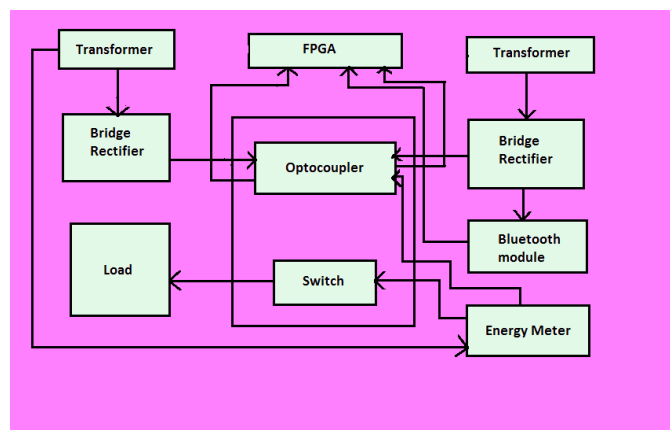


Figure1 Block Diagram implemented in FPGA

POWER SUPPLY

There are many types of power supply. Most are designed to convert

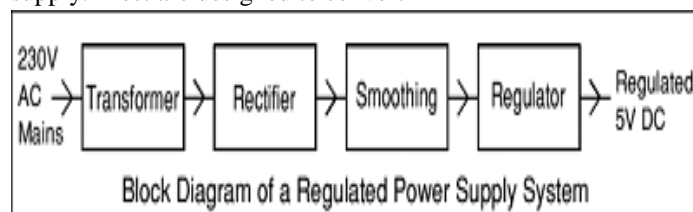


Figure 2 Block diagram of a supply diagram

regulated power

Voltage AC Mains electricity to a suitable low voltage supply for electronic Circuits and other Devices. A power supply can be broken down into a series of blocks, each of which performs a particular function.

- Transformer - steps down high voltage AC mains to low voltage AC.
- Rectifier - converts AC to DC, but the DC output is varying.
- Smoothing - smoothes the DC from varying greatly to a small ripple.
- Regulator - eliminates ripple by setting DC output to a fixed voltage.
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OPTO COUPLER

The function of OptoCoupler is isolate to the control circuit from power circuit. Pulse width modulation signal (PWM 1 to PWM 12) comes from FPGA Processor. The function of Opto Coupler is isolate to the control circuit from power circuit. Pulse width modulation signal (PWM 1 to PWM 12) comes from FPGA Processor. This signal is not directly fed through a power circuit. Suppose Control Circuit (FPGA) is connected to power circuit without isolation circuit, the control circuit may get affected. So we need to isolation circuit interface between power circuit and control circuit.

FPGA SPARTAN 3E

Very low cost, high-performance logic solution for high-volume, consumer-oriented applications
Proven advanced 90-nanometer process technology

- Multi-voltage, multi-standard Select IO interface pins
- Up to 376 I/O pins or 156 differential signal pairs
- LVCMOS, LVTTTL, HSTL, and SSTL single-ended signal standards
- 3.3V, 2.5V, 1.8V, 1.5V, and 1.2V signalling 622+ Mb/s data transfer rate per I/O
- True LVDS, RSDS, mini-LVDS, differential HSTL/SSTL differential I/O Enhanced Double Data Rate (DDR) support
- DDR SDRAM support up to 333 Mb/s.

FPGA DESIGN AND PROGRAMMING

To define the behaviour of the FPGA, the user provides a hardware description language (HDL) or a schematic design. The HDL form is more suited to work with large structures because it's possible to just specify them numerically rather than having to draw every piece by hand. However, schematic entry can allow for easier visualization of a design.

Then, using an electronic design automation tool, a technology-mapped net list is generated. The net list can then be fitted to the actual FPGA architecture using a process called place-and-route, usually performed by the FPGA company's proprietary place-and-route software. The user will validate the map, place and route results via timing analysis, simulation, and other verification methodologies. Once the design and validation process is complete, the binary file generated (also using the FPGA company's proprietary software) is used to (re)configure the FPGA. Going from schematic/HDL source files to actual configuration: The source files are fed to a software suite from the FPGA/CPLD vendor that through different steps will produce a file. This file is then transferred to the FPGA/CPLD via a serial interface (JTAG) or to an external memory device like an EEPROM. The most common HDLs are VHDL and Verilog, although in an attempt to reduce the complexity of designing in HDLs, which have been compared to the equivalent of assembly languages, there are moves to raise the abstraction level through the introduction of alternative languages. National Instrument's Lab VIEW graphical programming language (sometimes referred to as "G") has an FPGA add-in module available to target and program FPGA hardware. The Lab VIEW approach drastically simplifies the FPGA programming process.

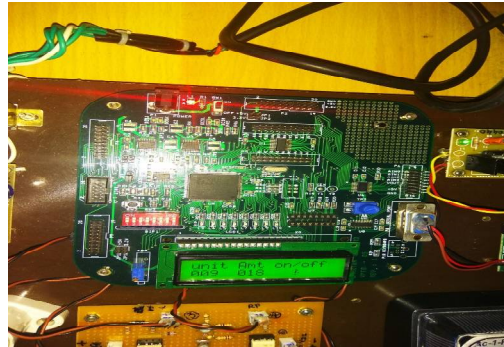
To simplify the design of complex systems in FPGAs, there exist libraries of predefined complex functions and circuits that have been tested and optimized to speed up the design process. These predefined circuits are commonly called IP cores, and are available from FPGA vendors and third-party IP suppliers (rarely free, and typically released under proprietary licenses). Other predefined circuits are available from developer communities such as Open Cores (typically released under free and open source licenses such as the GPL, BSD or similar license), and other sources.

In a typical design flow, an FPGA application developer will simulate the design at multiple stages throughout the design process. Initially the RTL description in VHDL or Verilog is simulated by creating test benches to simulate the system and observe results. Then, after the synthesis engine has mapped the design to a net list, the net list is translated to a gate level description where simulation is repeated to confirm the synthesis proceeded without errors. Finally the design is laid out in the FPGA at which point propagation delays can be added and the simulation run again with these values back-annotated onto the net list.

BLUETOOTH

Bluetooth is a short-range (10-100) wireless communications technology. Bluetooth Was Originally a Cable-Replacement Technology Uses the radio range of 2.45 GHz. Theoretical maximum bandwidth is 1 Mb/s. Allows up to 8 devices communicate in a local network called a Piconet, also known as a Personal Area Network or PAN.

III. RESULTS AND DISCUSSION



The above figure is the output of the entire system. The value shown in the LCD display is the meter reading. The same meter reading is shown in the substation by using Lab VIEW software. This system is achieved by using Bluetooth Protocol. Further enhancement can be done by using GSM protocol.

IV. CONCLUSION

As discussed in this paper, a new architecture of home energy management using Bluetooth communication has revisited the need for domestic energy management for efficient consumption of electricity. Consuming electrical energy efficiently results in reducing peak load, lowering electricity bills and minimizing the power consumption. This proposed methodology has discussed home energy management schemes where different energy scheduling, pricing schemes have been applied to get economical and social advantages.

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