

# FPGA Implementation of High Speed MAC Unit

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**ABSTRACT:** In the field of digital signal processing systems as well as in general processors computational speed and performance plays a pivotal role as they are widely used in filtering, convolution, DWT circuits, signal coding and optical communication system, multimedia information processing. Fundamental DSP algorithms depend heavily on multiply-accumulate performance. A high speed processor depends on the multiplier as it is one of the key hardware blocks. In order to obtain a best processing speed MAC unit is used. The speed of multiplication and addition determines the execution speed and performance of entire setup. In this project we will design and analyze the performance of MAC unit and thus, the area and delay parameters are optimized using various multipliers such as Array, Wallace tree multipliers, Vedic multipliers etc.

**KEYWORDS:** MAC (Multiplier and accumulator) UNIT, Wallace tree, Vedic multiplier.

## I. INTRODUCTION

Arithmetic operations contain several fundamental functions like Addition, Subtraction, Multiplication, and Division and so on. Multiplication is one of the basic and mostly used functions in arithmetic operations [1]. Arithmetic logical unit and multiply and Accumulate (MAC) are the basic blocks in Digital Signal Processing applications and in these operation multiplication is the basic function to be implemented [1]. In Convolution, Fast Fourier Transform (FFT) and microprocessors we implement DSP applications in their arithmetic and logic units [2]. We need high speed multipliers in DSP processors as these multiplication operations decide their execution time. Currently, the execution time of a digital signal processing chip still depends on the multiplication time. The recent improvement of technologies in many digital and signal processing applications, the need of high speed processors increased. In many signal and computer applications, high output of the arithmetic operations is needed to achieve the required performance [3]. Multiplication is one of the operations in arithmetic operations in such applications and to develop a high speed multiplier circuit became the main interest over many years. By reducing the time delay and the amount of power consumed we can meet the requirements of many applications [3]. This thesis presents different multiplier architectures and there implementation using Vedic Mathematics. We need to optimize at all levels that involve the design to minimize power consumption. The technologies and algorithms used to implement the digital circuits must include this optimization, circuit design, topology used to implement the circuits and the level at which the algorithms are designed. Digital multipliers are the main components used in any digital architecture. To implement any operation we need fast, reliable and efficient components. We have different types of multipliers available depending on the arrangement of the components.

In many DSP algorithms, the performance of digital signal processor algorithm depends on the multiplier that lies in the critical delay path. The speed and time delay of multiplication operation are important in DSP and also in the general processor. Previously a set of addition, subtraction and shift operations are used to implement the multiplications. Previously there were a lot of algorithms described to perform multiplication operation, each offering different advantages based on the speed, circuit design, effective area, and time delay, power dissipation and consumption. In computing system the major block is multiplier. The relation between the circuit design and constancy is, the amount of circuitry involved i.e. size of the device (n) is directly

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proportional to square of its constancy i.e. constancy is having  $n$  gates. For all the multiplication Algorithms that are used in DSP applications, the latency and execution time are the two major terms in the time delay perspectives. While computing a function when a latency delay occurs, it's nothing but calculation of how much time the inputs of a device are constant; it is the final result on the outputs. Multiplier is a major source of power dissipation and it's also a high delay block in the processor. Due to the high delay the power dissipation is also high so we plan minimize power consumption we also require to minimize the delay by using various delay optimizations [4]. In many of the digital signal processors (DSPs), digital multipliers are the main component used in it and their speed is largely determined by the speed of the DSPs [2]. The basic multipliers used in digital systems are Booth multiplication and Array multiplication. The execution time of the array multiplier less as the partial products is calculated individually.

Booth multiplication is another multiplication algorithm used in digital hardware. For exponential operations and high speed multiplication we need large booth arrays. Due to the need of binary multipliers in Digital signal processor, due to these it has always been an active field of research and a number of  $t$  multiplication algorithms have been reported in many [4]. Hence, firstly Urdhva tiryakbhyam sutra is implemented to digital system by coding it in vhdl and then it is synthesized in quartus II .The architecture obtained from quartus II is almost similar to the architecture of array multiplier and the number of multiplications are also same. This algorithm also determines the effectiveness to reduce the  $N \times N$  multiplier design module into a  $4 \times 4$  multiplier design modules. Then we discussed Nikhil am Sutra which is more efficient for multiplication of bigger number. Since it reduces the complex multiplications into a simple one. The proposed Vedic multiplication is demonstrated to show its effective delay, efficiency and hierarchy design by consider an example of  $4 \times 4$ -bit multiplication and then it is reduced to the operation of a single  $2 \times 2$ -bit multiplication. The Multiplier is implemented based on the Urdhva tiryakbhyam sutra which is one of the sutras of ancient India Vedic mathematics which means vertically and crosswise algorithm [4][5].

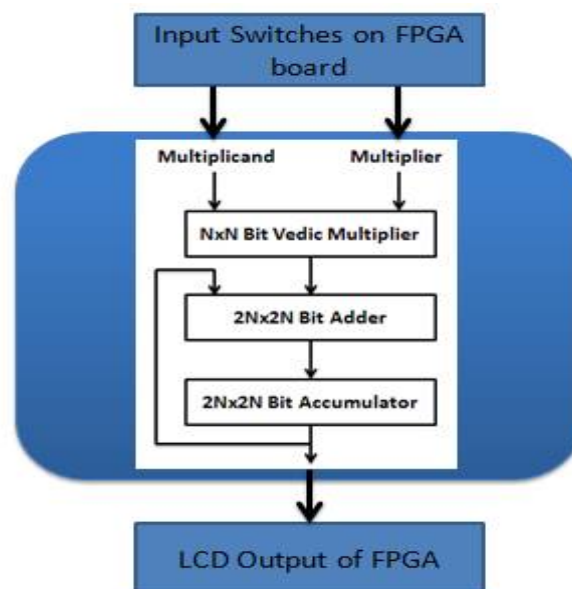


Fig.1 Mac Unit Structure

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## II. VEDIC MULTIPLIER

### A. 2-BIT VEDIC MULTIPLIER MODULE

The technique used for two, 2 bit numbers A and B where  $A=a_1a_0$  and  $B=b_1b_0$  as shown in Fig 1. First the LSB is multiplied which gives ultimate product of least significant bit (Vertical). The Least significant bit of multiplicand is multiplied with next higher bit of multiplier and added with product of least significant bit of multiplier and multiplicand of next higher bit (multiplicand). The sum gives the final product of second bit and carry is added with partial product obtained. The third corresponding bit is sum and fourth bit of final product is carry. The final product is  $c_2s_2s_1s_0$ . This method of multiplication is applicable to all types. The implementation of 2 bit Vedic multiplier module consists of four input AND gates and two half adders which is shown in Fig 2. The architecture of 2 bit Vedic multiplier is same as the architecture of 2 bit array multiplier. By Vedic method, the multiplication of 2 bit binary numbers does not have significant improvement in multiplier's efficiency. In 2bit Vedic multiplier, the total delay is only 2- half adder delays are same as the array multiplier.

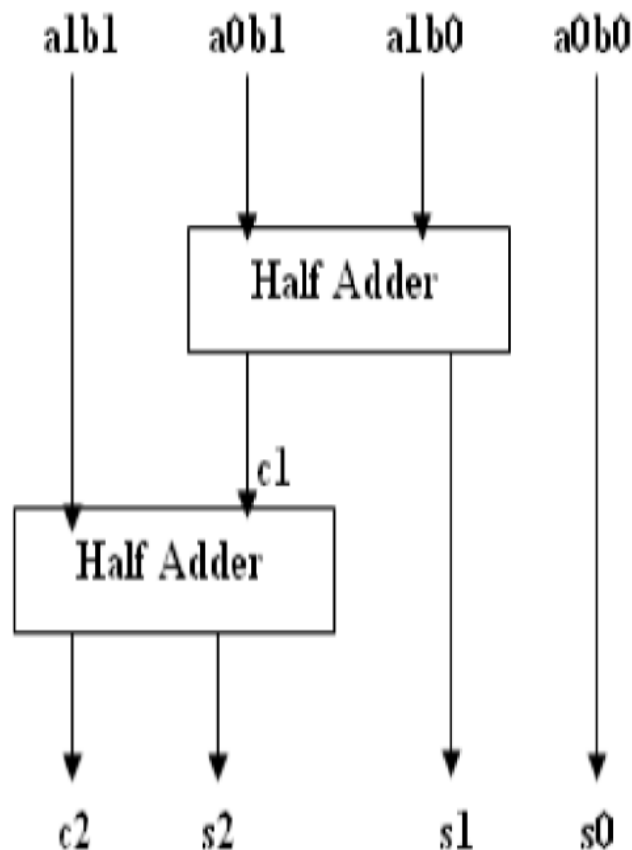


Fig.2 2x2 Vedic multiplier

### B. 4-BIT VEDIC MULTIPLIER MODULE

Evaluate the 4x4 multiplication by using  $A=a_3a_2a_1a_0$  and  $B=b_3b_2b_1b_0$ . The final result is  $S_7S_6S_5S_4S_3S_2S_1S_0$ . Divide A and B into two parts, say  $a_3a_2$  &  $a_1a_0$  for A and  $b_3b_2$  &  $b_1b_0$  for B. With the help of fundamentals of Vedic multiplication, taking two bit at a time and using 2 bit multiplier block.

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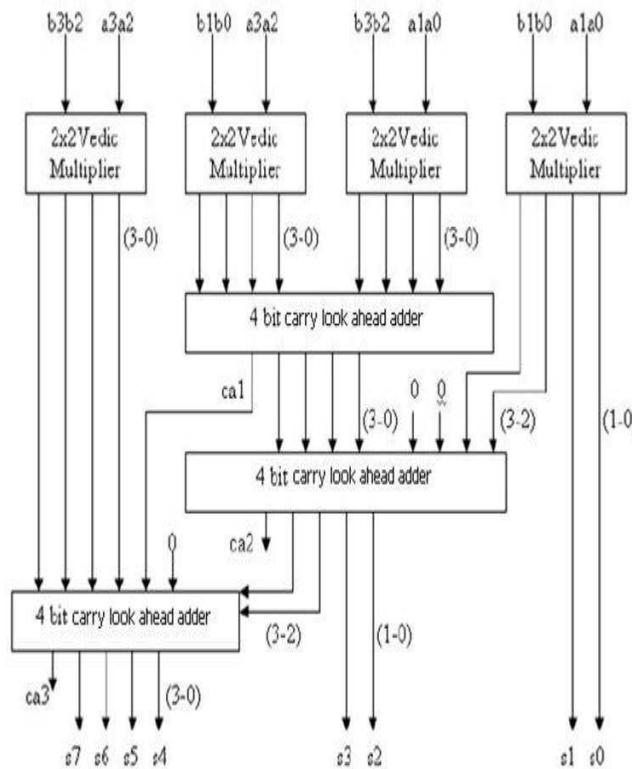


Fig 3. 4x4 Vedic multiplier

**C. 8-BIT VEDIC MULTIPLIER MODULE IMPLEMENTED USING VARIOUS MULTIPLIER**

Evaluate the 8x8 multiplication by using  $A=a7a6a5a4a3a2a1a0$  and  $B=b7b6b5b4b3b2b1b0$ . The final result is  $S15S14S13S12S11S10S9S8S7S6S5S4S3S2S1S0$ . Divide A and B into two parts, say  $a3a2a1a0$  &  $a7a6a5a4$  for A and  $b3b2b1b0$  &  $b7b6b5b4$  for B. With the help of fundamentals of Vedic multiplication, taking four bit at a time and using 4 bit multiplier block, The four bit multiplier block used here is executed using various multipliers like array, Wallace, Vedic multiplier. The projected multiplier architecture can be used to shrink the delay [6]. In the prevailing method, Vedic multiplier based on array multiplier erections and also new architecture introduced based on Ripple Carry (RC) adders which help to reduce delay. Reducing time delay essential for many applications.

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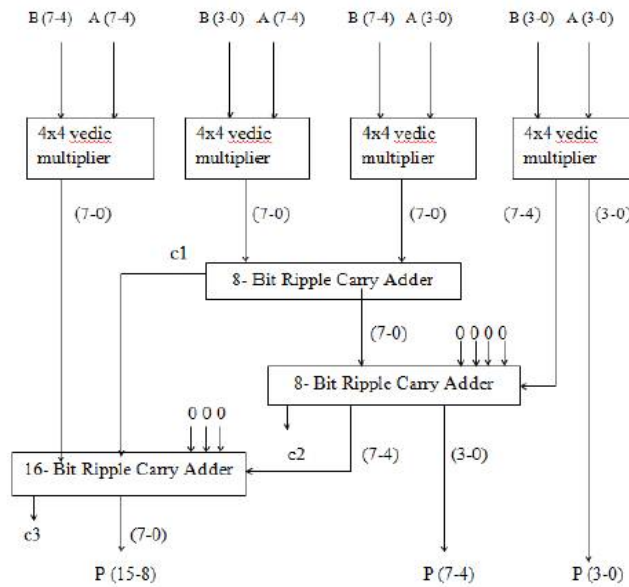


Fig 4. 8x8 Vedic multiplier

### III.SIMULATION OUTPUT

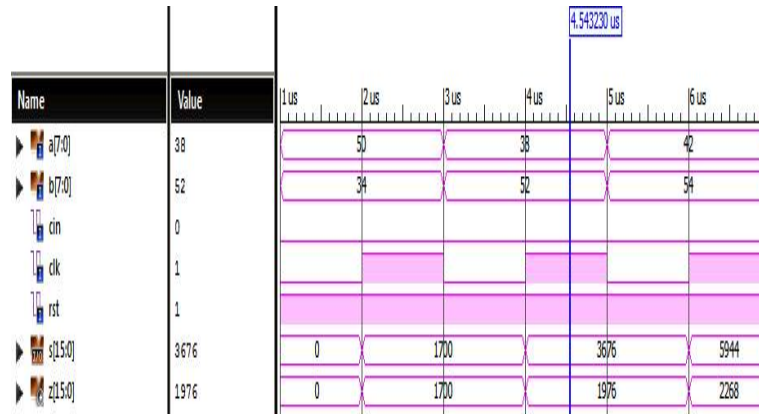
#### A. Simulation result of 4\*4 MAC Unit implemented using various multipliers using Vedic architecture



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**B. SIMULATION RESULT OF 8-BIT MAC UNIT USING VARIOUS MULTIPLIERS IMPLEMENTED IN VEDIC STRUCTURE**



**IV.RESULT**

**A. COMPARISON CHART**

The below table shows the different multipliers implemented in Vedic structure.

MULTIPLIERS	DELAY	NO OF 4-INPUT LUT'S	NO OF OCCUPIED SLICES
ARRAY 4*4	14.42ns	31	17
WALLACE 4*4	12.16ns	33	19
VEDIC 4*4	12.61ns	33	18

Table no 1. Comparison between various 4\*4 multipliers implemented using vedic structure

**B. COMPARISON CHART**

The below table shows the different multipliers result implemented using Vedic structure.

Multipliers in MAC	Delay	No of 4-input LUT'S	No of occupied slices
ARRAY 8*8	23.53ns	168	90
WALLACE 8*8	21.78ns	170	94
VEDIC 8*8	22.44ns	163	87

Table no 2. Comparison between various 8\*8 multipliers implemented using vedic structure

## V. CONCLUSION

In this research work a deep analysis and study work has been performed on different types of multipliers. Area and delay parameters of various multipliers were compared and analysed. In which Vedic multiplier structure found to be more efficient both in terms of area and speed parameters. So, An efficient MAC unit has been designed using various multipliers in Vedic structure. The design was implemented in FPGA. Hence, This system can be used in the real time application for providing good processing speed.

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