

# International Journal of Innovative Research in Science, Engineering and Technology

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## Traffic Light Controller Displaying Countdown using 7-segment Display

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**ABSTRACT:** Traffic problems on roads in the modern cities are increasing day by day as the number of vehicles on the road is increasing. Traffic lights control systems are used as the signalling devices for management of challenging traffic in cities. Over the years there is a drastic change in technology which is implemented to improve work efficiency, to reduce time losses. But irritating, poor traffic systems are available which in turn causes accidents. In order to reduce inconvenience, the system proposed in this paper has continuous down count display of waiting time. The main objective of the work is to simulate and synthesize the functionality to demonstrate Traffic Light Controller using state machines and to display countdown waiting for timer using 7 segment displays. The coding of the design is done in Verilog, the design simulation is done using Questa Sim and Xilinx. This system is also capable to modify the timings of traffic signals according to a requirement of the signals as the density of vehicles on the roads vary from place to place. The design has various benefits over traffic light controllers built with microcontrollers such as countdown display, low costs, ease in installation, simple structure, high reliability, maintenance and easier testing. This system is implemented using a state machine which is going to shift each state to next state when counter value waits up to a fixed time. After that colours of signals will shift automatically to next such as RED, GREEN and YELLOW. The system also considers delay unit for pedestrian, so it is a wider application-specific system.

**KEYWORDS:** Traffic lights control systems, continuous down count, 7 segment displays, Verilog, Questa Sim, state machines.

### I. INTRODUCTION

The main cause of the huge accidents is irresponsible driving and poor traffic control systems. There are many traffic control systems available but due to limited resources provided by available traffic systems with microcontroller or microprocessor are unknowingly leading to ever increase in travelling times and waiting time of people. The project provides the basic model of traffic light control system which has an additional feature of displaying a countdown timer on a 7-segment display. The main focus of work is that road users should get an exact time of wait for signals as and when user is at signals and also, we should have a system which minimizes waiting time. We want more efficient and less expensive system with use of evolving technology to meet the required objective. The problem we identified was, road users are unaware of time wasted in waiting for signals and even one cannot say anything about what will be the next signal which is going to be turned green? So, to avoid such a conflicting condition there is need of traffic light control system which will continuously display a countdown for all signals to make it user-friendly. It is very important as per as waiting time for signals at highways is considered to have such systems. To avoid any mischief with people on road due to unawareness of signals timing there should be some effectively smart system present and the interesting point here is we can make system smarter as and when required as it is electronic design developed with Verilog HDL

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Hardware Description Language. It is not a much tedious job but efficiency and cost of system differs from system to system. The key components of our work are traffic light control system works on the particular type of switching sequence of Green, Red and Yellow light signals in a specific way with given time limit form in program and sequence is generated with the help of a specific switching mechanism which controls a traffic light system as required sequence.

## II. BACKGROUND STUDY

There are many systems available like TLC (Traffic Light Controller) based on microcontrollers and microprocessors in many cities and many more are also present but major of the systems are not much known to community, there is lack of awareness about many present systems and also there are different ways of implementing same Traffic Light Control as with FPGA[2] or with ASIC or with PLD or with CPLD. Many systems are much costlier that they are hard to be implemented in large numbers. Verilog language is used as of the difficulty in writing a VHDL due to fully typed language which has to integrate the source code.

## III. MAIN BODY OF THE PAPER

### Verilog:

Programs for electronic chips are written with the help of Verilog Hardware Description Language. It is the language which is used in electronic devices that do not share a basic architecture of a computer. Relatively, Verilog is recent and it follows the coding methods of C programming language. Verilog uses weak typing in opposition to a strongly typed language like VHDL. It has the case sensitivity. Verilog is case sensitive, so it is not able to recognize a variable if the case used is not in a consistency with what it was early used. Hence, in short, Verilog is easier to learn than VHDL[3]. This is due to the popularity of the C programming language and also it makes most programmers familiar to the conventions used in Verilog. It has no concept of packages and all programming should be done with the simple data types which are provided by the programmer. Basically, a modelling language for a very efficient event-driven digital logic can be simulated initially, but further, it is pushed into use as a specification language for logic synthesis. Nowadays, one of the most commonly-used languages in digital hardware design are VHDL and Verilog HDL. Every chip (FPGA, ASIC, etc.) is virtually designed in parts using one of these two languages which combine structural and behavioural modelling styles[4].

### Xilinx:

The system is coded by using Verilog, this code can be dumped in FPGA development kit by using Xilinx ISE tools. When one opens a project file from a previous release the ISE software prompts a person to migrate the project. If the person clicks backup and migrate or migrate only the software automatically converts project file to the current release. After conversion of a project, one cannot open it in previous versions of ISE software. If the design includes IP modules that were created with the help of CORE Generator software or Xilinx platform studio (XPS) and need to modify these modules one may be required to update the core [1]. However, if the core netlist is present and one does not want to modify the core, updates are not required and the existing netlist is used during implementation. Here Xilinx is used for simulation of design for further implementation.

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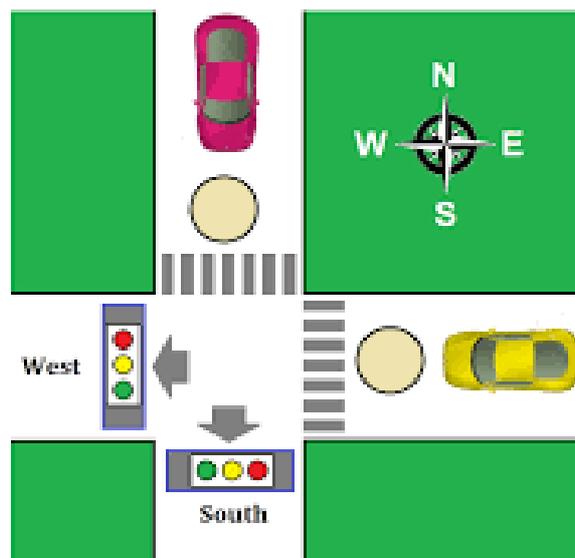


Fig1.Road structure for system.

## Finite state machine

Finite State machines are generally used for generation of control signal sequence. Mainly there are two types of state machines one is Mealy machines and other is Moore machines. The major difference between Mealy and Moore machines depends on methods of output generation. In Moore machines, output at any state is a function of current state. This shows that if state changes, the output also changes, But in Mealy machines, output is function of input as well as current state. A state machine can be divided into three parts as State register, Next-State Logic and Outputs. It is very important to model every part of the state machine in Verilog [1].

## IV. SYSTEM IMPLEMENTATION

### Road structure :

Generally, every traffic signal system has three signal lights. The green light which is on the bottom of the signal indicates road users to proceed, a yellow light which is located in the middle alerts to slow and to be prepared to stop, and red light which is on the top indicates to stop. Fig.1 shows structure of a chowk consisting of four main roads and each road is divided into two main ways (north-south and east-west). We are using two traffic signals A,B. The signals on East-West road is A where B is a traffic signal on North-South road. Both traffic signals have three lights. It is the basic road structure which includes only two ways to travel north-south and east-west so has two signal lights which are considered with signals of array of 3 digits for representation of red, yellow and green respectively. The road structure has also shown 'zebra crossings' for pedestrians so system has provided 2 seconds time period in which both the signals will be off to allow pedestrians to use roads.

### State machine and state table:

The state diagram shown in Fig.2 illustrates that there is counter timer which is counting time up to certain limit and after that the signal will be turned to next state. As an initial condition state S<sub>0</sub>, Light A[2:0] will be on so green light in East-West direction will be ON for 7 seconds and red signal light in other direction namely North-south will be ON. The important part needs to be noticed here is that when time counter count for one second it will simultaneously send the counted value to display value variable which will be displayed on 7-segment display, hence after counting of 7 seconds on display counter timer signals will shift to next state S<sub>1</sub>, in which Light A turns to be Yellow, to warn users to be prepared to stop. After that the counter will display only 2 seconds of time delay and signals will be turned in to

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next state 'S2' which has both Lights A[2:0] and Lights B[2:0] in STOP situation. Further the system goes to next state 'S3' which has Light B in green colour to allow north-south traffic to use road. Similarly, flow will be continued with displaying counted time on 7-segment display and signals will switch to next states S4,S5 respectively.

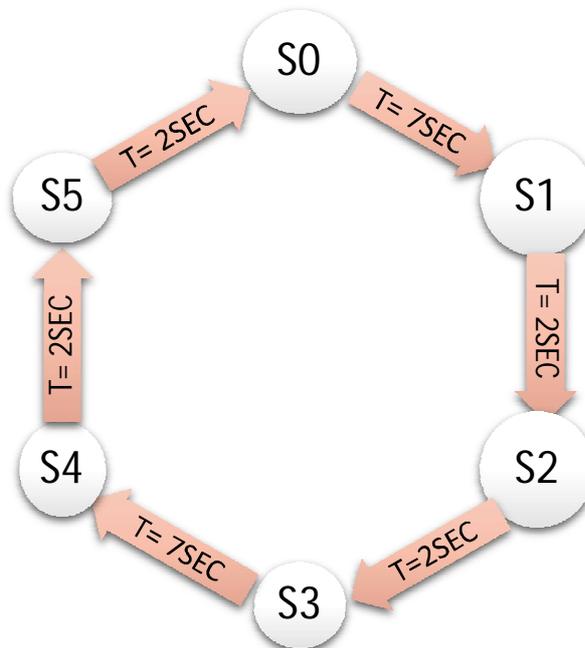


Fig2. State Diagram

The timing states of traffic lights are shown in Table1. The timing of signal lights can be increased or decreased according requirement of time delays. Initially before resetting, Light A traffic signal will be ON. After resetting, the system will again start from the state S0. Also, timer display will again start from initial value.

STATE	West-East	North-South	Delay (in seconds)
Initial S0	GREEN (001)	RED	7
S1	YELLOW (010)	RED	2
S2	RED (100)	RED	2(for pedestrians)
S3	RED	GREEN	7
S4	RED	YELLOW	2
S5	RED	RED	2(for pedestrians)

Table 1: State Table.

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## Logic Synthesis:

The expected functionality of this project system includes the traffic lights should change after every fixed interval of time and count down time should be displayed on 7 Segment Display. As per consideration in the road structure image, we are going consider two signal each one having 3 lights such as GREEN, YELLOW, RED. And one 7digits array element to which count down time is passed.

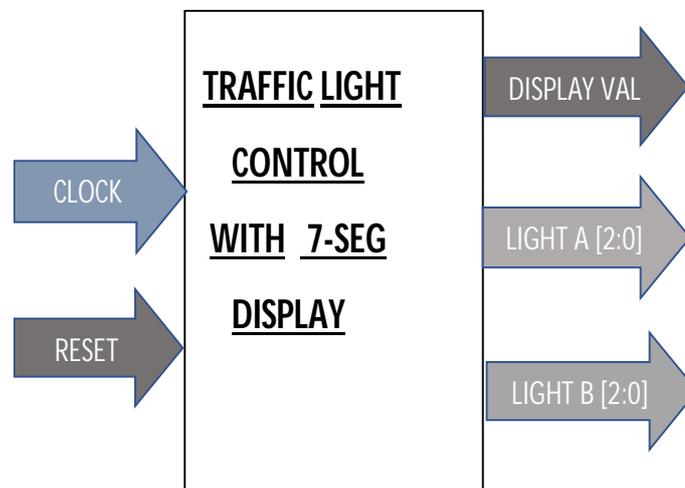


Fig.3. Block diagram of system

We programmed the logic in Verilog by considering two lights for signals as A [2:0], B [2:0] with RYG coding displaying in simulation as if GREEN is ON it should have value 001 and if RED is ON light variable should have value 100. Similarly, For YELLOW is ON it should have value 010 as shown in Table1.

We have written code with a module of traffic light which has 3 variables for system and one counting variable. There are two parts in logic building one-part swipes from one state to next state by checking count value on the basis of clock. Another part includes assigning the values to lights A, B as output for any particular state. Further at the end we came up with task which converts 4 digits count value into 7 digits value to send to 7-seg display unit as output. This experiment is successfully simulated on Questa sim and Xilinx which can be verified from the results which are shown further.

## V. EXPERIMENTAL RESULTS

The design is simulated with Xilinx ISE Simulator and Questa sim to verify that the design behaves as expected in real both in terms of functionality and timing. Fig 4 shows the timing waveform of the design.

Here we can observe in the fig.4 waveform output which clearly show clk,rst,display\_val, light\_A, light\_B variables and also, we can observe the initial conditions for Lights A and B. Further successful implementation can be conformed with RTL schematic and Technology schematic.

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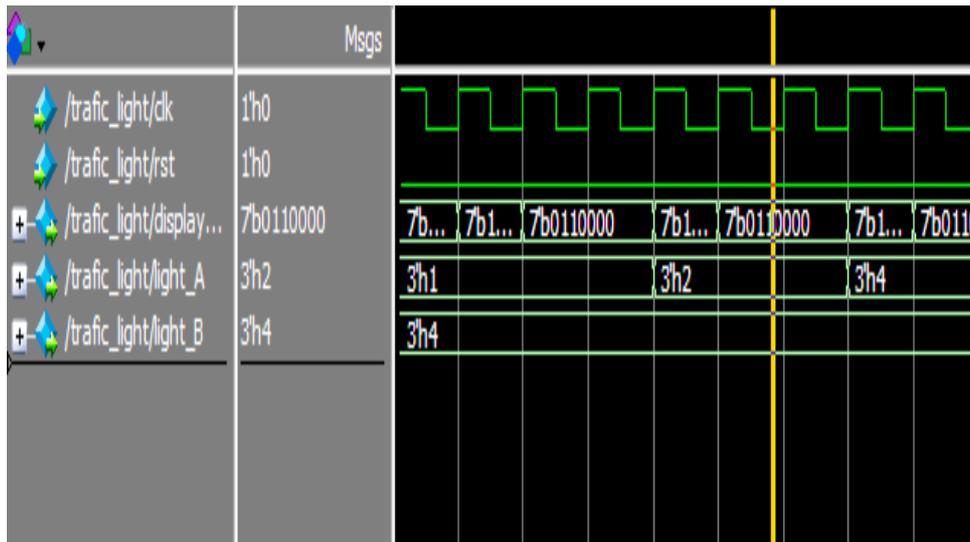


Fig.4.Waveform output.

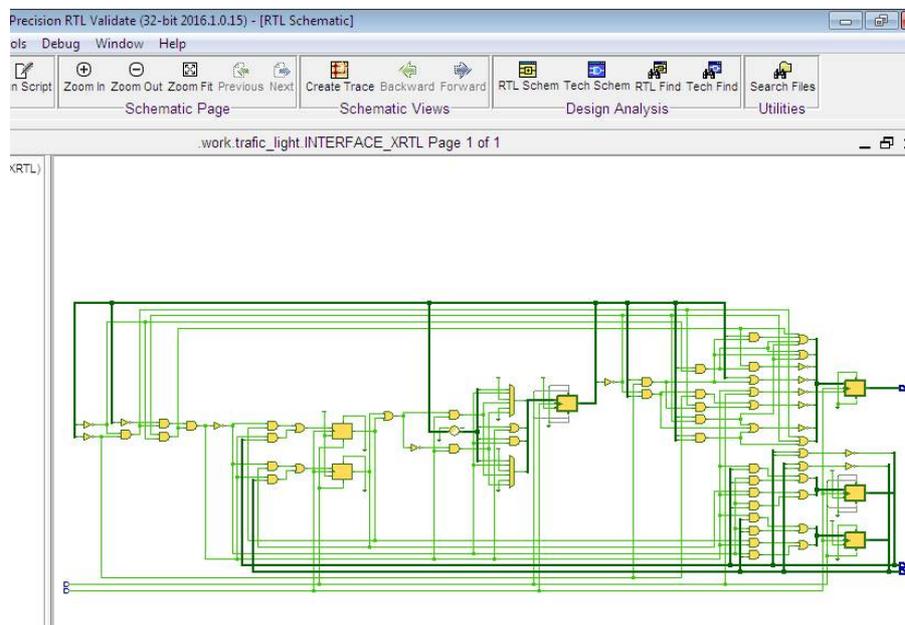


Fig.5.RTLschematic

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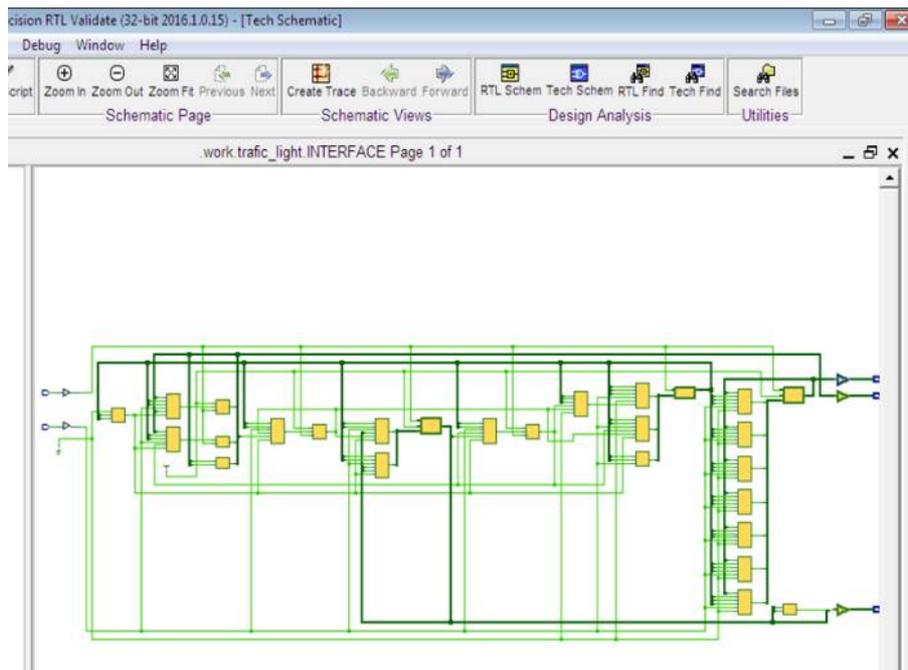


Fig.6.Technology schematic

## VI. CONCLUSION

In this paper we have presented a traffic light controller and countdown display system with an efficient and smart design with the help of finite state machines in Verilog. The simulation of design confirms the efficiency and functionality of the system. The further ways of traffic light controller can improve the traffic condition in very tremendous way. Any advancement in signal controllers can contribute to the miraculous improvement in the traffic condition and also in the protection from road accidents. This implementation of traffic light controller can be used as very system to people as it also shows time. The future scope of this project is it can be further improved for large road junctions and could be directly applied in real time with help of a greater number of such circuits. There is need of such smart systems in today's smart days.

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