

Design of High Gain Bandwidth CMOS Operational Amplifier

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ABSTRACT: Integrated fully differential two stage operational amplifier with two symmetric feedback paths for very High Gain Bandwidth of 4GHz is designed. Such fully differential opamps are well suited for driving differential input ADCs as well as differential transmission lines. They provide immunity to external noise. Improvement in dynamic range is a clear advantage. Antialiasing filtering (baseband signal processing) is made easy by fully differential opamps. In case of differential transmission lines, active termination by such opamps raise efficiency. Differential (Balanced) amplifiers are one way of implementing differential signaling, which has been a common design approach in audio, data-transmission, and telephone systems for years because of its inherent resistance to external-noise sources. This fully differential opamp is designed for Gain-Bandwidth of 4GHZ, phase margin of 65 degrees, dc gain 37dB, I_{dc} 500uA, 90dB CMRR.

KEYWORDS: Anti-aliasing filtering; dynamic range; fully differential; Gain-Bandwidth; Introduction; symmetric feedback;

I. INTRODUCTION

Fully differential opamp also known as balanced in balanced out opamp [1] finds its major application in ADCs for signal conditioning at differential inputs of ADC as anti-aliasing filter. It fundamentally acts as low pass filter for this application. An active, lowpass filter by adding capacitors in the feedback paths is created. Miller compensation is used to easily tune between the Gain Bandwidth and phase margin. In a fully differential amplifier, two feedback paths, one for each side, are possible in the main differential amplifier. This arrangement naturally forms two inverting amplifiers, and you can easily adapt inverting topologies to fully differential amplifiers. High gain enables this circuit to operate efficiently in a closed loop feedback system, whereas high bandwidth makes it suitable for high speed applications. The design is also able to address any fluctuation in supply or dc input voltages and stabilizes the operation by nullifying the effects due to alteration in functioning. This opamp is used in high speed, negative feedback applications as well. Common mode feedback given stabilizes the common mode output voltages allowing differential gain to be decided by the differential signal alone. This opamp uses resistive common mode feedback. Highgain differential opamps demand for common mode feedback [2].

II. BLOCK DIAGRAM OF TWO STAGE OPAMP

Circuit Description

Fully differential two stage op-amp architecture is used. Common source stage is cascaded to both the outputs of first stage differential amplifier. First stage uses N-type input differential amplifier which provides noise immunity to both to differential input and differential output signals. Opampuses Miller compensation technique to move poles of opamp apart from each other to raise the phase margin.

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Operation of Circuit

TABLE I. VOLTAGE DEFINITIONS

Parameter	Definition
I/P differential voltage	$V_{ID} = (V_{in+} - V_{in-})$
O/P Differential voltage	$V_{OD} = (V_{out+} - V_{out-})$
I/P common mode voltage	$V_{IC} = (V_{in+} + V_{in-})/2$
O/P common mode voltage	$V_{oc} = (V_{out+} + V_{out-})/2$

The signal is mainly amplified by NMOS transistors, which have considerable charge carrier mobility. Stage one has the two NMOS differential pair transistors NM0 and NM2, the respective current source load transistors as PM2 and PM0. NM1 transistor is the tail current source as in Fig.1. The Current source load transistors are gate controlled by a CMFB resistors R1 & R2. These resistors sense the common mode output voltages at the respective drain terminals of NM0 and NM2 input transistors and generate CM output voltage [2]. It is fed to the input of the gates of PM2 & PM0. Second stage uses two common source stages as PM4, NM7 & PM1, NM5 for differential outputs of first stage in cascade fashion. C1 & C2 are used for frequency compensation & the resistors R4 & R5 are in series with these C1 and C2 respectively. R4 and R5 compensate for the right hand plane zeros generated by C1 and C2. C1 and C2 along with R4 and R5 boost the Gain-Bandwidth and phase margin [2]. The current sources NM5 and NM7 of the second stage sink currents as in Fig.1.

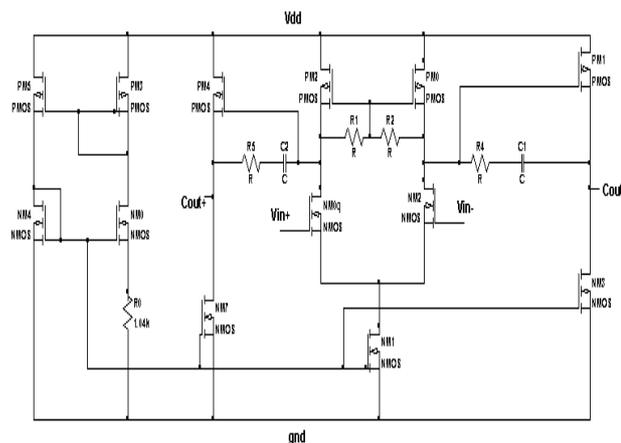


Fig 1. Proposed circuit diagram

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III. MODELLING

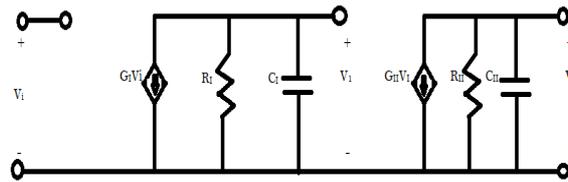


Fig. 2: Small signal analysis without frequency compensation

Transfer function is given by,

$$G = \frac{V_o}{V_i} = \frac{G_{I1}}{sC_{I1}R_{I1}+1} * \frac{G_{II}R_{II}}{sC_{II}R_{II}+1};(1)$$

Where, G_{I1} , G_{II} are trans-conductance of first and second stage respectively.

Pole frequencies are given by [6],

$$p1 = \frac{-1}{2\pi C_{I1}R_{I1}}; \quad (2)$$

$$p2 = \frac{-1}{2\pi C_{II}R_{II}};(3)$$

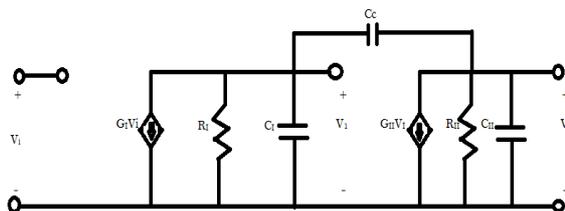


Fig. 3: Small signal analysis with frequency compensation

$$p1_{comp} = \frac{-1}{2\pi(G_{II}R_{II}C_c)}; \quad (5)$$

$$p2_{comp} = \frac{-G_{II}}{2\pi C_{II}};(6)$$

Gain Bandwidth is given by [6],

$$GBW = \frac{G_{I1}R_{I1}G_{II}R_{II}P2_{comp}}{2\pi C_c};(7)$$

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Gain Bandwidth can be varied by varying C_c but C_c has got limitation on its varying range as it affects phase margin achieved as well. If resistor R_z is used in series with C_c , a right hand plane zero is turned into left hand plane zero by taking R_z as [1],

$$R_z > \frac{1}{g_{m1}} \quad (8)$$

This condition compensates for more dominant pole. This improves phase margin considerably. Designer can pick up between phase margin and GBW. Phase margin and GBW tradeoff between their performances.

IV. EXPERIMENTAL RESULTS

Opamp is implemented in Cadence Virtuoso analog design environment (ADE) in 45nmprocess in GPDK. DC analysis assures saturation operating conditions of all the MOSFET devices. AC analysis results obtained meet Gain-Bandwidth of 4.23GHz and phase margin of 58.18°.

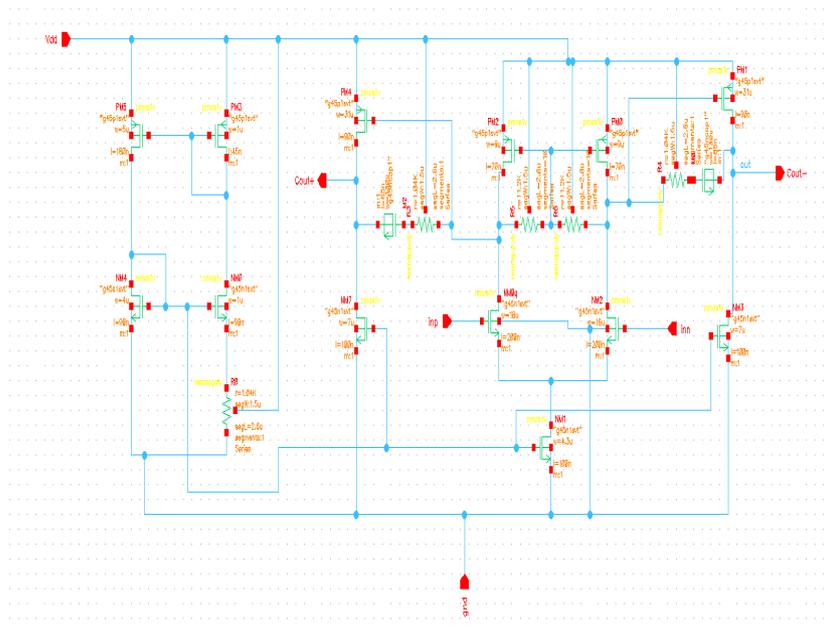


Fig. 4 Circuit diagram

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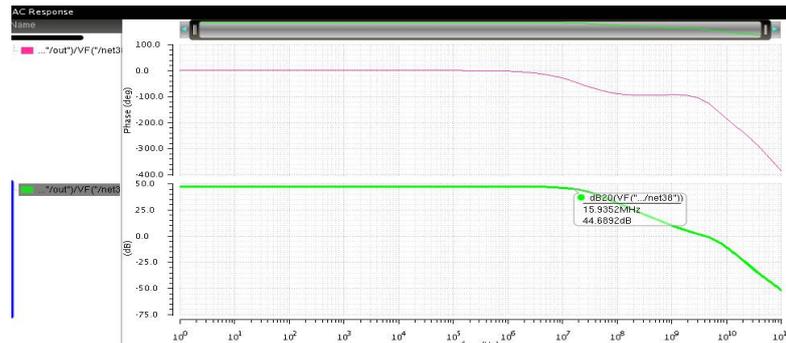


Fig. 5 First pole

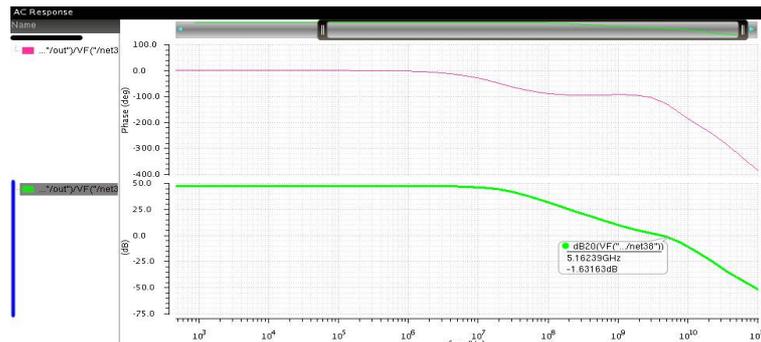


Fig. 6 Second pole

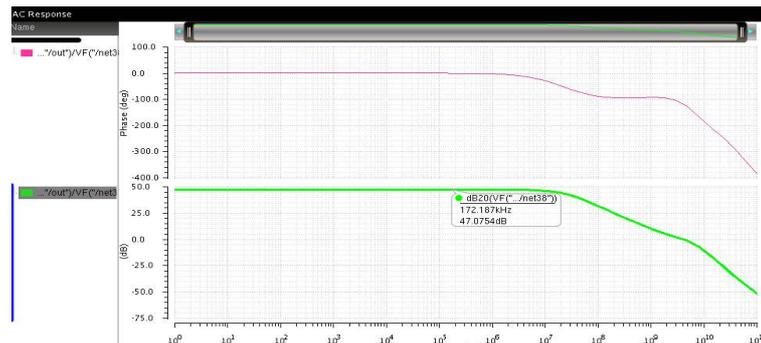


Fig. 7 DC gain

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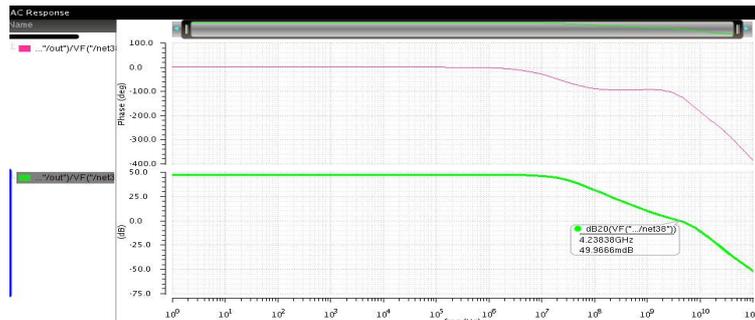


Fig. 8 Gain bandwidth

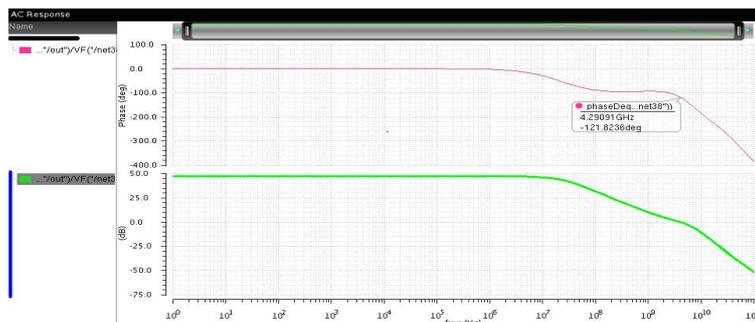


Fig. 9 Phase margin

First pole is moved to 15.9MHz and second pole is moved to 5.16 GHz which yields for high phase margin. DC voltage gain is 47 dB. Unity Gain-Bandwidth attained is 4.23GHz. Corner case analysis is also carried out for different corners like typical-typical, slow-slow, fast-fast by degrading supply voltage to 1V and changing operating temperature between -40° to 125 for all these corners.

TABLE I. CIRCUIT PARAMETERS

Parameter	Value	Comment
Vin	1.1 V	Supply
Unity Gain-Bandwidth	4.23GHz	-
Idc	715uA	DC current
Phase Margin	58.18°	-
C _L	100fF	Off chip load capacitor
First pole	15.9 MHz	-
DC gain	47dB	Open loop gain
Second pole	5.16 GHz	-

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V. CONCLUSION

All transistors are ensured to be in saturation (region 2). This is carried out with DC analysis. Frequency compensation carried out makes one pole dominant and improves phase margin by separating two poles. Unity gain bandwidth obtained is 4.23 GHz. Phase margin is 58.18°. DC gain achieved is 47dB. C1 and C2 compensating capacitors along with R4 and R5 play key role in phase margin and gain bandwidth achievement. P1 compensated becomes dominant pole as it is very close to origin compared to P1 uncompensated. This opamp is implemented in 45 nm process. Comparison with lower nodes shows that as we scale down in nm regime, more unity GBW can be achieved. Simultaneously, trade off between power consumed and GBW to be achieved should be carefully worked out.

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