

International Journal of Innovative Research in Science, Engineering and Technology

(A High Impact Factor, Monthly, Peer Reviewed Journal)

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Vol. 7, Issue 3, March 2018

Design and FPGA implementation of Novel Two's Complement Array Multiplier Circuits and their Comparison with Booth's Array and Modified Bough Wooley Array Multiplier

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ABSTRACT:Two's complement multiplication is used for several Digital applications. This paper proposes two novel two's complement array multiplier circuits with MSB(Most Significant Bit) identification technique. An unique control circuit is designed which can identify whether the given input is signed or unsigned. A comparison with the array structures of Recorded Booth and Modified Bough Wooley Multiplier is discussed in detail, proving the new array is faster than recorded Booth's and Modified Bough Wooley Multiplier. The results also show that the new array uses less hardware than Booth array. The simulated results and the RTL schematic are generated using VHDL. The results are mapped and checked using Xilinx XC3S250E – PQ208 Spartan 3E FPGA.

KEYWORDS:Booth's algorithm, Modified Bough Wooley algorithm,MSB based two's complement ,VHDL.

I. INTRODUCTION

Multimedia applications like Digital Signal Processing , 3D graphics and SoC processors require parallel multipliers for high speed execution. Hence much work is done on Algorithms and Design for Multiplication[2], [4], [5],[7],[8]. Multipliers require three important steps. a) generation of partial products b) reduction of partial products c) Sum and Carry Propagation. Several designs involve Modified Booth's Recorder for the first step since it can reduce the partial products to 50% [5], [7], [14],[15],. Some schemes select Wallace trees or Compressor trees for partial product reduction.[7],[14],[15].For carry and propagation, Advanced Adder approaches like Carry Look Ahead and Carry Select Adders are employed to reduce the propagation delay of carry[6], [12]. The main goal of recent papers is to optimize the path for partial product reduction [5],[8],.A conversion signal based algorithm where all the bits in right most "1" are complemented but the other digits are not disturbed is also discussed. Analysis and design of an approximate 4:2 compressor for utilization in a multiplier is also suggested in [1].A new algorithm based on synchronous computation of the partial sums of the two operands is also analysed . In this context a new algorithm is described. It's novel advantage is that it uses a new MSB identification technique for two's complement based array multiplier.Part one of this work consists of a short description about two's complement. Part two describes the new algorithm. Part three discusses about the comparison of the MSB technique with Booth's array and Modified Bough Wooley algorithm.

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II. THE CONVENTIONAL TWO'S COMPLEMENT

The main advantage of the two's complement are (1) The representation of zero is unique i.e there is no separate representation for negative zero.(2) No special treatment is required for sign of the number (3) Another important fact is that the carry coming out of the last addition can be ignored without affecting the correctness of the result.

Let $A = a_{n-1}a_{n-2}a_{n-3} \dots a_2a_1a_0$ be a two's complement number where a_{n-1} signifies the Most Significant Bit (MSB) as a signed bit. It can be evaluated as

$$A = -2^{N-1}a^{N-1} + \sum_{i=0}^{N-2} a^i$$

Consider two Binary digits in Two's Complement

$$X = -x_{m-1}2^{m-1} + \sum_{i=0}^{m-2} x_{i2^i}$$

$$Y = -y_{n-1}2^{n-1} + \sum_{j=0}^{n-2} y_{j2^j}$$

The product of X and Y can be shown as

$$P = \left(-x_{m-1}2^{m-1} + \sum_{i=0}^{m-2} x_{i2^i} \right) \left(-y_{n-1}2^{n-1} + \sum_{j=0}^{n-2} y_{j2^j} \right)$$

$$= \sum_{i=0}^{m-2} \sum_{j=0}^{n-2} x_i y_j 2^{i+j} + x_{m-1} y_{n-1} 2^{m+n-2} -$$

$$\left(\sum_{i=0}^{m-2} x_i y_{n-1} 2^{i+n-1} + \sum_{j=0}^{n-2} x_{m-1} y_j 2^{j+m-1} \right)$$

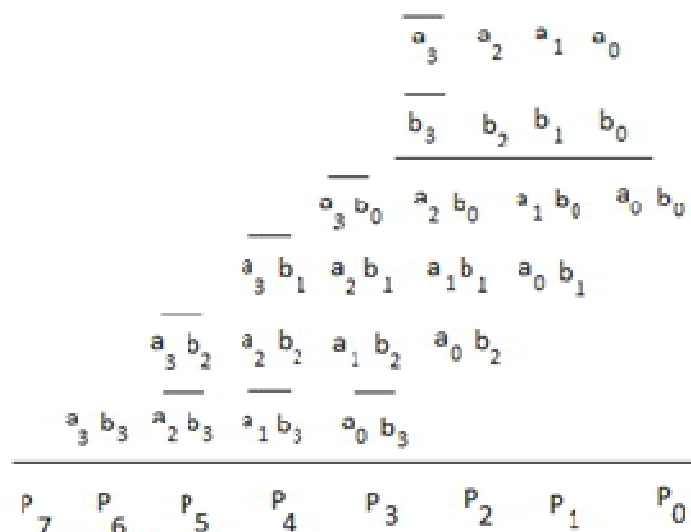


Fig 1:Conventional 4x4 two's complement array multiplier

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III. THE PROPOSED CIRCUIT I WITH MSB IDENTIFICATION TECHNIQUE

A new circuit has been proposed to perform two's complement array multiplication using Most Significant Bit (MSB) recognition technique. The circuit works as follows if the MSB of the multiplier is '1'

- Each bit of the multiplicand is inverted using XOR gate.
- The MUX circuit selects the output of the XOR gate using MSB of the multiplier as control signal
- The full adder performs the 2's complement operation by assigning MSB of the multiplier to Cin.

If the MSB of the multiplier is zero, then each bit of the multiplicand is converted to zero using AND gate. The MUX circuit now selects the output of the AND gate and the full adder adds these values with the partial products. In this case the circuit assigns zero to Cin.

The MSB identification circuit is given

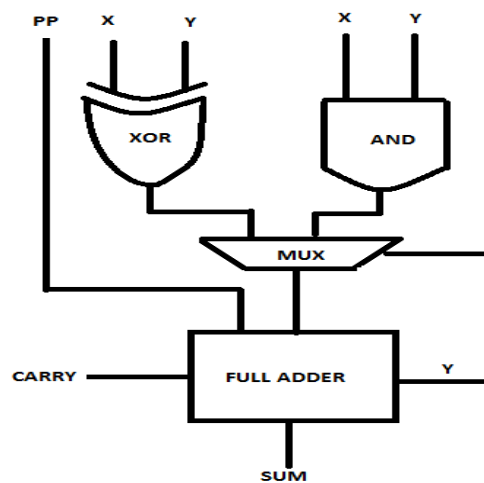


Fig 2:Control Logic I

IV. THE PROPOSED CIRCUIT II WITH NOT GATE

A NOT gate based circuit has been designed with a simple implementation technique as follows.

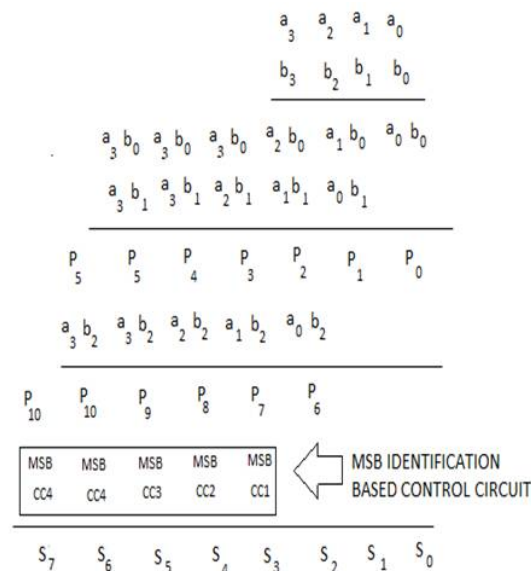
- If the MSB of the multiplier is '1' then each value of the multiplicand is inverted using a NOT gate.
- The MUX circuit selects the output of the NOT gate using MSB of the multiplier as control signal.
- The full adder performs the 2's complement operation by fixing Cin as '1'.

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If in this case the MSB of the multiplier is zero, then the MSB value is assigned to each bit of the multiplicand . This action converts the multiplier bits to Zero and the full adder adds each value with the partial products.

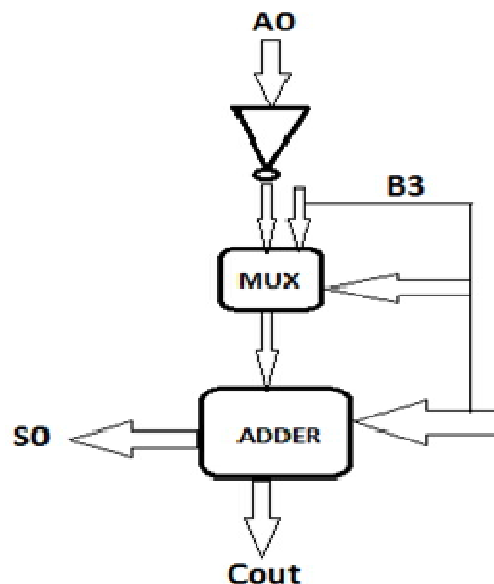


Fig 3:Control Logic II

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V. 4X4 BOOTH ARRAY MULTIPLIER

An array multiplier for the Booth algorithm is simply to mimic the operation of the multiple-cycle structure. In each step of the Booth algorithm, two bits (from LSB to MSB) of the multiplier are examined and taken an appropriate operation accordingly. Then, the partial product is shifted right by one bit position, which corresponds to shifting the multiplicand one bit left. Based on these observations, a 4 X 4 booth array multiplier can be derived. It requires 4 X 4 complementer and subtractor (CAS) units and 4 controllers (CTRLs). The function and logic circuit of CAS are given in the figure. The CTRL controls the operation of CAS and has the logic circuit shown in the figure

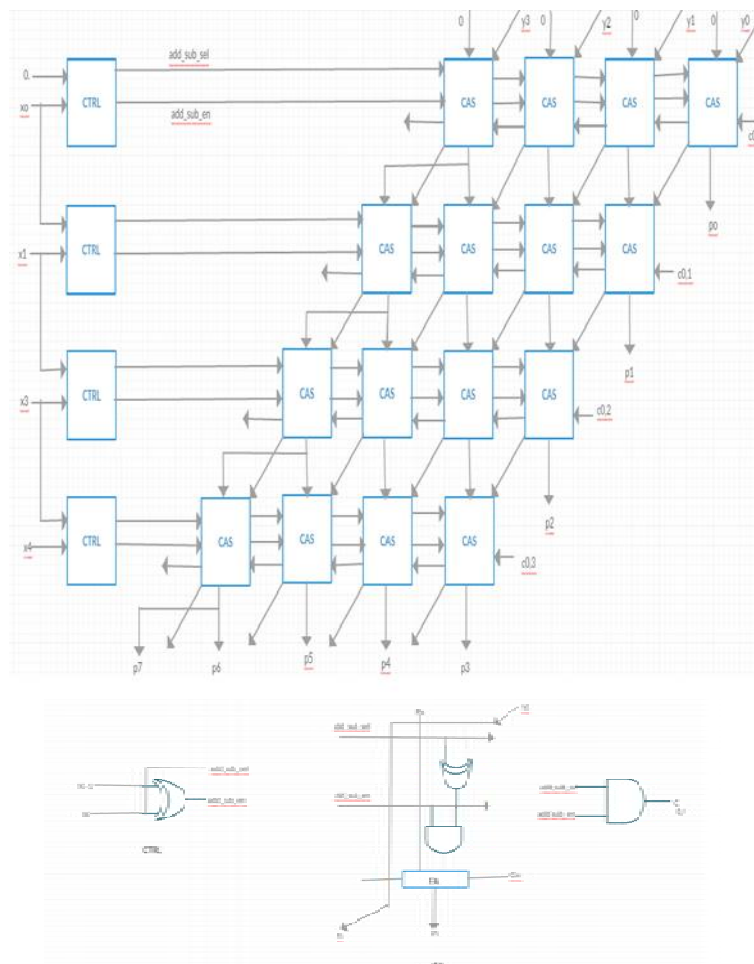


Fig 4: Booth Array Multiplier

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VI. 4X4 MODIFIED BAUGH WOOLEY ARRAY MULTIPLIER

In signed multiplication the length of the partial products and the number of partial products will be very high. So an algorithm was introduced for signed multiplication called as BaughWooley algorithm. The Baugh-Wooley multiplication is one amongst the cost-effective ways to handle the sign bits. This method has been developed so as to style regular multipliers, suited to 2's complement numbers. Baugh-Wooley Multiplier provides a high speed, signed multiplication algorithm. It uses parallel products to complement multiplication and adjusts the partial products to maximize the regularity of multiplication array. When number is represented in two's complement form, sign of the number is embedded in Baugh-Wooley multiplier. This algorithm has the advantage that the sign of the partial product bits are always kept positive so that array addition techniques can be directly employed. In the two's complement multiplication, each partial product bit is the AND of a multiplier bit and a multiplicand bit, and the sign of the partial product bits are positive.

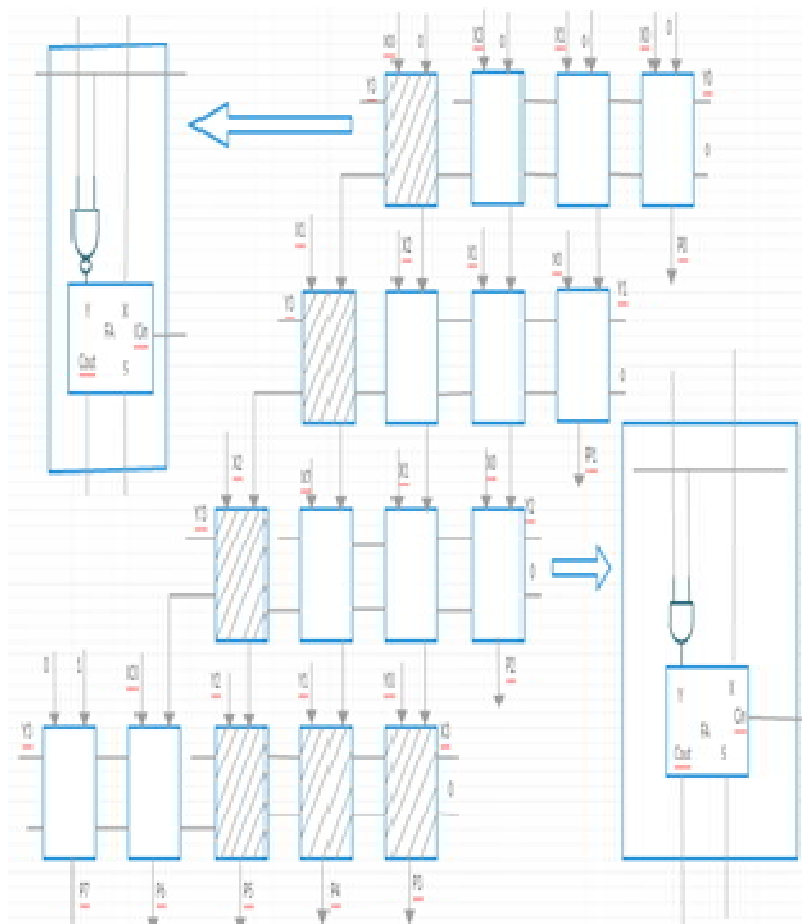


Fig 5: Modified Baugh Wooley Array Multiplier

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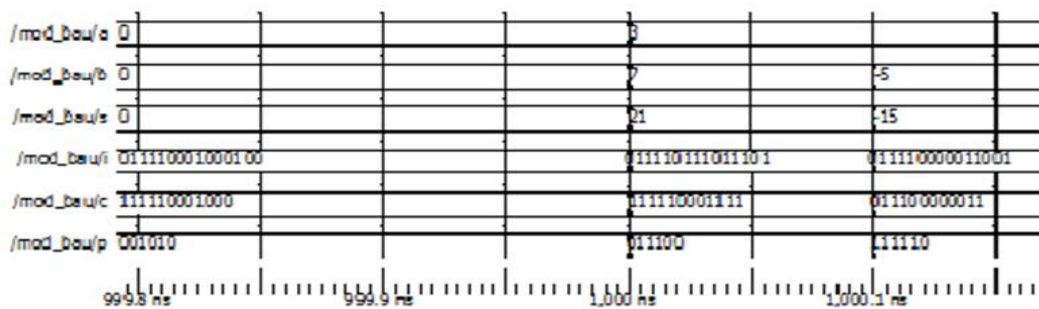
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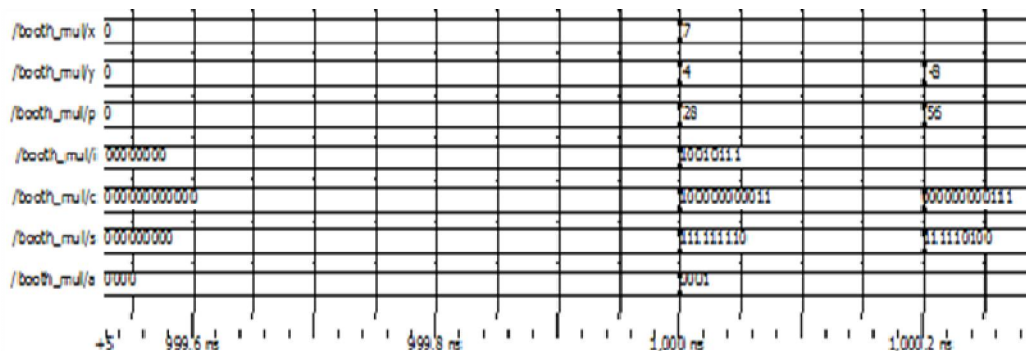
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VII.SIMULATION RESULTS

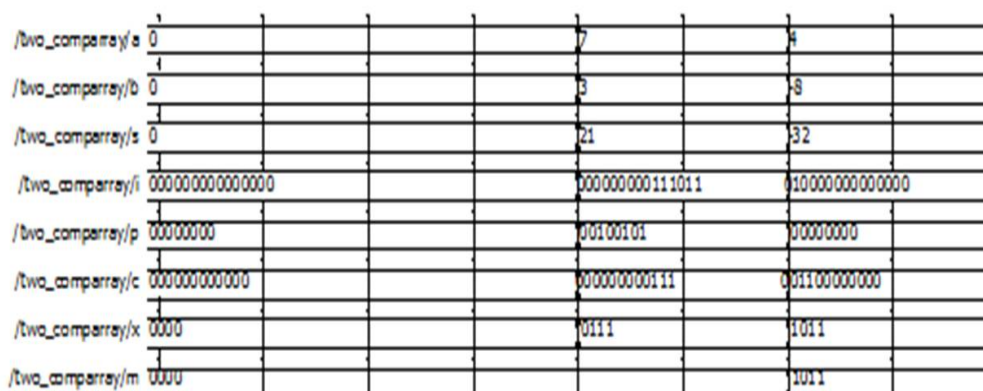
Modified Baugh Wooley Multiplier



Booth's Array Multiplier



Proposed Circuit I



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Proposed Circuit II



VI.COMPARISON OF DEVICE UTILIZATION SUMMARY

The proposed multipliers are compared with Booth's array and Modified Bough Wooley array array multipliers. From the table given below it is well known that the proposed circuit I provides better device utilization and less combinational path delay compared to Booth's array and Modified Baugh Wooley array multipliers.

The design has been coded using Very High Speed Integrated Circuit(VHDL), synthesized using Xilinx 13.2 ISE and mapped onto Xilinx XC3S250E – PQ208 Spartan 3E FPGA. It is clear from the given table that the proposed technique uses

Logic Utilization	Proposed Circuit I	Proposed Circuit II	Booth's Array	Modified Bough Wooley
No of Slices	2	17	21	2
No of 4 input LUT's	3	29	31	4
No of Bonded IOB's	8	16	17	12
Maximum combinational path delay	6.376ns	15.325ns	16.80ns	6.403ns

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