

Comparative Analysis of Three-Leg Single DC Link Capacitor Based DSTATCOM with Split Capacitor Based DSTATCOM

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ABSTRACT: This paper proposes a comparative analysis between a three leg split capacitor based DSTATCOM and a three leg single dc link capacitor based DSTATCOM. In both the topologies the DSTATCOM is coupled to the line by means of an interfacing inductor which acts as a filter. The major drawback associated with the split capacitor based DSTATCOM is the voltage unbalancing issue across the split capacitors at the front end of DSTATCOM. To overcome the above mentioned voltage unbalancing issue another topology is introduced named as single dc link capacitor based DSTATCOM. In this topology the split capacitors are converted into a single dc link capacitor, so that the voltage unbalancing issue associated with the split capacitor based DSTATCOM is avoided. Simulation studies for both the topologies are carried out and its results are presented.

KEYWORDS: Distribution Static Compensator (DSTATCOM), Voltage Source Inverter (VSI), Instantaneous Symmetrical Component Theory (ISCT), Hysteresis Band Current Controller (HBCC), Proportional Integral (PI) Controller.

I. INTRODUCTION

Most of our load systems are unbalanced and non-linear one. Due to the usage of these loads, excessive neutral current starts to flow through the neutral conductor. This will overload the neutral conductor and also distorts the source currents which causes the system to get heated and also reduces the life time of the system. It will cause other serious impacts on the distribution systems. In order to avoid such power quality issues, a compensating device is used named as DSTATCOM. DSTATCOM is nothing but an inverter which injects reactive power into the line in which the load is connected. This is normally called as reactive power compensation. DSTATCOM is basically a shunt compensator because it is connected parallel to the line by means of an interfacing inductor which acts as a filter. DSTATCOM can perform the operations such as load balancing, harmonic compensation, power factor correction, neutral current compensation. Load balancing means making the distorted source current due to the usage of non-linear loads to be a balanced sinusoidal one. Due to the usage of non-linear loads the source currents gets distorted. As a result of that the difference between the source currents starts to flow as a neutral current through the neutral conductor which will overload the neutral conductor. DSTATCOM must also be able to compensate the neutral current in the system.

There are different types of DSTATCOM topologies. It is mainly classified based on their structure and the type of control algorithms used. A detailed review of different types of DSTATCOM topologies has been reported in [1, 2, and 3]. The two main types of DSTATCOM topologies are transformer or magnetic-based topologies and inverter-based topologies. The compensation using magnetic-based topologies is very simple and effective. The main drawback of this topology is that it makes the system more bulky. So another DSTATCOM topology named as inverter-based topology is used for compensation. There are four main types of inverter-based topologies. They are four leg VSI based DSTATCOM, three single phase VSIs, three leg VSI with split capacitors and three leg VSI with neutral terminal at the positive or negative of DC bus. Four leg VSI based DSTATCOM has four legs. The first three legs are connected to three phase systems. The

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fourth leg is mainly used to compensate the neutral current, so that it is connected to the line neutral. This topology is explained further in [4,5]. The main drawback of this topology is the usage of more number of VSI switches which will result in more switching losses. Three single phase VSI based DSTATCOM topology has three single phase VSIs which is connected back to back. In this topology, each single phase VSI is responsible for the compensation of each single line in the system. Here, the DSTATCOM structure is connected to the line by means of a coupling transformer. The detailed view of this topology is explained in [1,6]. The split capacitor based DSTATCOM topology uses a three leg VSI with the split dc link capacitors at its front end. In order to compensate the neutral current the source neutral and load neutral are connected to the mid-point of the split capacitors. This topology has the advantage of using less number of VSI switches and independent control of VSI legs. This topology is further explained in [7,8]. The split capacitor based DSTATCOM topology has one serious problem associated with it. Since, it is using the split capacitors there is a voltage unbalancing issue across the capacitors which will results in unequal capacitance leakage currents, unequal delays in the switching devices, charging of capacitors is asymmetrical during transients. However when the load current contains a dc component, the voltage unbalance between the capacitors becomes very high. The problems due to the voltage unbalance is discussed in [9,10]. In order to avoid the unbalancing issue some additional circuitry is needed. However it will increase the overall cost of the system. It is further explained in [11,12].

The next DSTATCOM topology is single dc link capacitor based DSTATCOM. The detailed explanation of this topology is given in [13]. In order to avoid the voltage unbalancing issue associated with the split capacitor based DSTATCOM the split capacitor is converted into a single dc link capacitor. At the same time in order to compensate the neutral current an additional small ac capacitor is connected between the negative of the dc bus and the system neutral. The comparison between the split capacitor based DSTATCOM and single dc link capacitor based DSTATCOM is explained below.

Both the topologies uses the same control algorithms. (i) Instantaneous symmetrical component theory (ISCT) [14] to generate the reference currents. (ii) Hysteresis band current controller (HBCC) [15] to generate the pulses for the VSI switches. The steady state and transient performance of both the topologies for three-phase four-wire distribution system is explained through simulation studies.

II. STRUCTURAL COMPARISON BETWEEN THREE LEG SPLIT CAPACITOR BASED DSTATCOM AND SINGLE DC LINK CAPACITOR BASED DSTATOM

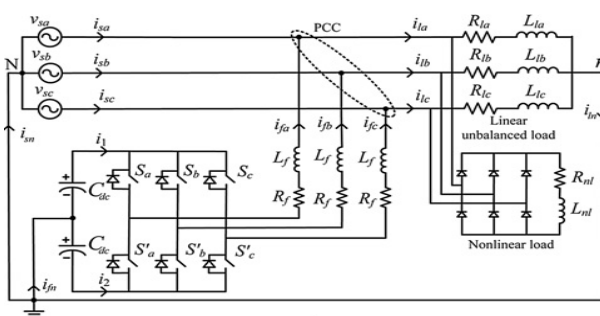


Fig. 1: Three leg split capacitor based DSTATCOM

Fig 1 represents the three leg split capacitor based DSTATCOM. In this topology, the split capacitor model is used before the DSTATCOM and to compensate the neutral current, both the source neutral and load neutral are connected to the middle of the two capacitors.

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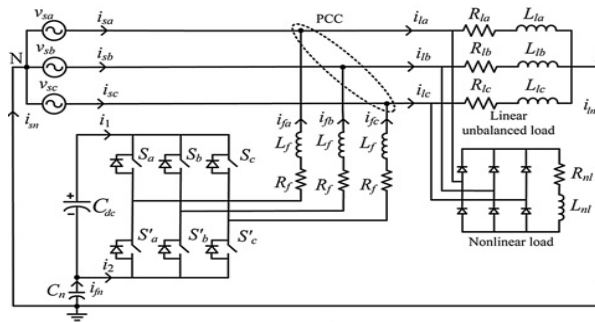


Fig. 2: Three leg single dc link capacitor based DSTATCOM

Fig 2 represents the three leg single dc link capacitor based DSTATCOM. In this topology instead of using split capacitors before the DSTATCOM, a single dc link capacitor is used. At the same time to compensate the neutral current, a small ac capacitor is connected between the negative of the dc bus and the system neutral. This is the structural difference between the two topologies.

III. DESIGN OF TWO DSTATCOM TOPOLOGIES

A. Design of split capacitor based DSTATCOM

The parameters to be considered while designing are, (i) DC link voltage (V_{dc}) (ii) DC storage capacitor (C_{dc}) (iii) Interfacing inductance (L_f) (iv) Switching frequency (F_{sw})

A.1 DC link capacitor value (C_{dc})

It is given by,

$$C_{dc} = \frac{(2X - \frac{X}{2})nT}{(1.8Vm)^2 - (1.4Vm)^2} \quad (1)$$

where, X is the DSTATCOM KVA rating, V_m is the peak value of source voltage, T is the time period of each cycle, n is the number of cycles.

A.2 Interfacing inductance (L_f)

It is given by,

$$L_f = \frac{1.6Vm}{4hF_{swmax}} \quad (2)$$

Where, $h = \frac{k_1(2m^2 - 1)}{k_2 4m^2} F_{swmax}$ (3)

K_1, K_2 is the proportionality constants. F_{swmax} is the maximum switching frequency. F_{swmin} is the minimum switching frequency.

m is given by,

$$m = \frac{1}{\sqrt{1 - \left(\frac{F_{swmin}}{F_{swmax}}\right)}} \quad (4)$$

A.3 DC link voltage (V_{dc})

The voltage reference (V_{dcref}) of DC link capacitor has been taken as $1.6V_m$ for each capacitor.

B. Design of single dc link capacitor based DSTATCOM

The parameters to be considered are, (i) Neutral capacitor (C_n) (ii) DC link voltage (V_{dc}) (iii) DC link capacitor (C_{dc}) (iv) Interfacing inductance (L_f)

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B.1 Neutral Capacitor (C_n)

In order to find out C_n , we need to equate the phase 'a' filter current and phase 'a' load current. This is done, because the filter sends the compensating current into the line to balance the load (i.e) making the source current as a balanced sinusoidal one.

The load current for 'a' phase is given by,

$$i_{la} = \frac{V_{sa}}{(R_{la} + jX_{la})} \quad (5)$$

The filter current for 'a' phase is given by,

$$i_{fa} = \frac{V_1 - V_{sa}}{R_f + j(X_f - X_{cn})} \quad (6)$$

where, V_{sa} is the phase 'a' source voltage, R_{la} and X_{la} is the phase 'a' load resistance and reactance, R_f and X_{f} is the filter resistance and reactance, V_1 is the fundamental inverter output voltage, X_{cn} is the reactance of neutral capacitor.

By equating the imaginary parts of equations (5) and (6),

$$\frac{(V_{sa}X_{la})}{(R_{la}^2 + X_{la}^2)} = \frac{(V_1 - V_{sa})}{R_f^2 + (X_f - X_{cn})^2} (X_f - X_{cn}) \quad (7)$$

By applying all the known values in equation (7), the value of neutral capacitor (C_n) can be found out.

B.2 DC link voltage (V_{dc})

As discussed in the split capacitor based DSTATCOM topology, we need to maintain a dc link voltage of $1.6V_m$. In this topology, only one dc capacitor is used. So the reference voltage (V_{dcref}) to be maintained across the capacitor is ($2 * 1.6V_m$).

B.3 DC link capacitor (C_{dc})

The functions of DC capacitor in the DSTATCOM are to (i) maintain the dc voltage with minimum ripple during steady state (ii) act as an energy storage element to supply reactive and harmonic power of the load.

It is given by,

$$C_{dc} = \frac{2(2X - \frac{X}{2})nT}{(1.8V_m)^2 - (1.4V_m)^2} \quad (8)$$

B.4 Filter inductance (L_f)

It influences (i) switching frequency (ii) rate of change of filter current.

It is given by,

$$L_f = \frac{1.6V_m}{4hF_{max}} \quad (9)$$

Where, F_{max} is the maximum switching frequency, h is the width of the hysteresis band. A proper hysteresis band ($\pm h$) is to be selected for better tracking performance. Normally, the band width is selected as 5% of the compensator current.

IV. CONTROL ALGORITHM

It is common for both the DSTATCOM topologies. The steps to be followed are,

- (i) Generate the reference filter currents (i_{fabc}^*).
- (ii) Compare the reference filter currents (i_{fabc}^*) with the actual filter currents (i_{fabc}) and generate the pulses for VSI switches.
- (iii) Maintain the dc link voltage (V_{dc}) at a reference value (V_{dcref}) with the help of PI controllers.

Step 1: Generate reference filter currents (i_{fabc}^)*

It is generated by using Instantaneous Symmetrical Component Theory (ISCT). It is given as,

$$i_{fa}^* = i_{la} - \frac{V_{sa} + \beta(V_{sb} - V_{sc})}{\sum_{j=a,b,c} V_{sj}^2} (P_l + P_{loss}) \quad (10)$$

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$$i^*_{fb} = i_{lb} - \frac{V_{sb} + \beta (V_{sc} - V_{sa})}{\sum_{j=a,b,c} V_{sj}^2} (P_l + P_{loss}) \quad (11)$$

$$i^*_{fc} = i_{lc} - \frac{V_{sc} + \beta (V_{sa} - V_{sb})}{\sum_{j=a,b,c} V_{sj}^2} (P_l + P_{loss}) \quad (12)$$

where, (i_{la} , i_{lb} , i_{lc}) represents the three phase load currents, (V_{sa} , V_{sb} , V_{sc}) represents the three phase source voltages, P_l is the average load power, P_{loss} represents the switching and ohmic losses in the actual compensator. $\beta = \frac{\tan \phi}{\sqrt{3}}$. ϕ is the desired phase angle between source voltage and current. In order to obtain unity power factor (UPF), the value of β was chosen as zero.

Average load power (P_l) is given by the equation,

$$P_l = \frac{1}{T} \int_{t_1-T}^{t_1} (V_{sa} i_{la} + V_{sb} i_{lb} + V_{sc} i_{lc}) dt \quad (13)$$

P_{loss} is given by the equation,

$$P_{loss} = K_p e_{vdc} + K_i \int e_{vdc} dt \quad (14)$$

where, $e_{vdc} = V_{dcref} - V_{dc}$. (i.e) the error difference between reference dc link voltage and actual dc link voltage, K_p is the proportional gain, K_i is the integral gain.

Step 2: Generate the pulses for VSI switches

In order to generate the pulses for VSI switches, a Hysteresis Band Current Controller (HBCC) technique is used. The switching control law is given as,

(i) If $i_{fa} \geq i^*_{fa} + h$, then bottom switch is turned ON whereas the top switch is turned OFF. ($U_a = 0, \overline{U}_a = 1$).

\overline{U}_a denotes all the VSI top switches.

U_a denotes all the VSI bottom switches.

(ii) If $i_{fa} \leq i^*_{fa} - h$, then bottom switch is turned OFF whereas the top switch is turned ON. ($U_a = 1, \overline{U}_a = 0$).

The control law given above is only for 'a' phase. The same control technique is used for the remaining two phases also.

The error value between the three phase actual filter currents (i_{fabc}) and the reference filter currents (i^*_{fabc}) is given to the HBCC, where the value of hysteresis bandwidth is set. In the HBCC, all the switching control techniques may take place to generate the pulses for the VSI switches.

Step 3: To maintain the dc link voltage (V_{dc}) at a reference value with the help of PI controller.

The dc link capacitor voltage is maintained constant using PI controller. In order to maintain the average dc voltage across the capacitor to be constant, the average value of dc current through the capacitor to be zero. The expression for dc link voltage (v_{dc}) is given by,

$$V_{dc} = \left(\frac{1}{C_{dc}} \right) \int i_{dc} dt \quad (15)$$

From equation (15) it is clear that V_{dc} is maintained constant only if i_{dc} is zero. i_{dc} represents the average value of dc current through the dc link capacitor. The deviation of V_{dc} from the reference value V_{dcref} at the end of each cycle, gives a result of a small deviation of i_{dc} from zero. So, in order to avoid deviation of V_{dc} , a small Proportional – Integral controller is used. The PI controller is designed based on equation (14).

V. SIMULATION RESULTS

In order to compare the performance of both the DSTATCOM topologies, same type of unbalanced load and non-linear load is used in both the topologies.

V.A Steady state performance comparison of both the DSTATCOM topologies.

In steady state performance, the load does not gets changed throughout the entire simulation time. The three phase source voltage (V_{sabc}) is also remain the same for the two DSTATCOM topologies.

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Table I: System parameters for both DSTATCOM topologies

Parameters	values	
	Split capacitor based DSTATCOM	Single DC link capacitor based DSTATCOM
Grid voltage	400 V L-L (rms), 50 Hz	400 V L-L (rms), 50 Hz
DC capacitor	$C_{dc} = 1150 \mu\text{F}$	$C_{dc} = 3300 \mu\text{F}$
DC-link voltage	$V_{dc} = 520$ (across each capacitor)	$2V_{dc} = 1040$
Neutral capacitor	No Neutral Capacitor is used	$C_n = 10 \text{ mF}$
Interfacing inductor	$L_f = 30 \text{ mH}$	$L_f = 45 \text{ mH}$
Interfacing resistance	$R_f = 0.5 \Omega$	$R_f = 0.5 \Omega$
Hysteresis band	$\pm h = 5\%$ of the compensator current	$\pm h = 5\%$ of the compensator current
Voltage controller PI gains	$K_p = 50, K_i = 0.05$	$K_p = 50, K_i = 0.05$
Linear load	$Z_{1a} = 17.5 + j7.8 \Omega, Z_{1b} = 27.5 + j12.5 \Omega, Z_{1c} = 37.5 + j31.4 \Omega$	$Z_{1a} = 17.5 + j7.8 \Omega, Z_{1b} = 27.5 + j12.5 \Omega, Z_{1c} = 37.5 + j31.4 \Omega$
Non-linear load	3 ϕ diode bridge rectifier	3 ϕ diode bridge rectifier

Table I shows the value of the parameters used in the simulation. Here, in both the topologies, the value of source voltage is same. It is taken as 400 V L-L (rms), 50 Hz. The values of dc link capacitors, dc link voltage, neutral capacitors, interfacing inductance in both the topologies are formed based on the formulas mentioned in section III.

V.A.1 Steady state performance of three leg split capacitor based DSTATCOM

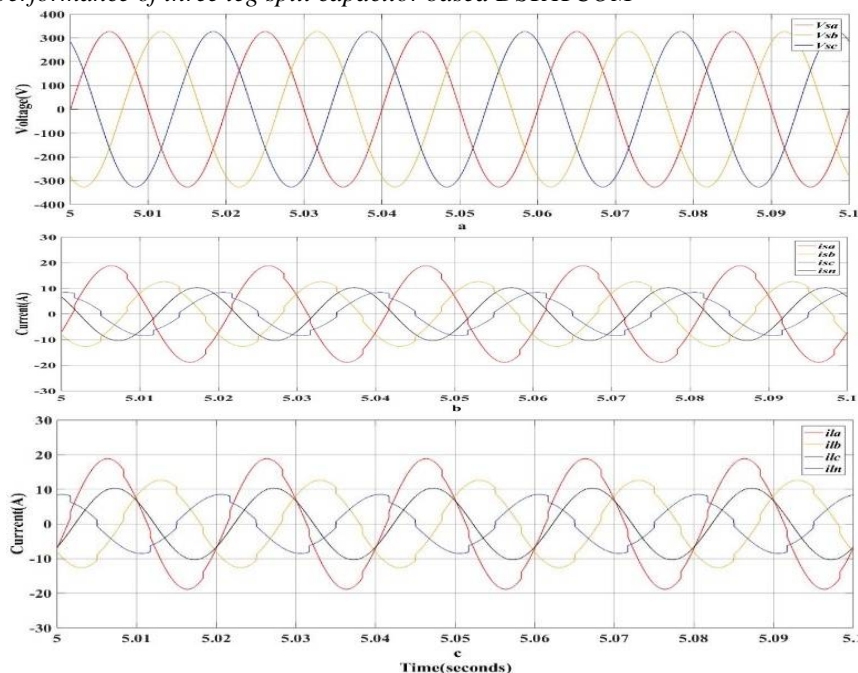


Fig. 3: Steady state performance of split capacitor based DSTATCOM before compensation - a) Source voltages (V_{sabc}), b) source currents (i_{sabc}) and source neutral current (i_{sn}) before compensation, c) load currents (i_{labc}) and load neutral (i_{ln})

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Fig 3(a) shows the three phase source voltages of 400 V L-L (rms), 50 Hz. Fig 3(b) shows the distorted three phase source currents before compensation. This distortion in source currents is due to usage of linear unbalanced load and non-linear load. Due to the unbalance in the source currents there exists a source neutral current. Fig 3(c) shows the distortion in the load currents due to the usage of linear unbalanced load and non-linear load.

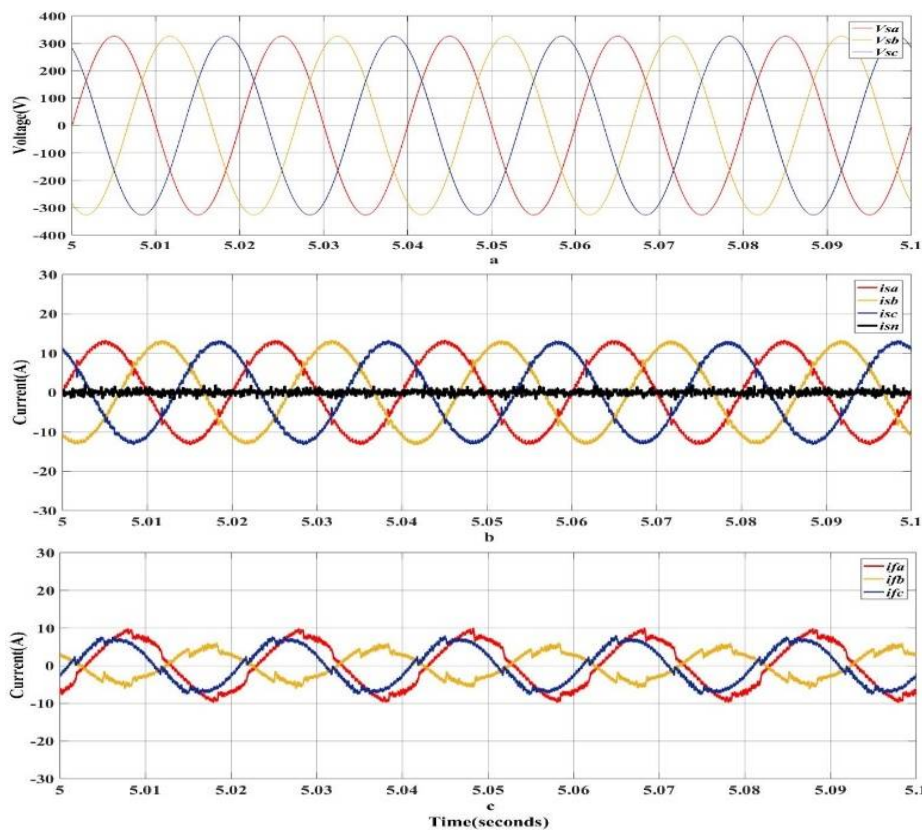
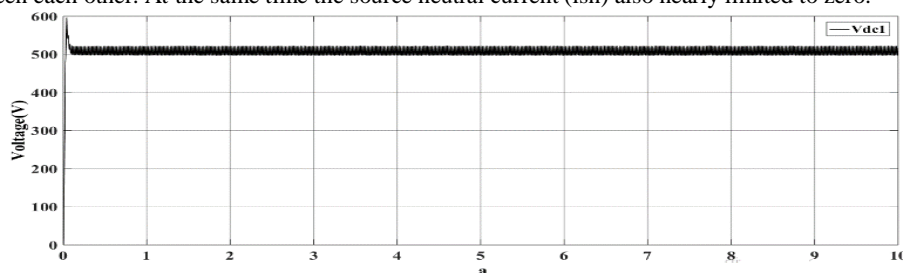


Fig. 4: Steady state performance of split capacitor based DSTATCOM after compensation - a) Source voltages (V_{sabc}), b) source currents (i_{sabc}) and source neutral current (i_{sn}) after compensation, c) filter currents (i_{fabc})

Fig 4(b) shows the three phase source currents (i_{sa} , i_{sb} , i_{sc}) after the compensation provided by the split capacitor based DSTATCOM. In order to bring the source currents as balanced sinusoidal one, the compensator currents or filter currents shown in Fig 4(c) are injected into the line by means of an interfacing inductor. Source currents after compensation has equal magnitude and proper phase displacement between each other. At the same time the source neutral current (i_{sn}) also nearly limited to zero.



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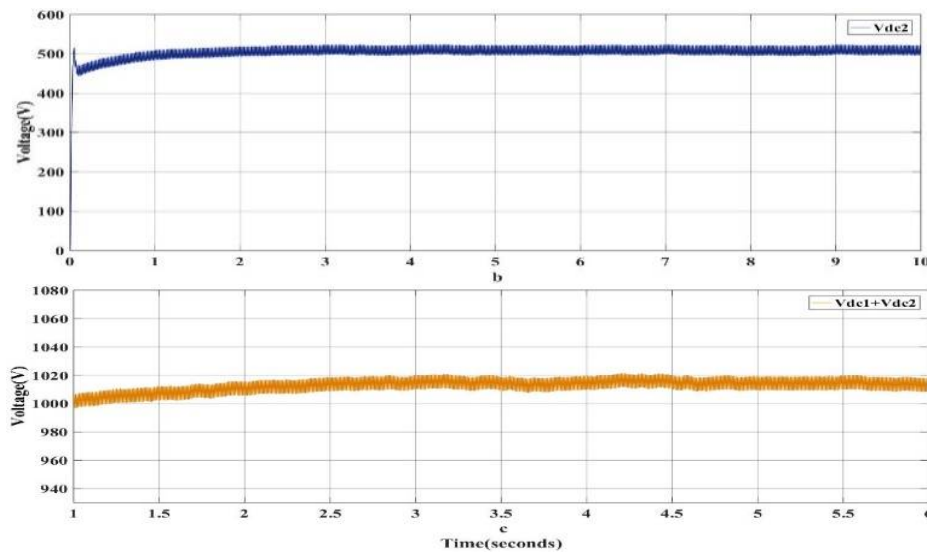
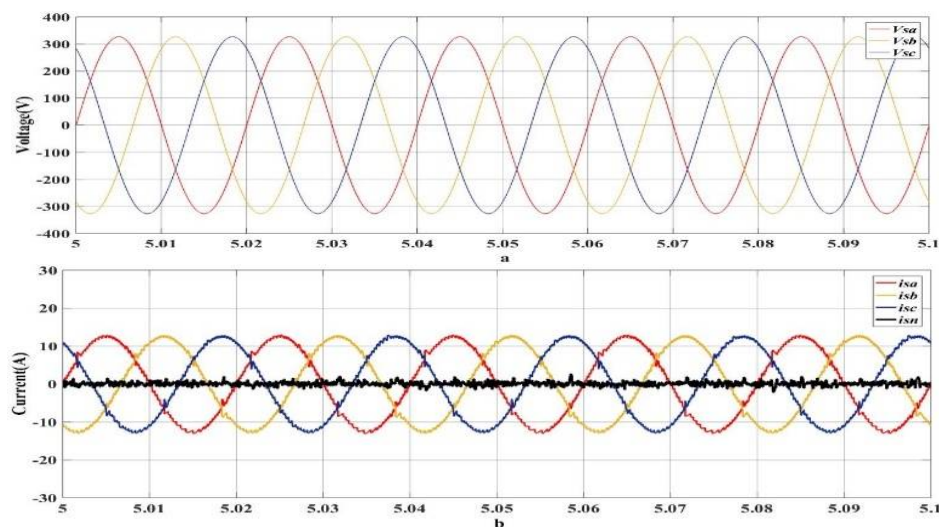


Fig. 5: DC link voltage (V_{dc}) across the dc link capacitors in split capacitor based DSTATCOM - a) Dc link voltage across the first capacitor (V_{dc1}), b) dc link voltage across the second capacitor (V_{dc2}), c) zoomed view of voltage unbalance across the two split capacitors ($V_{dc1} + V_{dc2}$)

With the help of PI controllers the voltages (V_{dc1} , V_{dc2}) is nearly maintained at 520 V. The main drawback of this topology is the voltage unbalancing issue. The voltage unbalance is shown in Fig 5(c). This voltage will cause more stress across the VSI switches which in turn leads to a lack in the performance of the system.

V.A.2 Steady state performance of three leg single dc link capacitor based DSTATCOM

Since, the same type of loads are used in both the topologies the load currents and source currents before compensation for single dc link capacitor based DSTATCOM is same as that of the split capacitor based DSTATCOM. Fig 3 also represents the steady state performance of single dc link capacitor based DSTATCOM before compensation.



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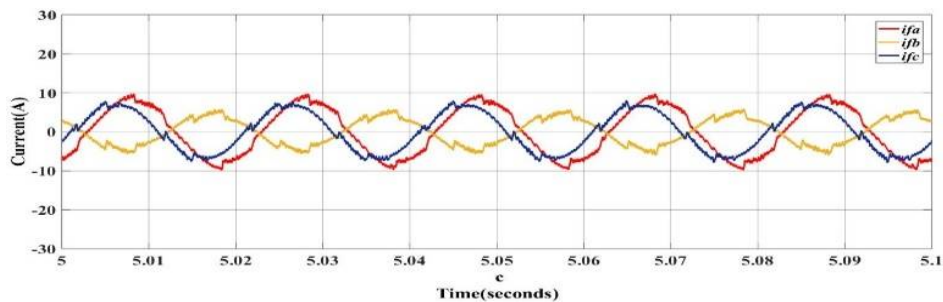


Fig. 6: Steady state performance of single dc link capacitor based DSTATCOM - a) Source voltages (V_{sabc}), b) source currents (i_{sabc}) and source neutral current (i_{sn}) after compensation, c) filter currents (i_{fabc})

Fig 6(b) shows the three phase source currents (i_{sa} , i_{sb} , i_{sc}) after the compensation provided by the split capacitor based DSTATCOM. In order to bring the source currents as balanced sinusoidal one, the compensator currents or filter currents shown in Fig 4(c) are injected into the line by means of an interfacing inductor. Source currents after compensation has equal magnitude and proper phase displacement between each other. At the same time the source neutral current (i_{sn}) also nearly limited to zero.

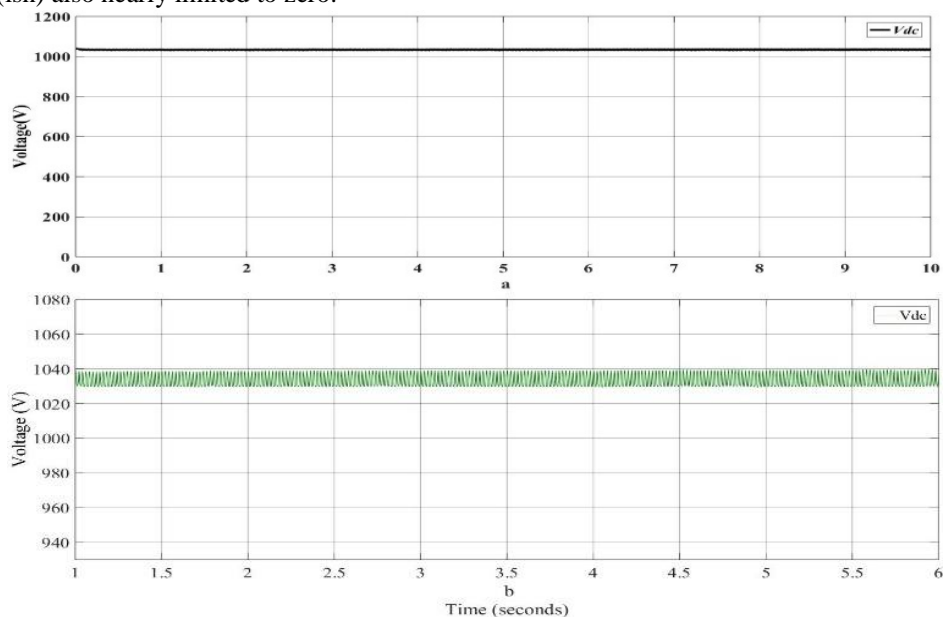


Fig. 7: DC link voltage (V_{dc}) across the dc link capacitor in single dc link capacitor based DSTATCOM - a) DC link voltage (V_{dc}) across dc link capacitor (C_{dc}), b) Zoomed view of dc link voltage across dc link capacitor

With the help of PI controller, the voltage across dc link capacitor (V_{dc}) is maintained at 1040 V. Since this topology uses only a single dc link capacitor, the voltage unbalancing issue associated with the split capacitor based DSTATCOM topology is eliminated here.

V.B Dynamic performance comparison of both the DSTATCOM topologies.

Normally, the dynamic performance of the system is tested by changing the load during the running condition. Here, it is tested under the condition that full load is changed into half load. The main aim of DSTATCOM under dynamic condition is to maintain the source currents to be balanced sinusoidal one irrespective of change in load.

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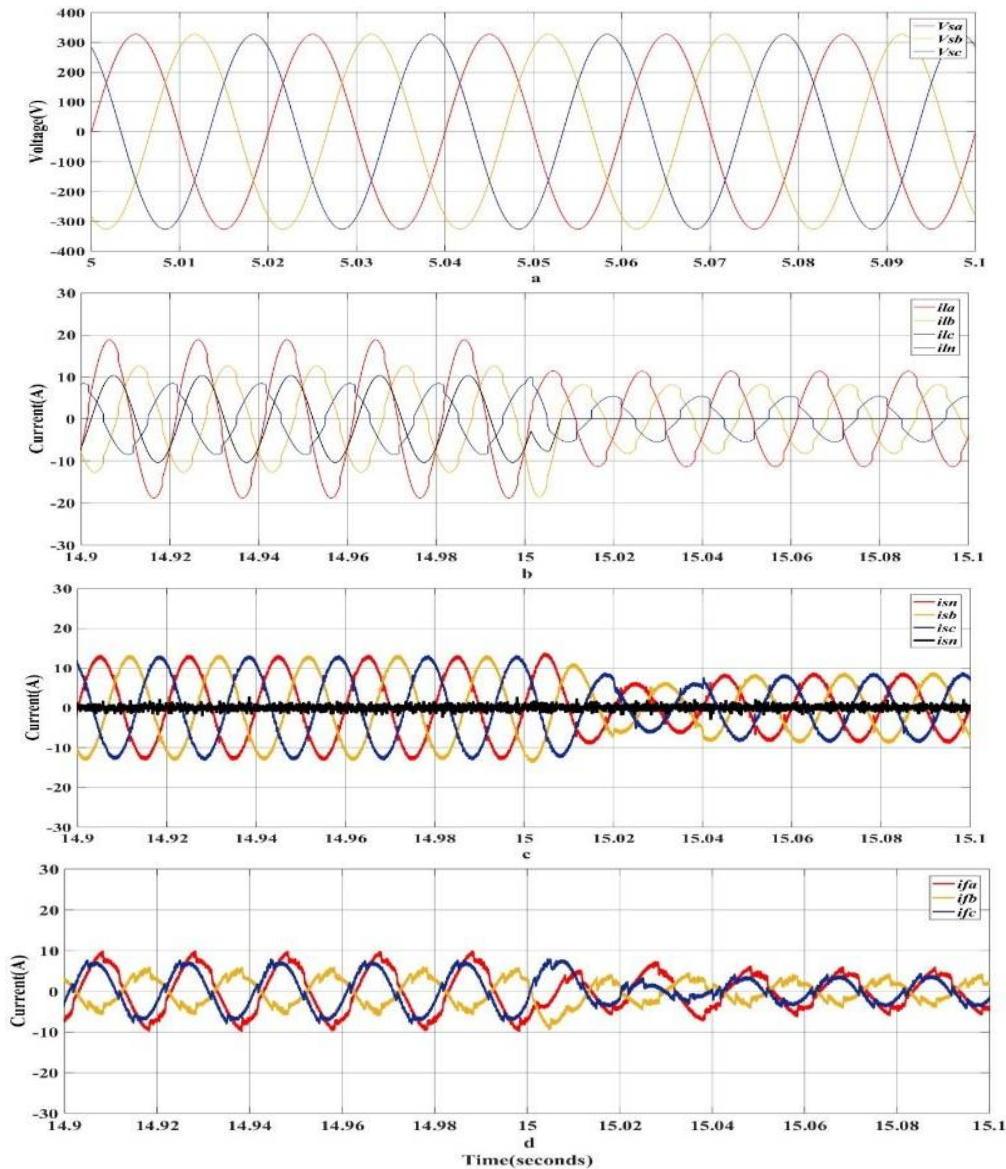


Fig. 8: Dynamic performance of split capacitor based DSTATCOM - a) source voltages (V_{sabc}), b) load currents (i_{labc}) and load neutral current (i_{ln}), c) source currents (i_{sabc}) and source neutral current (i_{sn}) after compensation, d) filter currents (i_{fabc})

In Fig 8(b), at the time of $t = 15$ seconds, the full load is changed into half load. The deviation in load currents after 15 sec, is shown in that figure. But the split capacitor based DSTATCOM provides the compensation currents into the line and brings the source currents as balanced sinusoidal one even after the disturbance occurs in the system. It is shown in Fig 8(c) and 8(d).

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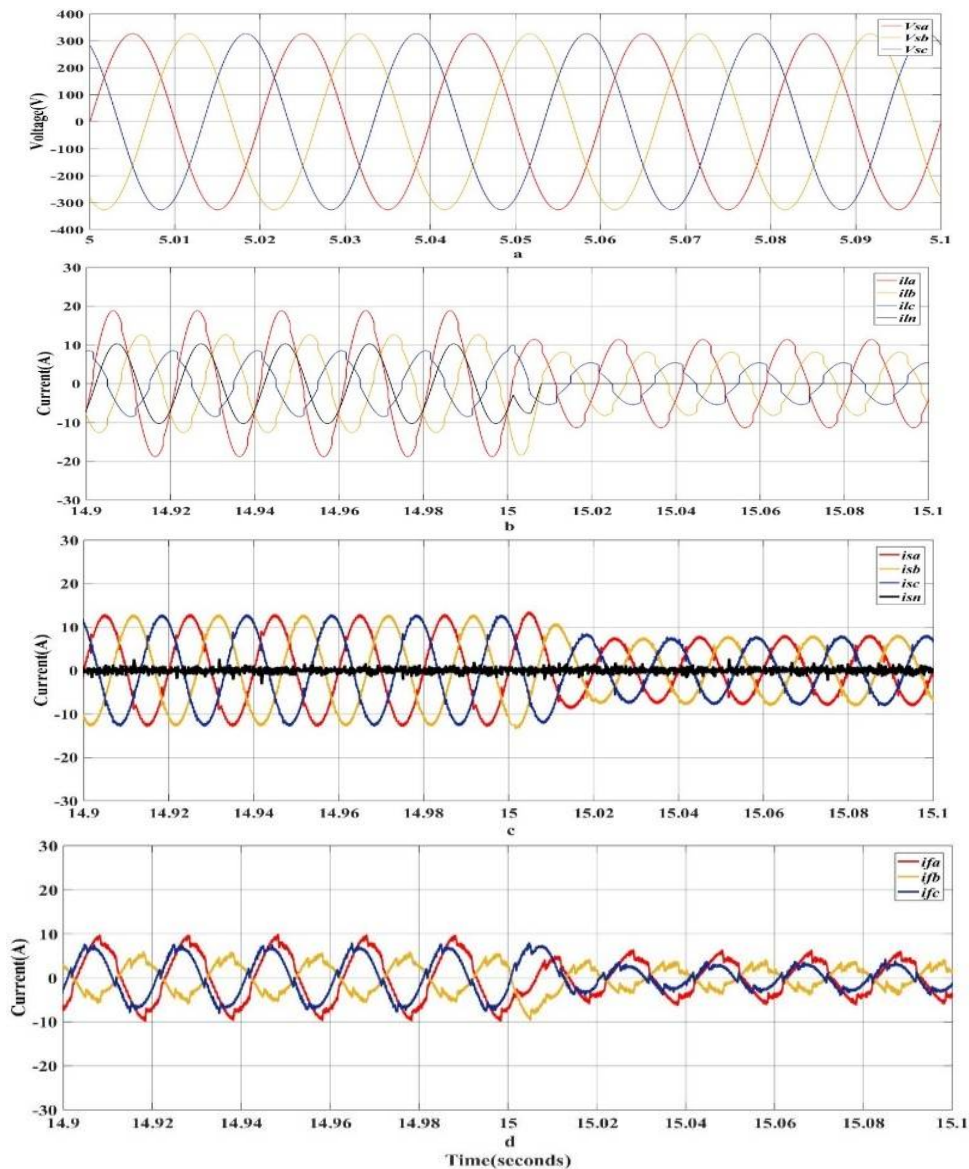


Fig. 9: Dynamic performance of single dc link capacitor based DSTATCOM - a) source voltages (V_{sabc}), b) load currents (i_{labc}) and load neutral current (i_{ln}), c) source currents (i_{sabc}) and source neutral current (i_{sn}) after compensation, d) filter currents (i_{fabc})

In this topology also, the DSTATCOM provides the compensator currents into the line and makes the source currents as balanced one. The load changes from full load to half load after $t = 15$ seconds. It is shown in Fig 9(b).

While comparing the figures 8(c) and 9(c), the time taken by the split capacitor based DSTATCOM to bring the source currents to be a balanced one after the load changes from full load to half load is somewhat higher than the single dc link capacitor based DSTATCOM. The fault or the load change appears at $t = 15$ seconds in both the topologies

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Table II: Time taken to settle after the occurrence of fault

Topologies	Settling time after the clearance of fault (seconds)
Split capacitor based DSTATCOM	0.04
Single DC link capacitor based DSTATCOM	0.01

Table II shows the split capacitor based DSTATCOM takes 0.04 second to clear the fault. But, in case of single dc link capacitor based DSTATCOM it takes only 0.01 second to clear the fault. This shows that single dc link capacitor based DSTATCOM has faster response than the split capacitor based DSTATCOM.

Table III: Simulation results: Fundamental currents value and THD (%) of source currents (i_{sabc})

Source currents (i_{sabc})	Split capacitor based DSTATCOM		Single dc link capacitor based DSTATCOM	
	Fundamental current value	THD	Fundamental current value	THD
i_{sa}	12.88	5.32	12.65	4.51
i_{sb}	12.80	5.40	12.63	4.78
i_{sc}	12.84	5.30	12.59	4.39

From the Table III, it is clearly shown that all the source currents (i_{sabc}) becomes more or less equal after compensation in both the topologies. But, Single dc link capacitor based topology is well better than Split capacitor based topology in case of total harmonic distortion. Another important factor is when the load contains more amount of dc component, it will lead to major voltage unbalancing issue across the capacitors.

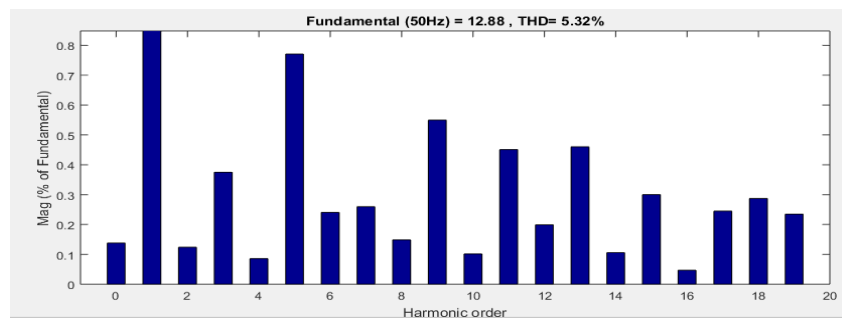


Fig. 10: Harmonic spectrum of phase 'a' in Split capacitor based DSTATCOM

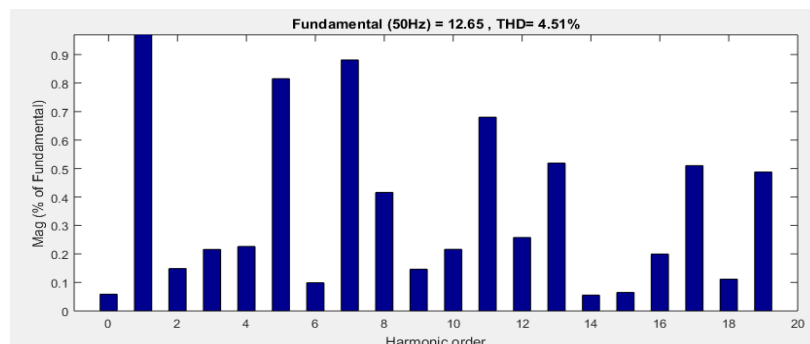


Fig. 11: Harmonic spectrum of phase 'a' in Single dc link capacitor based DSTATCOM

Fig 10 and Fig 11 shows the THD level comparison of both the DSTATCOM topologies for the phase 'a'. It is

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observed that the THD level and the amount of dc component is high in split capacitor based DSTATCOM when compared to single dc link capacitor based DSTATCOM. Since the amount of dc component is directly proportional to voltage unbalancing issue, the split capacitor based DSTATCOM having more amount of dc component is affected by more voltage unbalancing issue.

Table IV: DC component level present in both the topologies

Source currents (i_{sabc})	DC component level (% of fundamental value)	
	Split capacitor based DSTATCOM	Single dc link capacitor based DSTATCOM
i_{sa}	0.15	0.05
i_{sb}	0.2	0.1
i_{sc}	0.1	0.05

Table IV shows the amount of dc component present in three-phase source currents. It is clear that split capacitor based DSTATCOM topology has more amount of dc component than single capacitor based DSTATCOM topology. So, it shows that split capacitor topology has more voltage unbalancing issue when compared to single dc link capacitor topology.

VI. CONCLUSION

The performance of the both the topologies for power factor correction, load balancing, harmonic compensation and neutral current compensation are demonstrated through various simulation studies. Split capacitor based DSTATCOM topology has a serious problem of voltage unbalance and having more amount of dc component in it. But single dc link capacitor based DSTATCOM has the advantage of no voltage unbalancing issue and having less amount of dc component in source currents and at the same time it can able to eliminate the source neutral current (i_{sn}) with the help of small ac neutral capacitor. So overall single dc link capacitor based DSTATCOM has more advantages and performs well when compared to the split capacitor based DSTATCOM.

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