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An 8-bit 10 KS/s 400 nW SAR ADC for Biomedical Application

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ABSTRACT: All real time signals including bio signals are analog in nature. For processing, these signals are to be converted in to digital. Several analog to digital converters are available to do the same. In biomedical application such as pacemaker, there is a demand for long battery life time in order to avoid the frequent battery replacement. This can be achieved by designing low power ADCs. Of the available ADCs, SAR ADC is found to be more suitable for the conversion. This paper presents an 8-bit Successive Approximation Register Analog to Digital Converter (SAR-ADC) for biomedical application. At 10K samples/s, the SAR-ADC consumes 400 nW from a 1V power supply. The circuit is simulated using Cadence virtuoso tool under 90 nm CMOS technology. The results shows that the proposed SAR-ADC in 90 nm technology is a good candidate for biomedical medical application.

KEYWORDS: Analog-to-Digital Converter, Successive Approximation Register, Bio-signals and systems.

I. INTRODUCTION

The biomedical electronics world is rapidly changing with high future potential. With new technology, new designs with more features are placed into the biomedical devices. Nowadays, integrated circuit technology was developed in which the medical diagnostic systems can be miniaturized to portable devices. This kind of technology allow people to monitor their medical condition. One of such devices is the artificial pacemaker. The life time of the artificial pacemakers should last up to 10 years which mandate low power consumption per operation. The analog to digital converter is the crucial part of an implantable pacemaker since it consumes a large amount of power as the interface between sensed analog signal and digital signal processor block. Therefore, decreasing the power consumption of the ADC is a major concern. There are different architectures of ADC are available. These architectures have different kinds of features such as pipelined ADC whose bandwidth is usually above tens of megahertz, flash ADC which can operate in high sampling rate, sigma delta modulator has the ability to achieve high precision, and SAR ADC which owns qualities of low-power dissipation and lower chip area hence low cost; thus it is best suitable for devices, especially in wireless transmission sensor networks and medical application which requires low power dissipation, speed required is not high and resolution requirement is medium. Therefore, the SAR ADC architecture is considered in this study.

The rest of the paper is organized as follows. Section 2 explains the literature survey, Section 3 explains the architecture and the design of the SAR ADC. Section 4 discusses each building block and the simulation results. Measured results are presented in Section 4. Finally, Section 5 draws our conclusion.

II. LITERATURE SURVEY

In [1], the traditional SAR ADC is not suitable for lower supply voltage applications since low voltage causes high on-resistance of the on-off switch circuit and limits the ADC's input bandwidth. Clock boosting can solve this problem; however, the power consumption is high [2]. Reducing the power consumption of the SAR ADC becomes

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an important issue if the ADC is utilized in sensor networks or biomedical portable devices. Research approaches on reducing the power consumption of digital circuits has recently become the target in [3] and [4]. [5], uses an energy-saving method to save power consumption. [6], presented a novel dynamic latched comparator that demonstrates various efficient parameter like, lower offset voltage and higher load drivability compared to conventional dynamic latched comparators. In this novel design the comparator circuit with two additional inverters inserted between the input and output-stage of the conventional double-tail dynamic comparator, the gain preceding the regenerative latch stage is improved. The complementary version of the regenerative latch stage, which provides larger output drive current than the conventional one at a limited area, is implemented. Nevertheless, previous mentioned methods may enhance the SAR control logic complexity, and thus increases power dissipation. Hence, a 1V 8-bit 1 K Samples/s SAR ADC is presented.

III. THE ARCHITECTURE OF THE SAR ADC

The proposed SAR ADC design targets on a moderate resolution and low power consumption, therefore all the circuit components except the comparator possess single-ended structures in order to reduce power dissipation. Although a fully-differential circuit structure achieves better common mode noise rejection and less distortion. As illustrated in Fig. 1, the proposed ADC consists of a Sample-and-Hold (S/H) circuit, a charge redistribution Digital-to-Analog Converter (DAC), a comparator and a SAR control logic circuit.

It is found that adjusting the reference voltage also influences the performance of the ADC while conducting measurement. When designing the binary weighted capacitor array of the DAC, delay constant is taken into consideration so that switches coping with different values of capacitors are designed with certain proportion. The value of unit capacitor is set to be larger enough to overcome the noise of kT/C where k is Boltzmann constant, T is temperature in $^{\circ}K$, and C is the total capacitance of the capacitor array in Farad. Since the total capacitors' value is large enough to suppress kT/C noise, how to overcome the mismatch issue of the capacitor array becomes significant.

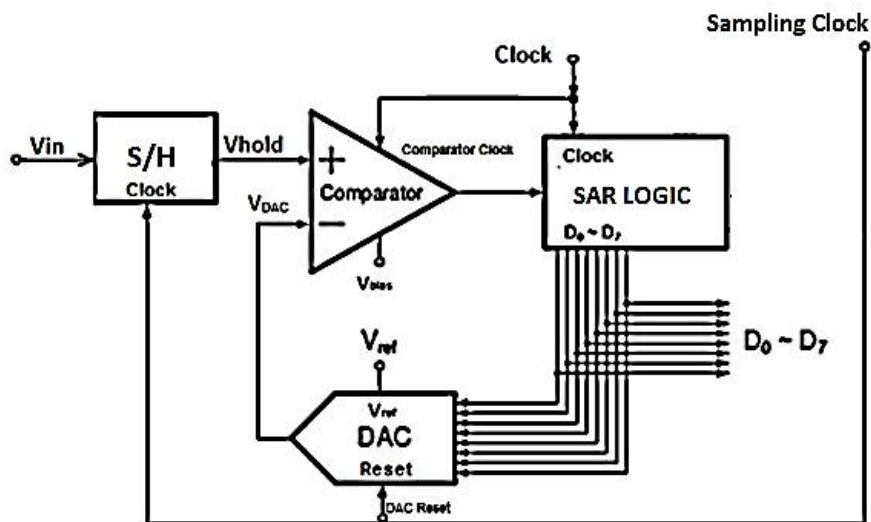


Fig. 1. Schematic of SAR ADC

IV. IMPLEMENTATIONS AND RESULTS

A. Passive Op-Amp free Sample and Hold (S/H) circuit:

Sample-and-hold (S/H) circuit is one of the main significant building block of ADCs. It is also often referred to as “Track-and-Hold (T/H)” circuit. It is the first block of the ADC components in which the input signal is seen by the input of the S/H circuit. Basic S/H circuit is a single-ended architecture. It consists of single NMOS switch and a sampling capacitor C_s . In basic S/H circuit Charge injection and clock feed through are considered to be two major problems. It happens when a transistor is used as a switch in a switched capacitor circuit. S/H circuit with Dummy Switch is considered one of the most common methods that is used to overcome the charge injection.

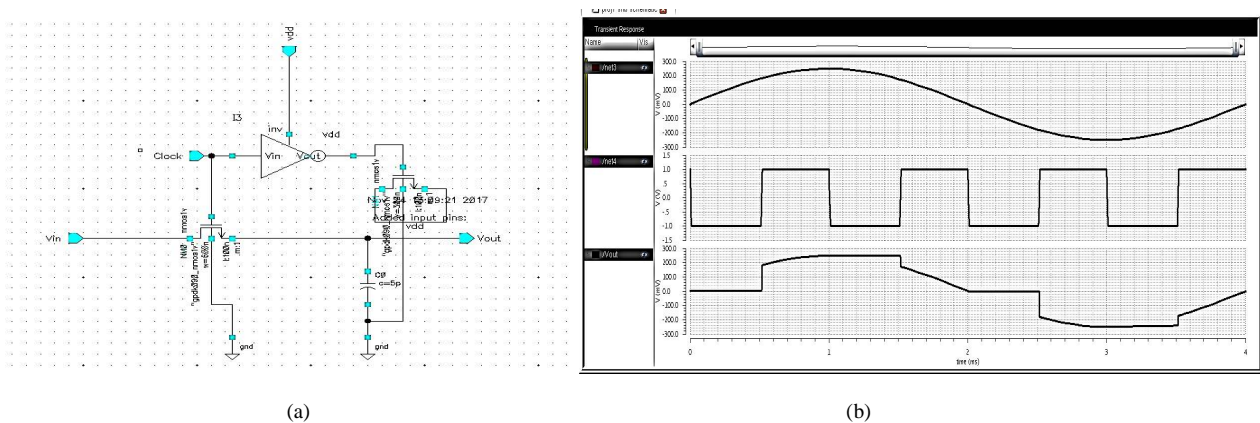


Fig. 2. (a) Schematic of the sample and hold circuit (b) Output of the sample and hold circuit

Fig. 2(a) and Fig. 2(b) shows passive Op-Amp free S/H circuit with dummy switch and the corresponding output. The frequency of the sampling clock is set to 10 KHz. The simulation is carried out for an input sinusoidal signal with peak-to-peak amplitude of 500 mV and frequency of 250 Hz. The power consumption of the sample and hold circuit is around 48 nW.

B. Comparator:

The comparator is the second most widely used component in electronic circuits, after operational amplifier. It is a key building block for applications where digital information needs to be recovered from analog signal especially in ADCs. Usually, the comparator stage is followed by a latch. Such comparators are well suited for logic circuits as the latch provides a large and fast output signal whose amplitude and waveform are independent of input signal. There are two types of comparators, namely static comparators and dynamic comparators. In static comparators, at every point in time (except during the switching transients), each gate output is connected to either (VDD) or (VSS) via a low-resistance path. It is used in medium speed applications. On the other hand, the dynamic comparators, relies on temporary storage of signal values on the capacitance of high impedance circuit nodes. It is used for high speed applications but it is more sensitive to noise. It’s worth noting that different sampling rates are used for different applications.

The trend of achieving both higher speed and lower power consumption in medium-to-high speed applications makes the dynamic comparators very attractive. It is also energy efficient design due to non-consumption of static current in contrast to the static comparator. This is done with the addition of a clock input which will block the

current to flow between the supplies. However, the dynamic comparators are more sensitive to noise compared with the static comparator.

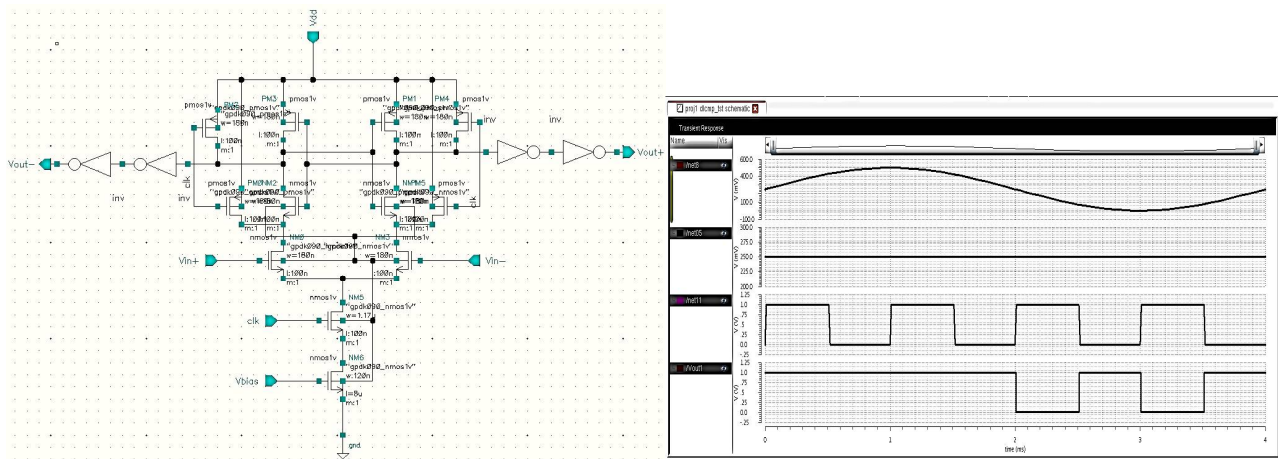


Fig. 3. (a) Schematic of the dynamic comparator with back to back inverter (b) Output of the dynamic comparator

Fig. 3(a) and Fig. 3(b) shows the schematic of dynamic latched comparator using back-to-back inverters and the corresponding output respectively. This comparator consists of a pre-amplifier stage and a track and latch stage. The pre-amplifier stage is used to amplify the input signal and block the kickback noise. Although the output signal of the pre-amplifier is larger than the input signal, it is still not large enough to drive the digital circuit. A track and latch stage is needed to amplify the signal to logic by the positive feedback loop. The advantages of this comparator is that, it achieves a fast decision due to strong positive feedback enabled by two cross-coupled pairs, and a low input referred offset enabled by the input differential pair stage. Furthermore, it offers high input impedance, full swing output and no static power consumption.

C. Digital to Analog Converter (DAC):

The main theme of this work is to reduce the power consumption therefore, the binary weighted DAC is the most suitable type in term of low power. The binary weighted type might be binary arrays of currents signals (in resistor or current approaches) or binary weighted arrays of charges. The conventional voltage driven R-2R techniques suffers from difficulties in the fabrication process. In addition to that, it requires careful control of the on-resistance ratios in the MOS switches over a wide range of values. Therefore, the binary weighted arrays of charges is preferred due to the following advantages: As the MOS device is used as a charge switch, it has inherently zero offset voltage and as an amplifier, it has very high input resistance. In addition to that, capacitors are easily fabricated in metal gate technology. As a result, using the capacitors rather than the resistors as the precision components, and using the charge rather than the current as the working medium can reduce power dissipation. Fig. 4 shows a schematic diagram of an 8-bit binary weighted switched capacitor array DAC. The performance of the DAC is completely dependent on the unit capacitance. The unit capacitance of the DAC is chosen to be 500 fF. if the unit capacitance value is increased the effect of thermal noise decreases. From Fig.4 the DAC consists of an DAC switch implemented using an PMOS and an NMOS transistor for charging and discharging capacitors. A NMOS is used as the reset switch which connects the output terminal to ground when it is turned on. The reference voltage used is 500 mV.

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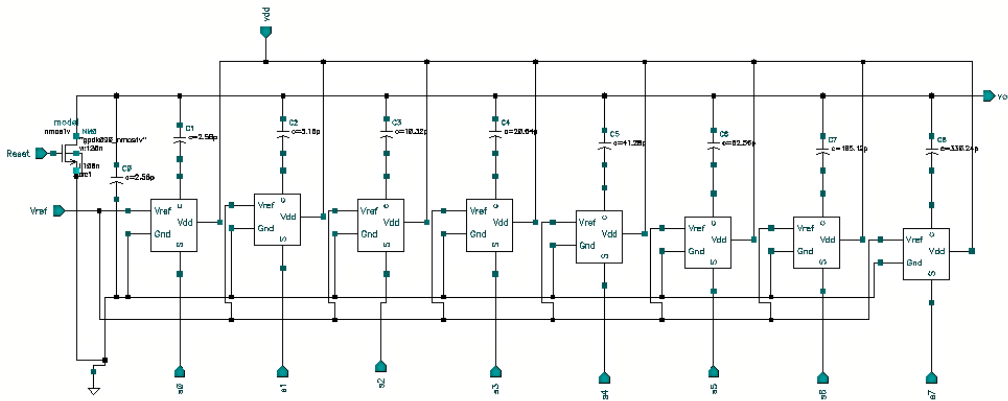


Fig. 4. Schematic of the 8-bit DAC

D. SAR Control Logic:

The SAR ADC is based on the binary search algorithm. The Successive Approximation Register (SAR) is the digital controller circuit which is responsible for executing the binary search algorithm technique. The SAR logic is the last block of the ADC components in which the output of the SAR-ADC circuit will be determined according to the comparator output. Therefore, it has a significant effect on the whole ADC performance which in turns will affect the overall system. The Successive Approximation register contains N bit for an N-bit ADC. There are three possibilities for each bit, it can be set to '1', reset to '0' or keeps its value. In the first step, MSB is set to '1' and other bits are reset to '0'. The digital word is converted to the analog value through DAC. The analog signal at the output of the DAC is inserted to the input of the comparator and is compared with the sampled input. Based on the comparator result, the SAR controller defines the MSB value. If the input is higher than the output of the DAC. The MSB remains at '1', otherwise it is reset to '0'. The rest of the bits are determined in the same manner. In the last cycle, the converted digital word is stored. Therefore, an N-bit SAR ADC takes N+1 clock cycles to perform a conversion. Fig. 5 shows the schematic diagram of SAR control logic. It consists of an SAR unit and a chain of OR gates. The SAR unit is designed using a 3:1 MUX and a D-FF. When the OR input is made high the ADC enters halt state where no conversion of takes place. The conversion is continued only when the OR input is low. The circuit is tested by assuming comparator output as '0'. Fig. 6 shows the output of the SAR control logic.

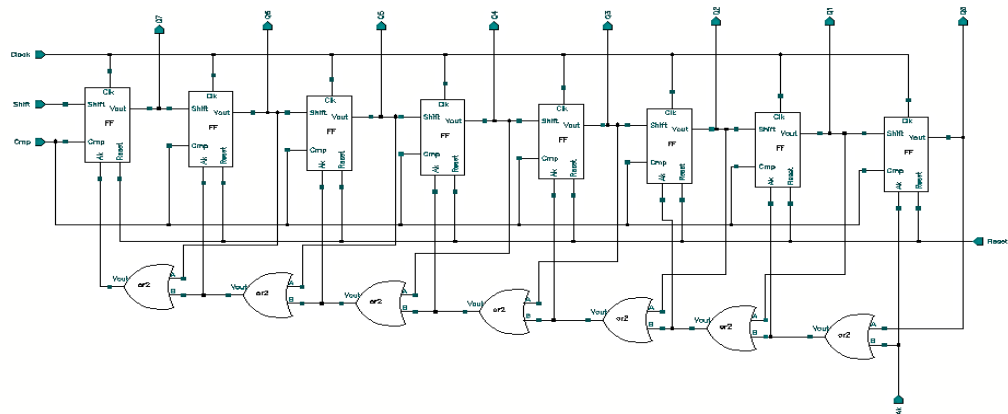


Fig. 5. Schematic of the SAR logic

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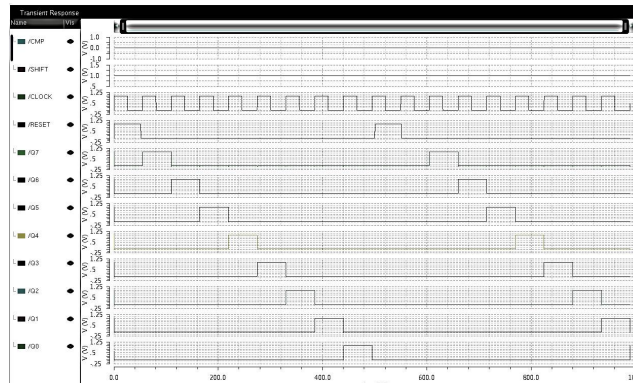


Fig. 6. Output of the SAR logic

E. SAR ADC

The 8-bit single ended DAC based SAR ADC is implemented under 90 nm CMOS technology using Cadence Virtuoso tool. The building blocks of the ADC are dynamic latched comparator with cross coupled inverters, Binary weighted switched capacitor array DAC, a SAR control logic and a sample and hold circuit with dummy gate.

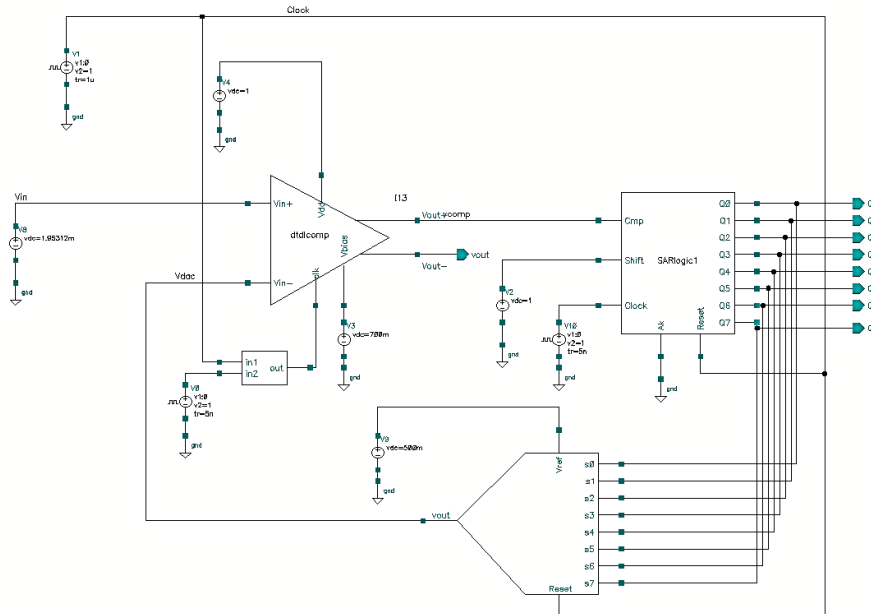


Fig. 7. Schematic of the 8-bit SAR ADC

Fig. 7 shows the schematic of 8-bit single ended SAR ADC. The ADC is simulated using Cadence Virtuoso tool under 90 nm CMOS technology. The circuit is simulated for an input sinusoidal wave of 500 mV_{pp} and frequency of 250 Hz. The sampling rate of the SAR ADC is set to 10 KS/s. The reference voltage of the DAC is set to 500 mV. The clock frequency for the comparator and the SAR control logic is set to 200 KHz.

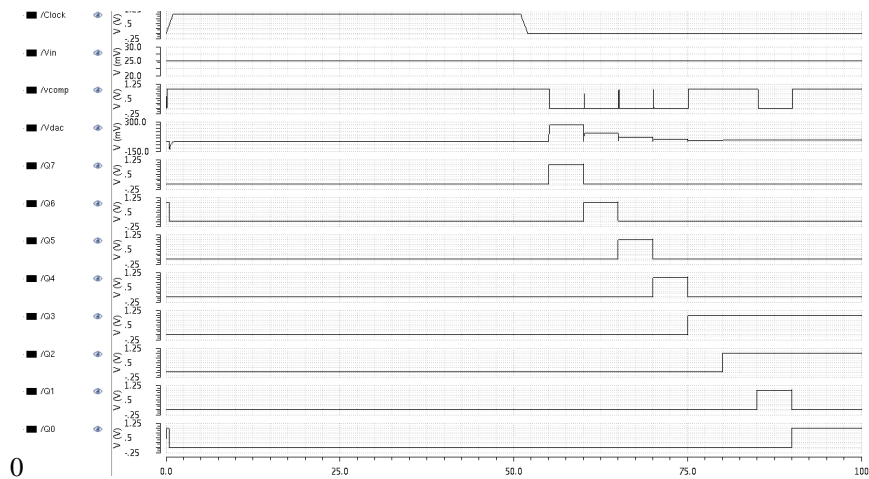


Fig. 8. Output of the 8-bit SAR ADC

Fig. 8 shows the output of the SAR ADC for an input voltage equal to 25 mV. The digital estimation of the input voltage is equal to 00001101. From Fig. 11, during the positive edge of the sampling clock (Clock) except sample and hold circuit all other circuits becomes inactive. Thus reducing the power consumption of the overall ADC. The response of the SAR ADC for different input voltage level is observed and graph are plotted (Fig. 9(a) and (b)) for finding the nonlinearities (DNL and INL) of the SAR ADC. The measured DNL and INL are +0.2/-0.6 LSB and +0.46/-0.21 LSB respectively. The signal to noise ratio (SNR) of the SAR ADC is found using MATLAB. Fig. 9(c) shows the SNR plot of the ADC. The measured SNR is 47.1 dB.

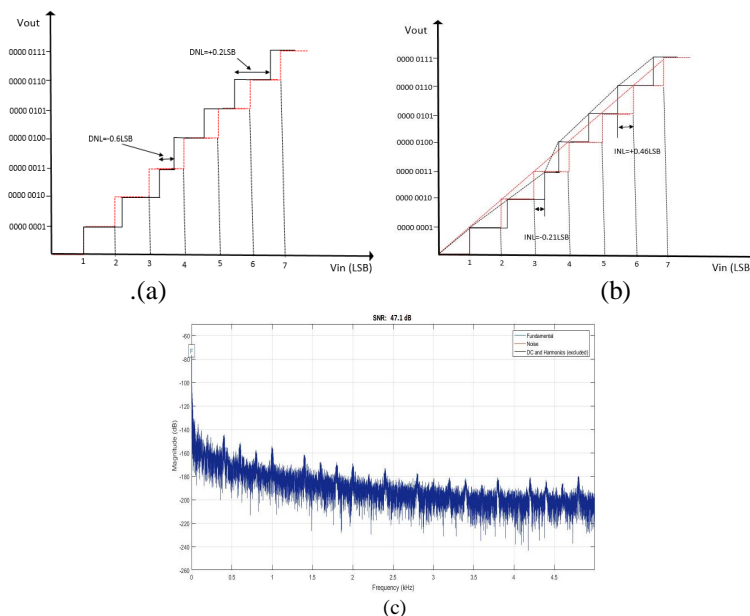


Fig. 9. (a) DNL, (b) INL and (c) SNR plot of the 8-bit SAR ADC

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Table I shows the comparison of the presented work with other work for the single ended DAC based ADC. The comparison is made based on the key performance parameters namely sampling rate of the ADC, supply voltage, resolution and power consumption of the ADC.

Table I: Performance analysis of single ended DAC based 8-bit SAR ADC

Parameters	Ref [11]	Ref [12]	This work
Technology (nm)	180	90	90
Resolution (Bits)	8	10	8
Supply voltage (V)	1.5	1	1
Power consumption (W)	120 μ	283 n	400 n
DNL (LSB)	-	0.6/-0.37	0.2/-0.6
INL (LSB)	-	0.94/-0.89	0.46/-0.21
Sampling rate (KS/s)	100	10	10
SNR (dB)	46.3	48.71	47.1
ENOB (Bits)	7.5	9.3	7.23

The power consumption of the ADC is in nW which makes it suitable for low power application namely biomedical application and wireless sensing networks. The DNL and INL (nonlinearities) are very less hence improving the accuracy of the ADC.

V. CONCLUSION

The single ended DAC based SAR ADC is implemented using 90 nm technology using Cadence Virtuoso tool at 1 V supply voltage and sampling rate of 10 KS/s. The circuits are simulated for an input signal with peak to peak voltage of 500 mV and frequency of 250 Hz using Cadence Virtuoso tool under 90 nm CMOS technology. The DNL and INL for 8-bit SAR ADC are plotted and the measured DNL and INL are 0.2/-0.6 and 0.46/-0.21 respectively. At 1 V supply voltage the SAR ADC consumes 400 nW of power.

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