

A Survey: Design of 10T Memory Cell for High Radiation Environment

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ABSTRACT In this paper, based on hardening techniques three different designs of 10T memory cells are discussed. The designs are based on the radiation tolerance capacity of the memory cell. Comparing the three technologies the radiation hardened design of 10T memory cell has increased read/write access time with enhanced reliability level in high radiation environment.

KEYWORDS: RHBD, Single Event upset, Radiation hardening.

I. INTRODUCTION

Memories represent the important part in modern circuit designs. SRAM have been widely used in various electronic systems and plays vital role in delay, area, power and reliability. In general, SRAM cells are more affected to reliability changes due to high densities, low critical charge and low supply voltage. In SRAM cells a particle impact can change the state of cells leading to formation of single event upset. The single event upset is a main reliability failure function that causes defect in electronic system by changing the stored value temporarily [4]. When the charged particles collide with a sensitive node in an integrated circuit the induced charge along with the path are collected and stored by drifting process. Once the voltage generated by stored charge is higher than the switching threshold of the circuit then the value stored in the sensitive node changes.

II. A 10T SRAM BIT-CELL WITH DIFFERENTIAL READ CAPABILITY

Due to low signal charge and reduced noise margin, nanoscale integrated circuits are extremely susceptible to particle-induced single event transients (SETs) [6], [10], [11]. Primarily, SETs are caused by alpha particles and cosmic neutrons, which originate from packaging materials and inter-galactic rays, respectively. Through direct or indirect ionization in silicon, these particles generate extra charge, which gets collected by sensitive nodes and creates voltage transients at those nodes [12]. When the amplitude and duration of the transient is large, it alters the stored value in the latch, causing a single event upset (SEU). A SEU is also referred to as a 'soft error' as it does not permanently damage the device. However, soft error can lead to system malfunctions and as such, state-of-the-art microprocessors require soft error protection [8].

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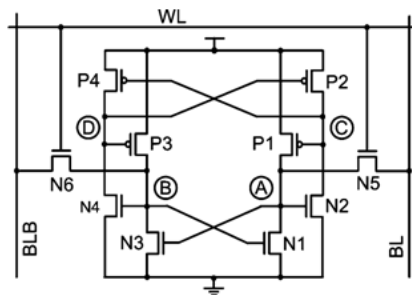


Fig 1 A soft error robust Quatro-10T cell.

The quad-node 10T or Quatro-10T cell is shown in Fig. 1. Two access transistors, N5 and N6, connect the bitlines (BL and BLB) to the storage nodes A and B. If the stored bit is '0', the logic values at nodes A, B, C, and D are '0', '1', '1', and '0', respectively. Each of these nodes is driven by an NMOS and a PMOS transistor, their gates being connected to two different nodes. As a result, if an SET pulls down (up) a node voltage, the node voltage is restored by the 'ON' PMOS (NMOS) transistor connected to the node and driven by an unaffected node. If the SET turns on a PMOS (NMOS) transistor, the transistor has to work against an unaffected 'ON' NMOS (PMOS) transistor to pull up (down) its drain voltage. Thus, a negative feedback prevents any accidental flipping of the cell.

It should be noted that if an SET simultaneously affects multiple nodes through charge sharing the proposed Quatro-10T cell may flip like the DICE cell. The probability of such a failure depends on the location, magnitude, and duration of the transients. The worst case happens when two nodes of the same potential (nodes A and D or nodes B and C) are affected. Therefore, in order to reduce the possibility of upsets due to charge sharing, the Quatro-10T is laid out by keeping the "same potential nodes" as physically apart as possible.

In a read operation, as the word line (WL) signal turns on N5 and N6, the pull-down transistor N1 (N3) discharges BL. The resulting differential bitline voltage ensures reliable sensing under the worst-case bitline leakage. The logic-0 degradation is similar to that of a 6T cell for the same driver-to-access (N1/N5) ratio. However, a larger read disturbance at logic-0 node is required to flip the Quatro-10T cell. This is because, unlike the 6T cell, the accessed node does not directly drive any PMOS transistor.

In a write operation, the Quatro-10T cell is driven to the new logic value by both bit lines. For writing 0, BL and BLB are pre-charged to '0' and '1' respectively, and the WL is activated. Once WL is high, BL pulls down the potential at node A, below V_{th} to turn off N3. In order to achieve this, N5 has to be stronger than P1.

A 10T SRAM cell designed reduces soft errors by 98% and facilitates a differential read access. Differential read is critical for easier design of the sense amplifier and for reliable sense operation under the worst case conditions. The high SNM of the proposed cell enables operating in sub-0.4 V regime to save leakage power while offering better data stability compared to the 6T cell as well as the DICE cell.

III. A 10T SRAM CELLS FOR LOW VOLTAGE OPERATION

Here two types of a soft error hardened 10T SRAM cells with high static noise margin (SNM) are proposed for low voltage operation[4]. The proposed NMOS stacked SRAM cell operates normally with higher read SNM near to sub-threshold region compared to prior works. Simulated results using 0.18um standard CMOS process demonstrate that proposed NMOS stacked-10T cell has high read SNM and high soft error resilience of at least 100 times higher than unprotected standard 6T SRAM cell for a single event transient (SET).

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SRAMs dominate CMOS computing chips taking well over half of the total transistor count of high performance ICs these days. This dominance forces designers not only to minimize both of the SRAM layout area imposing a tight transistor density and the power consumption of the SRAM but also to increase the static noise margin (SNM) [7].

To reduce power consumption, dynamic voltage scaling (DVS) is one of popular techniques for low power circuits. The power consumed by these circuits has a main component (dynamic power) that is proportional to the square of the supply voltage. Additionally, for every supply voltage, there is a maximum value of the clock frequency [9]. The advantage of using DVS is that the supply voltage (and hence clock frequency) can be adjusted depending on the specific needs during execution. Therefore, SRAM cell should be functional at lower voltage for DVS technique.

In addition, CMOS based SRAM and logic circuit elements have been facing serious reliability issues because of soft errors under standard environments. Due to low signal charge and reduced noise margin, nanoscale integrated circuits are extremely susceptible to particle-induced single event transients (SETs)

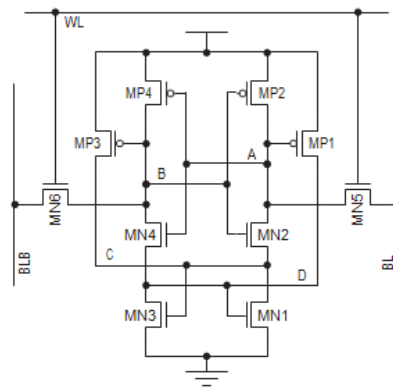


Fig 2 A hardened PMOS stacked 10T SRAM cell

Fig. 2 shows the schematic of the proposed PMOS stacked 10T SRAM cell. The cell consists of 4 PMOSs and 6 NMOSs. Two access transistors, NM5 and NM6, connect the bit lines (BL and BLB) to the storage nodes A and B. If the stored bit is '1', the logic values at nodes A,B,C and D are '1','0','1', and '0', respectively. C and D nodes are driven by MN4 and MN2, respectively. If a SET pulls down A node voltage, the node voltage is restored by the MN4 and MP2 connected to the node and driven by an unaffected node. Although the voltage of node A is changed, node C is unaffected because the node is only affected by MN4. Since MP1 and MP2 are not turned on at the same time, node A are able to be recovered '1'.

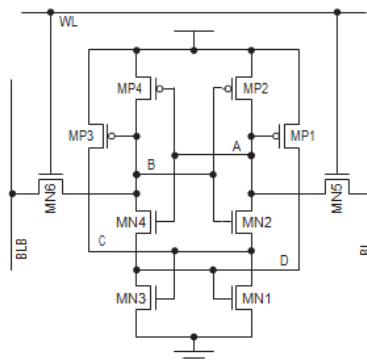


Fig 3 A hardened NMOS stacked 10T SRAM cell

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Fig. 3 shows the schematic of another proposed NMOS stacked 10T SRAM cell. The composition of the cell is same as the previously proposed PMOS stacked 10T SRAM cell but NMOSs are stacked in contrast to the previously proposed PMOS stacked 10T SRAM cell. The operation is also similar to the previously proposed PMOS stacked 10T SRAM cell. However, because node C and D are driven by MP3 and MP1, respectively, one of C and D goes to supply voltage(VDD) definitely. Therefore, the operation is ensured at lower supply voltage compared to the previously proposed PMOS stacked 10T SRAM cell.

In read operation of the proposed NMOS stacked 10T SRAM cell, as the word line (WL) signal turns on NM5 and NM6, the pull-down transistors MN2 and MN1 discharge BL if VA is '0' because VA of '0' turns on MP1 so that node D goes to '1' and MN1 turns on. For a stable read operation, the SNM depends on the aspect ratio of MN1, MN2 and MN5. Due to stacked property, MN1 and MN2 should be larger than the pull-down transistor of the standard 6T cell. However, because VA's voltage change is not related to turning MN1 on directly, which means that high SNM is not affected to VA directly, the proposed cell has larger read SNM than the standard 6T cell.

In write operation, the proposed NMOS stacked 10T SRAM cell is driven to the new logic value by both bit lines (BL and BLB). For writing 0, BL and BLB are pre-charged to '0' and '1' respectively, and the WL is activated. Once WL is high, BL pulls down the potential at node A and BLB pulls up the potential at node B. Because the response of MP1 and MP3 depends on the node A and B, MN1 and MN3 are turned on and off directly by the current driven by MP1 and MP3, respectively.

This paper shows two types of soft error hardened 10T SRAM cells. One is the PMOS stacked-10T and the other is NMOS stacked-10T. The former has soft error hardened property when '1' is stored in the bit line and the latter has soft error hardened property when '0' is stored in the bit line. The simulation results show that proposed NMOS stacked-10T cell has higher read SNM compared to not only standard-6T but also Quatro-10T. Moreover, the proposed NMOS stacked-10T cell and PMOS stacked-10T cell provide a soft error resilience of at least 100 times higher than SEU unprotected standard 6T SRAM cell.

IV. 10T MEMORY CELL WITH HIGH RADIATION HARDENING

In this design based on upset physical mechanism together with reasonable transistor size, a robust 10T memory cell is proposed to enhance the reliability level in aerospace radiation environment, while keeping the main advantages of small area, low power, and high stability[1]. Using Taiwan Semiconductor Manufacturing Company 65-nm CMOS commercial standard process, simulations performed in Cadence Spectre demonstrate the ability of the proposed radiation-hardened-by-design 10T cell to tolerate both $0 \rightarrow 1$ and $1 \rightarrow 0$ single node upsets, with the increased read/write access time.

SRAMs have been widely adopted in various aerospace electronic systems, and play a major role in the delay, area, power, and critical reliability [5]. In aerospace applications, SRAMs have a key constrain that makes a challenge in the reliability induced by energetic particles. Therefore, single event upsets (SEUs) are a major reliability failure mechanism that can cause a malfunctioning of an electronic system by altering the stored value temporarily. When the charged particle hits a sensitive node of an integrated circuit, the induced charge along its path can be efficiently collected and accumulated through drift processes. Once a transient voltage pulse generated by the accumulated charge is above the switching threshold of the circuit, the stored value in this sensitive node will be changed [2]. However, it is the fact that the SRAM cell (i.e., 6T) is usually built using two cross-coupled inverters, and the changed value in a stored node can also trigger the positive feedback mechanism to flip the state in another sensitive node so that an error occurs in the memory. Because these corrupted data can be fully recovered by overwriting operations, such a phenomenon is also reported as the soft error [3].

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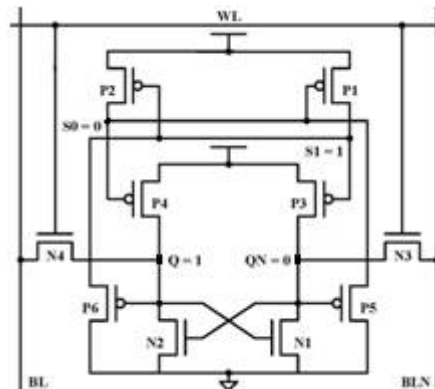


Fig 4 Schematic of a RHBD 10T memory cell.

For the given RHBD 10T memory cell, Fig. 1 describes its basic schematic structure. From this figure, it can be seen that the proposed RHBD memory cell consists of ten transistors in which PMOS transistors are transistors P1 P6, and the remaining transistors (N1 N4) are NMOS transistors. Both NMOS transistors N4 and N3 are defined as the access transistors, and their gates are connected with a wordline (WL). Hence, when this WL is in high mode (WL = 1), two access transistors are turned ON. At the moment, write/read operation can be implemented. The stored nodes are nodes Q, QN, S1, and S0 in which these four nodes are responsible for keeping the stored value correctly. In order to quickly transmit the digital signal to the output port during a read operation, a differential sense amplifier has to be employed and connected with two bit lines BL and BLN.

Assuming that the stored value of the proposed RHBD 10T memory cell is 1 in digital logic, i.e., $Q = 1$, $QN = 0$, $S1 = 1$, and $S0 = 0$, as shown in Fig. 1. It is easily concluded that the proposed RHBD 10T memory cell is steadily maintaining the stored value when WL is driven by a low voltage (WL = 0). Before normal read operation, due to precharge circuitry, the voltages of the bit lines BL and BLN will be raised to 1 in digital logic. In read operation, WL is in high mode (WL = 1), and then two access transistors N3 and N4 are turned ON immediately. Nodes Q, QN, S1, and S0 are keeping the stored value, and the voltage of bitline BL is also unchanged. However, the voltage of bitline BLN is decreased due to the discharge operation through ON transistors N1 and N3. Once the voltage difference of bitlines is a constant value which has been confirmed in the differential sense amplifier connecting with two bitlines, the stored digital signal in memory cell will be output as soon as possible. The purpose of write operation is to change the stored logical value correctly. Therefore, before write operation, due to the write circuitry, the voltages of bitline BL will be 0 in digital logic. Contrary to the voltage of bitline BL, the voltage of bitline BLN will be 1. When the voltage of WL is supply voltage VDD (WL = 1), write operation is executed. Transistors N2, P2, P3, and P6 are turned ON. At the moment, the states of transistors N1, P1, P4, and P5 will be OFF, so that the logical value of this memory cell is rightly changed to 0. Therefore, write operation can also be completed successfully.

A novel RHBD 10T cell in TSMC 65-nm CMOS process is presented. Contrasted and past solidified 10T memory cell, the proposed cell can recuperate an error in any one sensitive node. The recreation results present that the penalty presented for the proposed 10T cell is the expanded write/read get to time that may influence its applications with fast necessities. Be that as it may, while thinking about the limitations of the objective applications, contrasted and other solidified memory cells, the proposed RHBD 10T cell can be viewed as a decent decision for aviation applications as it gives a decent parity among execution, territory, power, and unwavering quality for recollections working at radiation condition.

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V. CONCLUSION

This paper proposes the survey of three different memory cell designs which are used in high radiation environment. The 10T memory cell with high radiation hardening is best suited for high radiation environment. The other designs can provide only partial single event upset robustness. Compared with previous hardened 10T memory cell, the 10T memory cell with high radiation hardening can recover an error in any one sensitive node. The simulation results present that the penalty introduced for the proposed 10T cell is the increased write/read access time that may affect its applications with high-speed requirements.

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