

A Review on “Finfets: The Emerging Technology in Field of Micro Integrated Circuits”

Prof.Sachin N. Joshi

Assistant Professor, Department of E&TC, Sanmati Engineering College, Washim, Maharashtra, India

ABSTRACT FinFET technology has been born as a result of the unceasingly intense increase in the levels of integration. The basic principle or belief of Moore's law has held true for many years from the earliest years of integrated circuit technology. Essentially it states that the number of transistors on a given area of silicon slice doubles every two years. Some of the landmark chips of the relatively early integrated circuit era had a low transistor count even though they were advanced for the time. The 6800 microprocessor for example had just 5000 transistors. Today's have many orders of magnitude more. To achieve the large increases in levels of integration, many parameters have changed. Fundamentally the feature sizes have reduced to enable more devices to be fabricated within a given area. However other figures such as power dissipation and line voltage have reduced along with increased frequency performance. There are limits to the scalability of the individual devices and as process technologies continued to shrink towards 20 nm, it became impossible to achieve the proper scaling of various device parameters. Those like the power supply voltage, which is the dominant factor in determining dynamic power, were particularly affected. It was found that optimizing for one variable such as performance resulted in unwanted compromises in other areas like power. It was therefore necessary to look at other more revolutionary options like a change in transistor structure from the traditional planar transistor.

I. INTRODUCTION

• What is a FinFET?

Type 3 DG-FETs are called FinFETs. Even though current conduction is in the plane of the wafer, it is not strictly a planar device. Rather, it is referred to as a quasi-planar device, because its geometry in the vertical direction (viz. the fin height) also affects device behavior. Amongst the DG-FET types, the FinFET is the easiest one to fabricate. Its schematic is shown in Fig. 1.

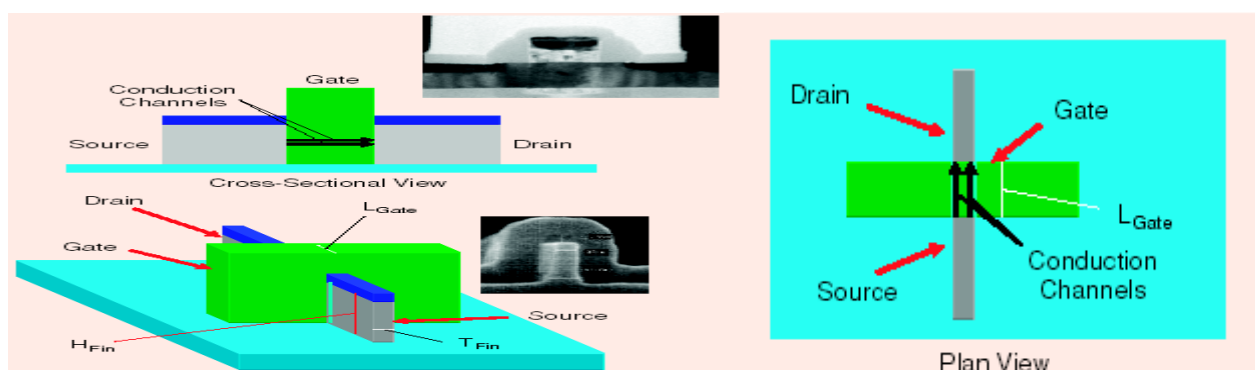


Fig. 1: FinFET structure, with dimensions marked

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Because of the vertically thin channel structure, it is referred to as a fin because it resembles a fish's fin; hence the name FinFET. A gate can also be fabricated at the top of the fin, in which case it is a triple gate FET. Or optionally, the oxide above the fin can be made thick enough so that the gate above the fin is as good as not being present. It should be noted that while the gate length L of a FinFET is in the same sense as that in a conventional planar FET, the device width W is quite different. W is defined as:

$$W = 2H_{fin} + T_{fin}$$

Where H_{fin} and T_{fin} are the fin height and thickness respectively it refers to the fin thickness as the fin width. The reason for this is quite clear when one notices that W as defined above is indeed the width of the gate region that is in touch with (ie. in control of) the channel in the fin (albeit with a dielectric in between). This fact can especially be seen if one unfolds the gate (ie. unwraps it). The above definition of device width is for a triple gate FinFET. If the gate above the fin is absent/ineffective, then the T_{fin} term in the above definition is taken out. On the surface, this freedom in the vertical direction (of increasing H_{fin}) is a much desired capability since it lets one increase the device width W without increasing the planar layout area! (Increasing W increases the I_{on} , a desirable feature). However, it will be seen in subsequent sections in this report, that there is a definite range (in relation to T_{fin}) beyond which H_{fin} should *not* be increased, else one encounters SCE.

• FinFET fabrication

The key challenges in FinFET fabrication are the thin, uniform fin; and also in reducing the source-drain series resistance. FinFET's have broadly been reported to have been fabricated in 2 ways.

- Gate-first process: Here the gate stack is patterned/formed first, and then the source and drain regions are formed.
- Gate-last process (also called replacement gate process): Here source and drain regions are formed first and then the gate is formed. Fig. 2 illustrates both processes.

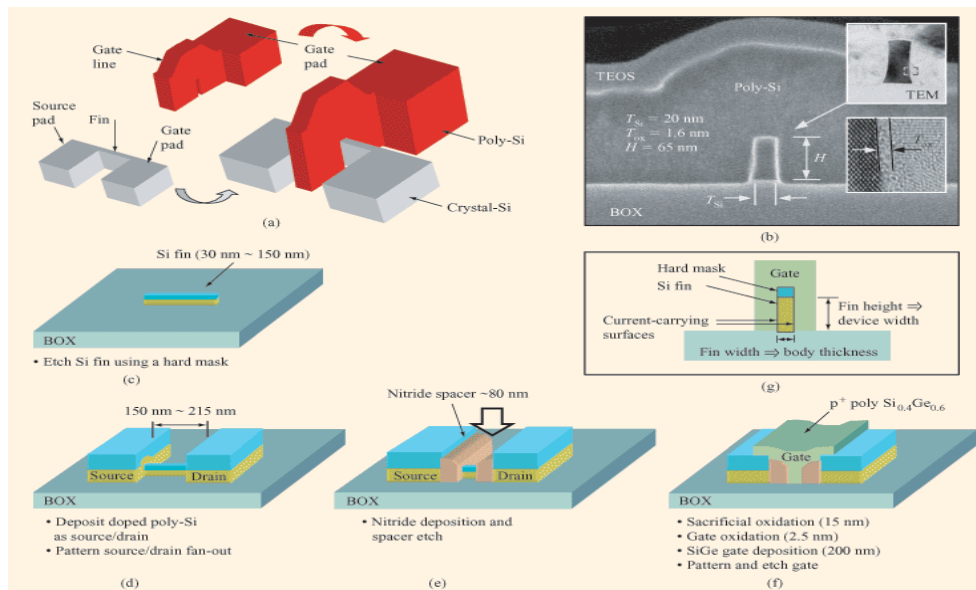


Fig. 2: High level FinFET fabrication steps; (a-b): Gate-first process, (c-f): Gate last process

FinFET's are usually fabricated on an SOI substrate. It starts by patterning and etching thin fins on the SOI wafer using a hard mask. The hard mask is retained throughout the process to protect the fin. The fin thickness is

typically half or one third the gate length, so it is a very small dimension. It is made by either e-beam lithography or by optical lithography using extensive line width trimming

In the gate-first process, fabrication steps after the fin formation are similar to that in a conventional bulk MOSFET process. In the gate-last process, the source/drain is formed immediately after fin patterning. To protect the fin while forming the other regions, doped poly or poly SiGe or even doped amorphous Silicon [8] is deposited on the fin. Then the S/D fan-out pads are patterned, leaving a thin slot between the source and the drain. This distance determines the gate length, which can be further reduced using a dielectric sidewall spacer. Finally the gate oxide is grown and the gate material is deposited and patterned.

To create thin fins very close to each other, the sidewall image transfer (SIT) technique can be used. This technique can help obtain a fin pitch that is half the lithography pitch, which is desirable because:

- It improves *device* layout density (done by creating very close fins and using a trim level to *break* the gate continuity, thus separating devices), and
- It enables having the fin pitch smaller than the fin height, which is desirable because it make the FinFET have a greater effective device width than a planar conventional FET. The SIT technique is illustrated in Fig. 3.

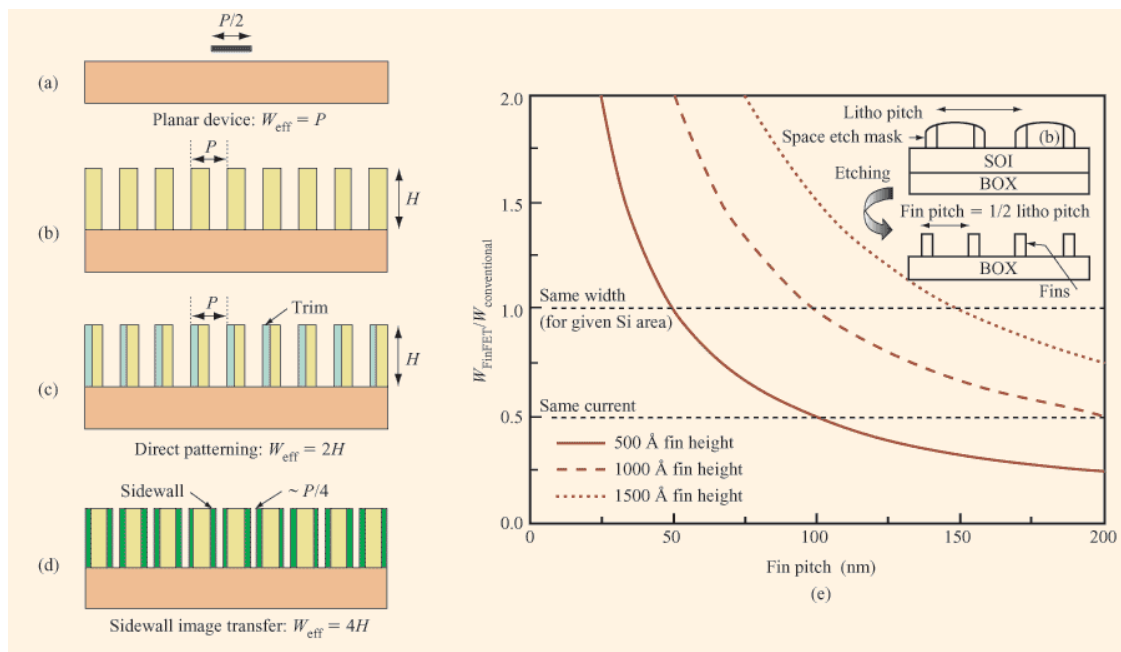


Fig. 3: Sidewall Image Transfer (SIT) technique to create closely spaced, narrow fins

II. ADVANTAGES OF FINFET TECHNOLOGY

There are many advantages to IC manufacturers of using FinFETs. The FinFET is a technology that is used within ICs. FinFETs are not available as discrete devices. However FinFET technology is becoming more widespread as feature sizes within integrated circuits fall and there is a growing need to provide very much higher levels of integration with less power consumption within integrated circuits.

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Table 1 : Advantages of FinFET Technology

FINFET ADVANTAGES	
PARAMETER	DETAILS
Power	Much lower power consumption allows high integration levels. Early adopters reported 150% improvements.
Operating voltage	FinFETs operate at a lower voltage as a result of their lower threshold voltage.
Feature sizes	Possible to pass through the 20nm barrier previously thought as an end point.
Static leakage current	Typically reduced by up to 90%
Operating speed	Often in excess of 30% faster than the non-FinFET versions.

III. CONCLUSION

FinFETs appear to be the device of choice in sub-50nm designs, because of their reduced short channel effects (SCE) and relative ease of integration into existing fabrication processes. They seem well suited to help us stay on track with Moore's law, for a little while longer. A *gate-first* method of fabricating FinFETs is advantageous in that it is more akin to the conventional CMOS process. This is probably the reason why there is more literature on this method. On the other hand, a *gate-last* method of fabricating FinFETs is advantageous from a thermal stability point of view when introducing metal gates and high-k gate dielectrics. Tall, thin fins help minimize SCE, but tend to increase series resistance. For best SCE, keeping manufacturability in mind, the ideal dimensions reported are a fin thickness of one third the channel length [6]. Tall fin heights are desirable because they yield higher ON currents (increased W_{eff}), but it gets more difficult to manufacture them with uniformly steep sidewalls. So a fine balance needs to be struck. FinFETs need to be used with metal gates with appropriate work function, for yielding desired V_T . Also, undoped fins need to be used to minimize corner effects. It was shown that Molybdenum with controlled Nitrogen doping is suitable for this. Fabrication techniques need to be improved to create thin fins with uniform thickness (uniformity across devices) as well as smooth, vertical sidewalls. These are necessary for consistent and high ON currents.

Also, the parasitic series resistance needs to be brought down to acceptable levels. People have shown lowered series resistance with raised source-drain (RSD) using selective epitaxy, and also with high angle S/D implants.

On the modeling front, compact models for FinFETs need to evolve more. Lastly, self-heating problems, which are inherent in SOI devices and not limited to FinFETs, need to be handled before FinFETs can be adopted on a large scale.

REFERENCES

1. A. Burenkov and J. Lorenz , "Corner Effect in Double and Triple Gate FinFETs", ESSDERC 2003, pp. 135-138
2. P.M. Solomon et al, "Two Gates are better than one", IEEE Circuits and Devices Magazine, Jan 2003, pp. 48-62
3. Yuan Taur, "Analytic Solutions of Charge and Capacitance in Symmetric and Asymmetric Double-Gate MOSFETs", IEEE Trans. Electron Devices, vol. 48, pp. 2861-2869, Dec 2001
4. E.J. Nowak et al, "Turning Silicon on its edge", IEEE Circuits and Devices Magazine, Jan/Feb 2004, pp. 20-31
5. Xusheng Wu et al, "Impact of Non-Vertical Sidewall on Sub-50nm FinFET", SOIC 2003, pp. 151-152
6. Gen Pei et al, "FinFET Design Considerations Based on 3-D Simulation and Analytical Modeling", IEEE Trans. Electron Devices, vol. 49, pp. 1411-1419, Aug 2002
7. H.-S.P. Wong, "Beyond the conventional transistor", IBM Journal of Research and Development (<http://www.research.ibm.com/journal/rd/462/wong.html>)
8. Digh Hisamoto et al, "FinFET—A Self-Aligned Double-Gate MOSFET Scalable to 20 nm", IEEE Trans. Electron Devices, vol. 47, pp. 2320-2325, Dec 2000.