

Comparison between Baugh Wooley Multiplier, Array Multiplier and Wallace Tree Multiplier

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ABSTRACT: A multiplier is one of the key hardware blocks in most digital signal processing(DSP) systems. Typical DSP applications where a multiplier plays an important role include digital filtering, digital communications and spectral analysis. Many current DSP applications are targeted at portable, battery-operated systems, so that the power dissipation becomes one of the primary design constraints. Since multipliers are rather complex circuits and must typically operated at a high system clock rate, reducing the delay of multiplier is an essential part of satisfying the overall design. Multiplications are very expensive and it slows the overall operation. The performance of many computational problems are often dominated by the speed at which a multiplication operation can be executed. In this paper, the following three important types of multipliers (Baugh Wooley,Array,Wallace tree) are constructed using different types of adders cells presented in (shalem.R et al (1999)),we then find out the best one in the performance characteristics like power dissipation,speed and area.

KEYWORDS: Multiplication of long bits, Baugh Wooley Multiplier, Array Multiplier and Wallace Tree Multiplier.

I. INTRODUCTION

BAUGH WOOLEY MULTIPLIER:

Baugh Wooley algorithm for the unsigned binary multiplication is based on the concept shown in figure 1.The algorithm specifies that all possible AND terms are created first, and then sent through an array of half-adders and full-adders with the carry-outs chained to the next most significant bit at each level of addition. Negative operands may be multiplied using a Baugh Wooley multiplier.

Charles R.Baugh and Bruce A.Wooley,member of IEEE presents "A Two's complement parallel array multiplication algorithm" in 1973.In this two's complement, m-bit by n-bit parallel array multiplication is described. As multiplication is an essential function in digital system due to its necessity in operation of digital filters and Fourier Transform Processor. This paper presents an algorithm for parallel two's complement multiplication. The advantage of the algorithm is the sign of all the partial products bits are positive, which need for the complement of each multiplier and multiplicand bit.Baugh Wooley algorithm is used in high performance multiplier(HPM) tree, which inherits regular and repeating structure of the array multiplier. Baugh Wooley multiplier exhibits less delay, low power dissipation and the area occupied is also small compared to other array multiplier.

Output:

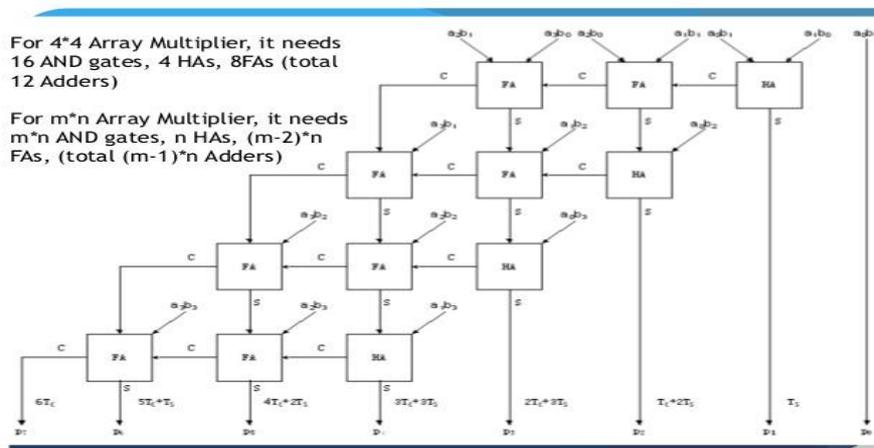
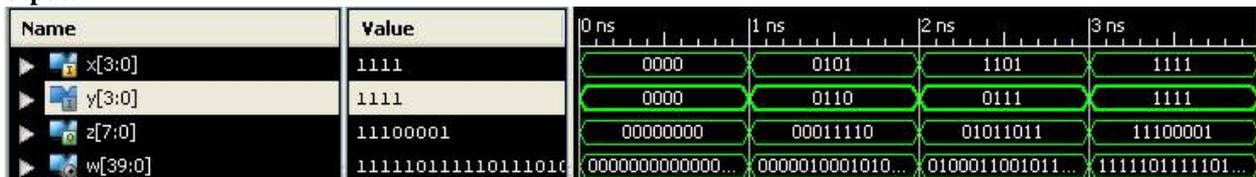


Figure-3:

Output:



Wallace tree multiplier

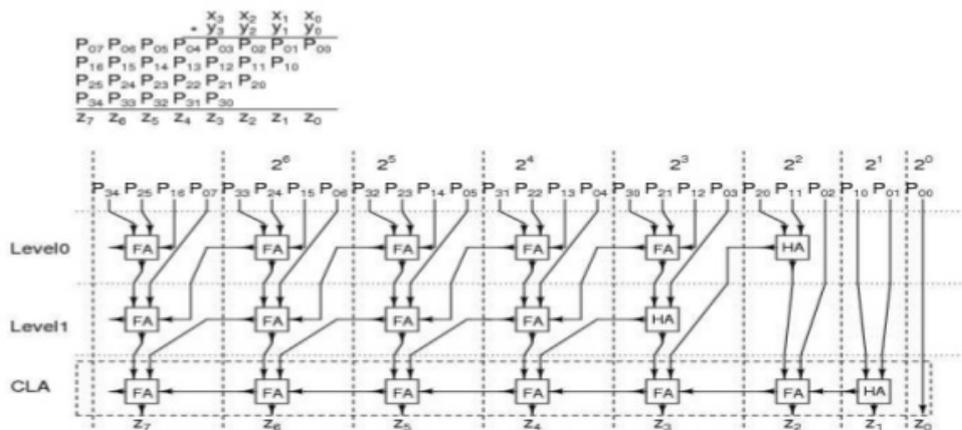


Figure-4:

Output:

| Name | Value | 0 ns | 1 ns | 2 ns | 3 ns |
|-----------|----------|----------|----------|----------|----------|
| a[3:0] | 1111 | 0000 | 0101 | 1101 | 1111 |
| b[3:0] | 1111 | 0000 | 0110 | 0111 | 1111 |
| prod[7:0] | 11100001 | 00000000 | 00011110 | 01011011 | 11100001 |

IV. CONCLUSION

Different parameters obtained from simulation that is useful for determining the efficiency of the multiplier includes power consumed and number of slices used. The delay of each multiplier is also mentioned below.

Power Consumption:

- Wallace Tree – less
- Baugh Wooley – more
- Array – most

Number of slices used:

- Wallace Tree – 17
- Baugh Wooley – 18
- Array – 18

Delay:

- Wallace Tree – 14.204
- Baugh Wooley – 12.340
- Array – 13.231

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