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Design and Implementation Low Power High Speed Multiplier using Vedic Mathematics

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ABSTRACT: In this paper, we design a high speed 16x16 CMOS Vedic multiplier, for different configuration. All simulation is done on tanner EDA TOOL 13.00 software. Urdhva tiryagbhyam Sutra is most efficient Sutra (Algorithm) for high speed multiplication, and less number of transistor count. An adiabatic logic is used to design 16 X 16 CMOS Vedic multiplier. Multiplication is one of the basic operations for any high speed digital logic system design, digital signal processors or communication system. Primary issues in design of multiplier are area, delay, and power dissipation. There are many algorithms like booth multiplier, array multiplier, vedic multiplier, compressor based Vedic multiplier for overcoming this problems.

I. INTRODUCTION

Multiplication is an important fundamental function in arithmetic operations. Multiplication-based operations such as Multiply and Accumulate(MAC) and inner product are among some of the frequently used Computation- Intensive Arithmetic Functions(CIAF) currently implemented in many Digital Signal Processing (DSP) applications such as convolution, Fast Fourier Transform(FFT), filtering and in microprocessors in its arithmetic and logic unit [1]. Since multiplication dominates the execution time of most DSP algorithms, so there is a need of high speed multiplier. Currently, multiplication time is still the dominant factor in determining the instruction cycle time of a DSP chip.

The demand for high speed processing has been increasing as a result of expanding computer and signal processing applications. Higher throughput arithmetic operations are important to achieve the desired performance in many real-time signal and image processing applications [2]. One of the key arithmetic operations in such applications is multiplication and the development of fast multiplier circuit has been a subject of interest over decades. Reducing the time delay and power consumption are very essential requirements for many applications. This work presents a different multiplier architectures. Multiplier based on Vedic Mathematics is one of the fast and low power multiplier. Minimizing power consumption for digital systems involves optimization at all levels of the design. This optimization includes the technology used to implement the digital circuits, the circuit style and topology, the architecture for implementing the circuits and at the highest level the algorithms that are being implemented. Digital multipliers are the most commonly used components in any digital circuit design. They are fast, reliable and efficient components that are utilized to implement any operation. Depending upon the arrangement of the components, there are different types of multipliers available. Particular multiplier architecture is chosen based on the application.

In many DSP algorithms, the multiplier lies in the critical delay path and ultimately determines the performance of algorithm. The speed of multiplication operation is of great importance in DSP as well as in general processor. In the past multiplication was implemented generally with a sequence of addition, subtraction and shift operations. There have been many algorithms proposals in literature to perform multiplication, each offering different advantages and having tradeoff in terms of speed, circuit complexity, area and power consumption.

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II. BASIC OF VEDIC MULTIPLIER AND ALGORITHM

Early Indian Mathematics

The early Indian mathematicians of the Indus Valley Civilization used a variety of spontaneous tricks perform multiplication. Most calculations were performed on small slate hand tablets, using chalk tables. One technique was of lattice multiplication. Here a table was drawn up with the rows and columns labeled by the multiplicands. Each box of the table is divided diagonally into two, as a triangular lattice. The entries of the table held the partial products, written as decimal numbers. The product could then be formed by summing down the diagonals of the lattice. This is shown below:

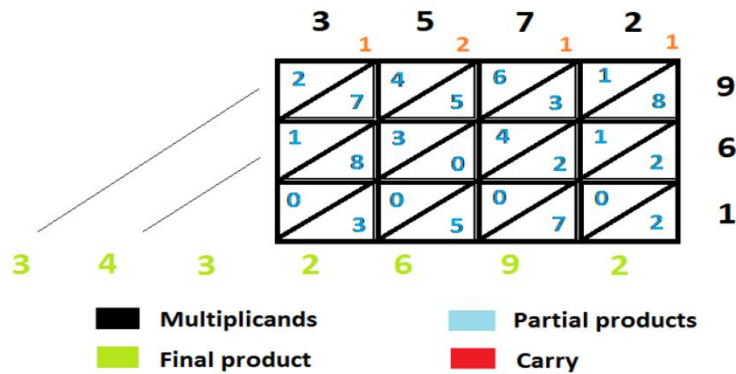


Figure 1 : Example of Early Mathematician Technique

History of Vedic Mathematics

Vedic mathematics is part of four Vedas (books of wisdom). It is part of Sthapatya- Veda (book on civil engineering and architecture), which is an upa-veda (supplement) of Atharva Veda. It covers explanation of several modern mathematical terms including arithmetic, geometry (plane, co-ordinate), trigonometry, quadratic equations, factorization and even calculus.

His Holiness Jagadguru Shankaracharya Bharati Krishna Teerthaji Maharaja (1884-1960) comprised all this work together and gave its mathematical explanation while discussing it for various applications. Swahiji constructed 16 sutras (formulae) and 16 Upa sutras (sub formulae) after extensive research in Atharva Veda. Obviously these formulae are not to be found in present text of Atharva Veda because these formulae were constructed by Swamiji himself. Vedic mathematics is not only a mathematical wonder but also it is logical. That's why VM has such a degree of eminence which cannot be disapproved. Due these phenomenal characteristic, VM has already crossed the boundaries of India and has become a leading topic of research abroad. VM deals with several basic as well as complex mathematical operations. Especially, methods of basic arithmetic are extremely simple and powerful

III. URDHVA TIRYAKBHYAM SUTRA

The multiplier is based on an algorithm Urdhva Tiryakbhyam (Vertical & Crosswise) of ancient Indian Vedic Mathematics. Urdhva Tiryakbhyam Sutra is a general multiplication formula applicable to all cases of multiplication. It literally means "Vertically and crosswise". It is based on a novel concept through which the generation of all partial products can be done with the concurrent addition of these partial products. The parallelism in generation of partial products and their summation is obtained using Urdhva Tiryakbhyam explained in fig 2.1. The algorithm can be generalized for n x n bit number. Since the partial products and their sums are calculated in parallel, the multiplier is independent of the clock frequency of the processor. Thus the multiplier will require the same amount of time to calculate the product and hence is independent of the clock frequency. The net advantage is that it reduces the need of microprocessors to operate at increasingly high clock frequencies. While a higher clock frequency generally results in

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increased processing power, its disadvantage is that it also increases power dissipation which results in higher device operating temperatures. By adopting the Vedic multiplier, microprocessors designers can easily circumvent these problems to avoid catastrophic device failures. The processing power of multiplier can easily be increased by increasing the input and output data bus widths since it has a quite a regular structure. Due to its regular structure, it can be easily layout in a silicon chip. The Multiplier has the advantage that as the number of bits increases, gate delay and area increases very slowly as compared to other multipliers. Therefore it is time, space and power efficient. It is demonstrated that this architecture is quite efficient in terms of silicon area/speed [10, 4].

Implementation of Vedic Multiplier

The designing of Vedic Multiplier is based on a novel technique of digital multiplication which is quite different from the conventional method of multiplication like add and shift. Where small blocks are used to design the bigger one. The functionality of each block is verified using simulation software, Tanner EDA 13.00v.

Block Design of 8 x 8 Bits Vedic Multiplier

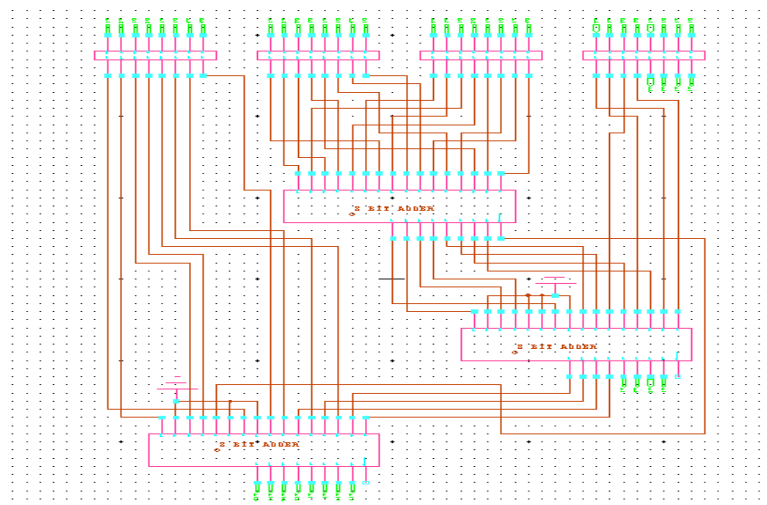


Figure 2 Circuit Diagram of 8x8 Bit Vedic Multiplier

Now the basic building block of 8x8 bit Vedic multiplier is 4x4 bits multiplier. For bigger multiplier implementation like 8x8 bits multiplier the 4x4 bits multiplier units has been used as components which are implemented already in Tanner library. The structural modeling of any design shows fastest design.

IV. RESULTS

Simulation Results of 8 x 8 CMOS Vedic Multiplier

When the given input bit $A = a_7 a_6 a_5 a_4 a_3 a_2 a_1 a_0$ & $B = b_7 b_6 b_5 b_4 b_3 b_2 b_1 b_0$

$A = 255 (1111\ 1111)$

$B = 15 (1111\ 1111)$

Then output its $S = 65,025 (1111\ 1110\ 0000\ 0001)$

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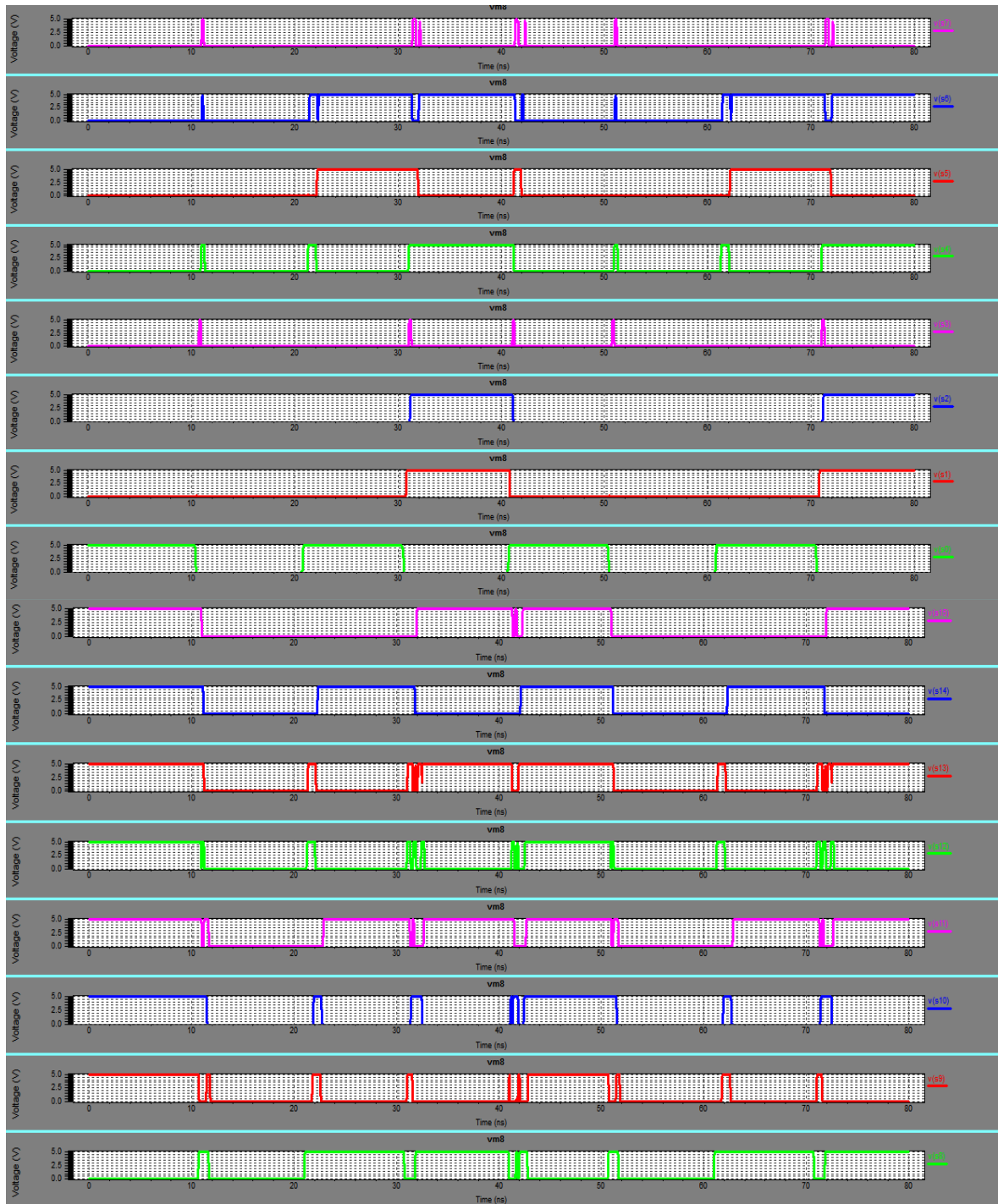


Fig 3: Output waveform of 8x8 vbedic multiplier

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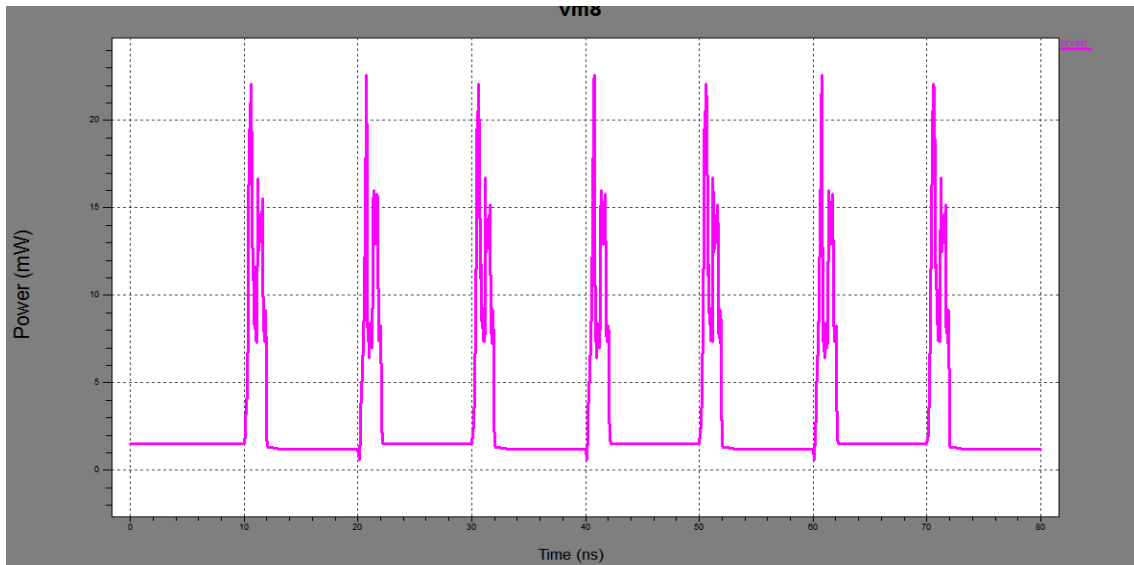


Fig 4: output power of 8x8 vedic multiplier

Table 1 : Delay and power dissipation of 8x8 Vedic Multiplier

S. No.	V _{dd} (V)	Delay (ns)	Power (mW)	Transistor count
1.	1.8	13.892	2.018	4681
2.	2	13.013	2.267	
3.	3	10.781	8.06	
4.	4	9.008	10.48	
5.	5	9.203	11.60	

V. CONCLUSION

The design of 16x16 CMOS Vedic multiplier has been implemented on Tanner EDA tool 13.00v. The computation delay for 8x8 bits Vedic multiplier is 9.203 ns at 5V and for 16x16 CMOS Vedic multiplier is 20.856ns at 5V. Since power and delay of proposed Vedic multiplier is reduced as compared to existing multiplier. Thus, it is more efficient for fast multiplication.

REFERENCES

1. Arpita S. Likhitar , M. N. Thakare , S. R. Vaidya "A Hierarchical Design of 16 -bitn Vedic Multiplier " Research Scholar, SDCOE, Wardha, India ISSN (Online): 2319-7064.
2. Akshata R , Prof. V.P. Gejji, Prof. B.R. Pandurangi," ANALYSIS OF VEDIC MULTIPLIER" International conference on computing, communication and energy systems, Dept. of Electronics and Communication Gogte Institute of Technology Belagavi, India.
3. D.Muthulakshmi1, S.Durgadevi2, B.Iyyappan, "High Speed and Reduced Area 16 bit Vedic Multiplier Using Carry Select Adder" International Journal of Advanced Research Trends in Engineering and Technology (IJARTET) Vol. II, Issue III, March 2015.
4. Poornima M, Shivaraj Kumar Patil, Shivukumar , Shridhar K P , Sanjay H, " Implementation of Multiplier using Vedic Algorithm" International Journal of Innovative Technology and Exploring Engineering (IJITEE) ISSN: 2278-3075, Volume-2, Issue-6, May 2013.
5. Sainadh chintha, Ch. Tirupathi Rao, " FPGA Implementation of Fast and Power Efficient 4 Bit Vedic Multiplier (Urdhva Tiryakbhayam) using Reversible Logical Gate", International Journal of IT, Engineering and Applied Sciences Research (IJIEASR) ISSN: 2319-4413 Volume 3, No. 10, October 2014.



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6. Shashidhar Shivanagi, Dr. A.B.Kalpana, Kumaraswamy KV, "Do-254 Implementation of High Speed Vedic Multiplier" International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering (An ISO 3297: 2007 Certified Organization)Vol. 5, Issue 5, May 2016.