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Design and Analysis of Multiplier Using GDI and CMOS Technology

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ABSTRACT: In this paper reconfigurable 8x8 Wallace Tree multiplier using CMOS and GDI technology is designed in 180nm. Wallace Tree multiplier is efficient in power and regularity without increase in delay and area. The idea is the generation of partial products in parallel using AND gates. The addition of partial products is reducing using Wallace Tree which is hierarchically divided into levels. Therefore there will be a significant reduction in the power consumption, since power is provided only to the level that is involved in computation and the remaining two levels switched off.

The result shows that the GDI based Wallace tree multiplier is performing best as compare to CMOS based multiplier. Power dissipation and delay of GDI and CMOS based Wallace tree multiplier at 1.8 V power supply is 8.8 m W & 9.6 mW and 0.02 nS & 0.17nS respectively.

All the designs have been implemented, analysed and simulated on 180 nm CMOS technology using Tanner tool 13.1.

I. INTRODUCTION

The demand for increasing speed, compact implementation and low power dissipation triggers numerous research efforts. With the scaling down of VLSI technologies, more complicate digital circuits have been implemented with a higher clock rate and lower supply voltage. However, the decreased supply voltage restricts the signal swing in circuits and brings difficulties for circuit design.

In low-voltage environments, the transistor characteristics also degrade and some circuit techniques can no longer be used, thus the low-voltage design is different from the traditional circuit design technique. Gate Diffusion input (GDI) a new technique of designing low-power digital combinational circuit. This technique allows reduction in power consumption, transistor count, propagation delay and area of digital circuits.

Motivation

The core of any kind of processor is its data path. Data path is the one of the crucial component that decides the key parameters such as the clock frequency, area and power dissipation of the design. Adders and multipliers are the main components in the data path and high performance systems such as FIR filters, microprocessors, digital signal processors, etc. A system's performance is generally determined by the performance of the multiplier because the multiplier is generally the slowest element in the system. Furthermore, it is generally the most area consuming. Hence, optimizing the speed and area of the multiplier is a major design issue. However, area and speed are usually conflicting constraints so that improving speed results mostly in larger areas.

II. BASICS OF MULTIPLIERS

Multiplication is an operation that occurs frequently in digital signal processing and many other applications. However, multipliers occupy a much larger area and incur much longer delays than adders. Therefore it is imperative that special techniques be used to speed up the calculation of the product while maintaining a reasonable area.

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The product is the result of multiplying the multiplicand to the multiplier. The multiplication operation is performed in two main steps. First is the partial product formation, which consists of AND-ing each bit of the multiplier with the multiplicand. Each successive partial product belongs one place to the left of the previous partial product. The second step is partial product accumulation, where the partial products are combined to form the result.

3.1 Basic Multiplication Process

The operation of multiplication is rather simple in digital electronics. It has its origin from the classical algorithm for the product of two binary numbers. This algorithm uses addition and shift left operations to calculate the product of two binary numbers. Techniques involve computing a set of partial products, and then summing the partial products together.

A generic block diagram of multiplier is shown in figure 1. In $M \times N$ -bit multiplication can be viewed as forming N partial products of M bits each, and then summing the appropriately shifted partial products to produce an $M+N$ -bit result as product. Binary multiplications is equivalent to a logical AND operation. Therefore, generating partial products must be added and, if necessary, any carry values passed to the next column.

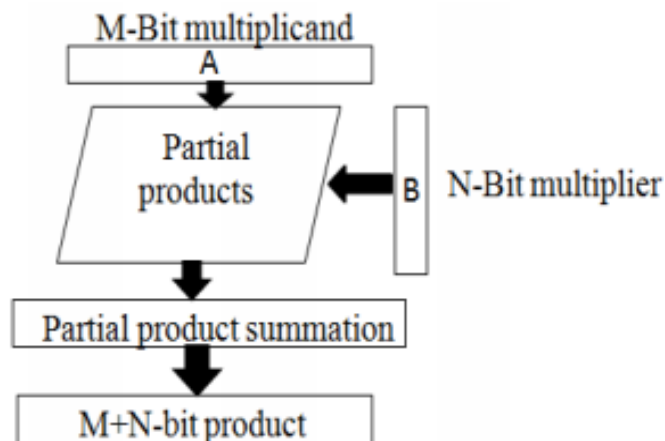


Fig 1: Generic Multiplier Block Diagram

The most basic form of multiplication consists of forming the product of two unsigned(positive) binary number [36]. This can be accomplished through traditional technique simplified to radix 2.

```

1011 (this is 11 in binary)
× 1011 (this is 11 in binary)
=====
1011 (1011 × 1)
1011 (1011 × 1, shifted one position to the left)
0000 (1011 × 0, shifted two positions to the left)
+1011 (1011 × 1, shifted three positions to the left)
=====
01111001 (this is 121 in binary)

```

The above example shows the multiplication process of two unsigned binary digits. The first digit is called Multiplicand and the second one is Multiplier. Partial product generation is the very first step in binary multiplier. If the multiplier bit is “0”, then partial product row is also zero, and if it is “1”, then the multiplicand is copied as it is. From the 2nd bit multiplication onwards, each partial product row is shifted one unit to the left as shown in the above mentioned example.

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Multiplication involves two basic operations:

- Generation of the partial product
- Their accumulation

Partial Product Generation Method

A partial product formed by multiplying the multiplicand by one digit of the multiplier when the multiplier has more than one digit. Partial products are used as intermediate steps in calculating larger products. Fig 2 shows the block diagram of partial product generation.

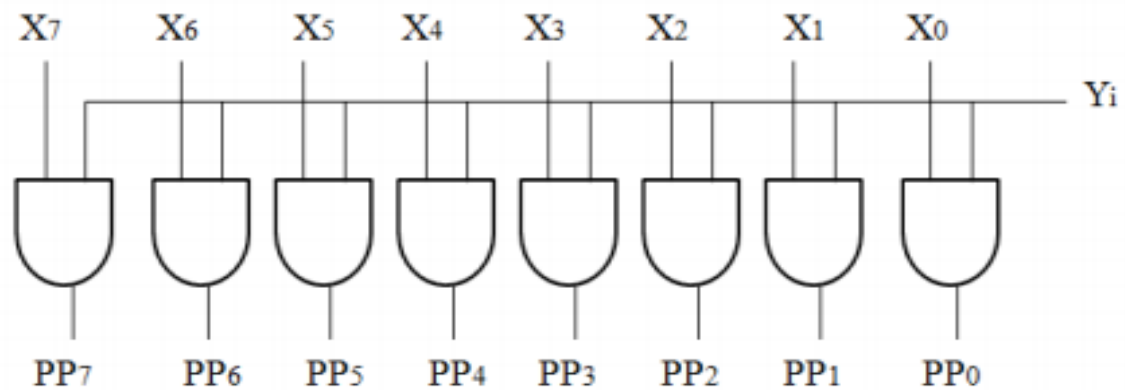


Fig 2: Generation logic of partial product

There are two ways to improve the speed of multiplication operation.

- Speed up the process of partial products generation.
- Reduce the number of partial products that needs to be generated.

The first option can be achieved by using different architecture for partial product generation. Considering if a bit is generated with just an AND gate delay, it seems that the partial product bits are already calculated in the fastest way possible. AND operation is equivalent to multiplication on two numbers. The second option will most likely take longer than an AND gate, but it reduces the number of partial product results in a smaller tree and save the time of partial product generation Thus it would be beneficial to implement this option.

Modified Booth Multiplier

Block diagram of the Modified Booth multiplier is shown in fig3. This circuit takes two 8-bit binary numbers and produces the 16-bit product. The multiplier, $X[7:0]$, is divided into four groups: 0, X_0, X_1 ; X_1, X_2, X_3 ; X_3, X_4, X_5 ; X_5, X_6, X_7 .

Each of these groups is passed into a Booth encoder, which outputs bits corresponding to the operations. Each group of these selection bits are sent to a Booth decoder block, which outputs the appropriate partial product term based on the selected operation. These partial products are then sign extended so that sign bits are taken in to account during the summing.

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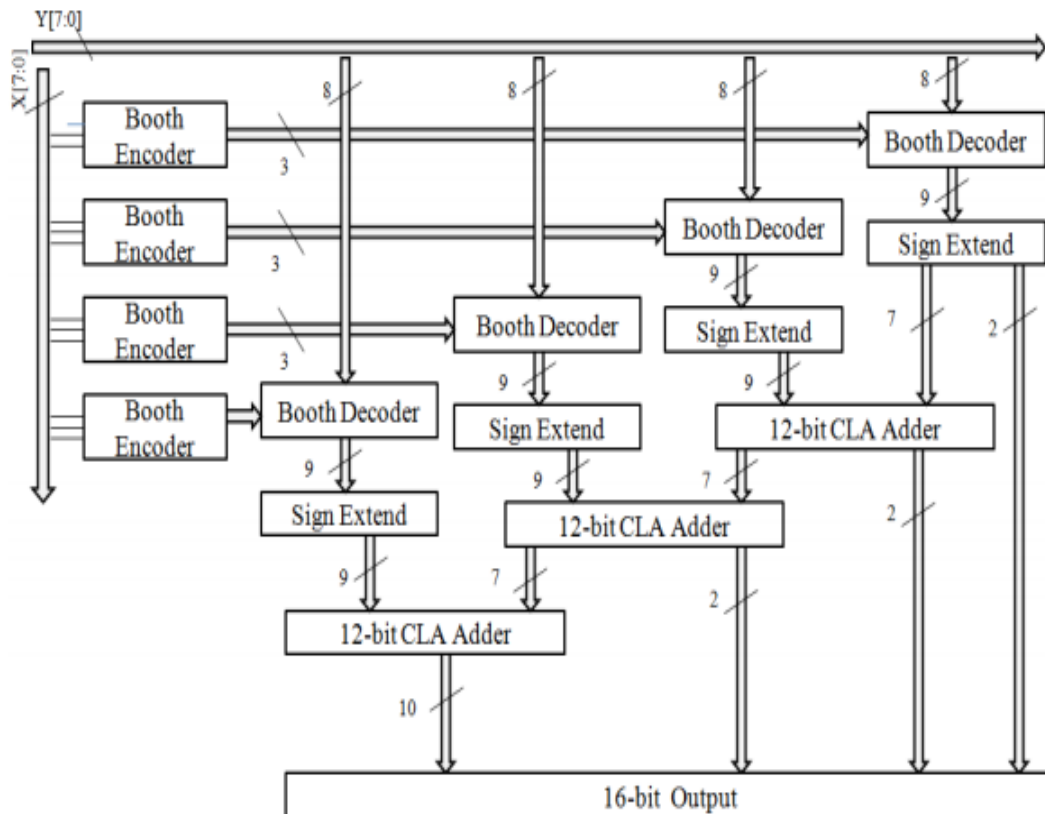


Fig 3: Modified Booth Multiplier

8-BIT Multiplier

8x8 bit multiplier architecture based on Wallace Tree is shown in fig 4.19, which is efficient in terms of power and regularity without increase in delay and area. The idea involves the generation of partial products in parallel using AND gates. The addition of partial products is done using Wallace tree, which is hierarchal, divided into levels. There will be a reduction in the power consumption, since power is provided only to the level that is involved in computation. Hardware realization of 8 x 8 multiplier is shown in fig 4.

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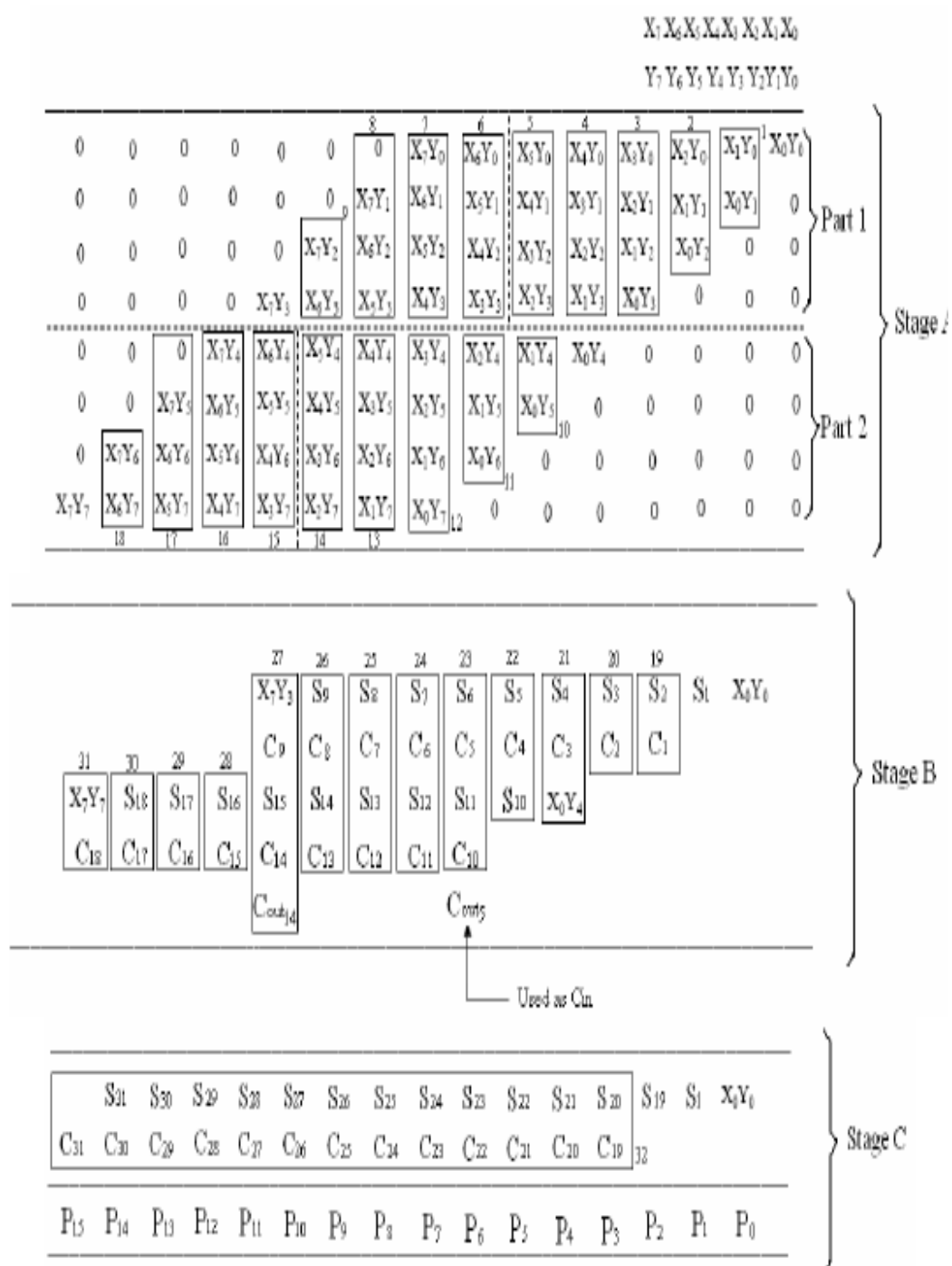


Fig 4: Hardware implementation of 8 x 8 Multiplier

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Schematic diagram of GDI based 8 x 8 multiplier is shown in fig 5.

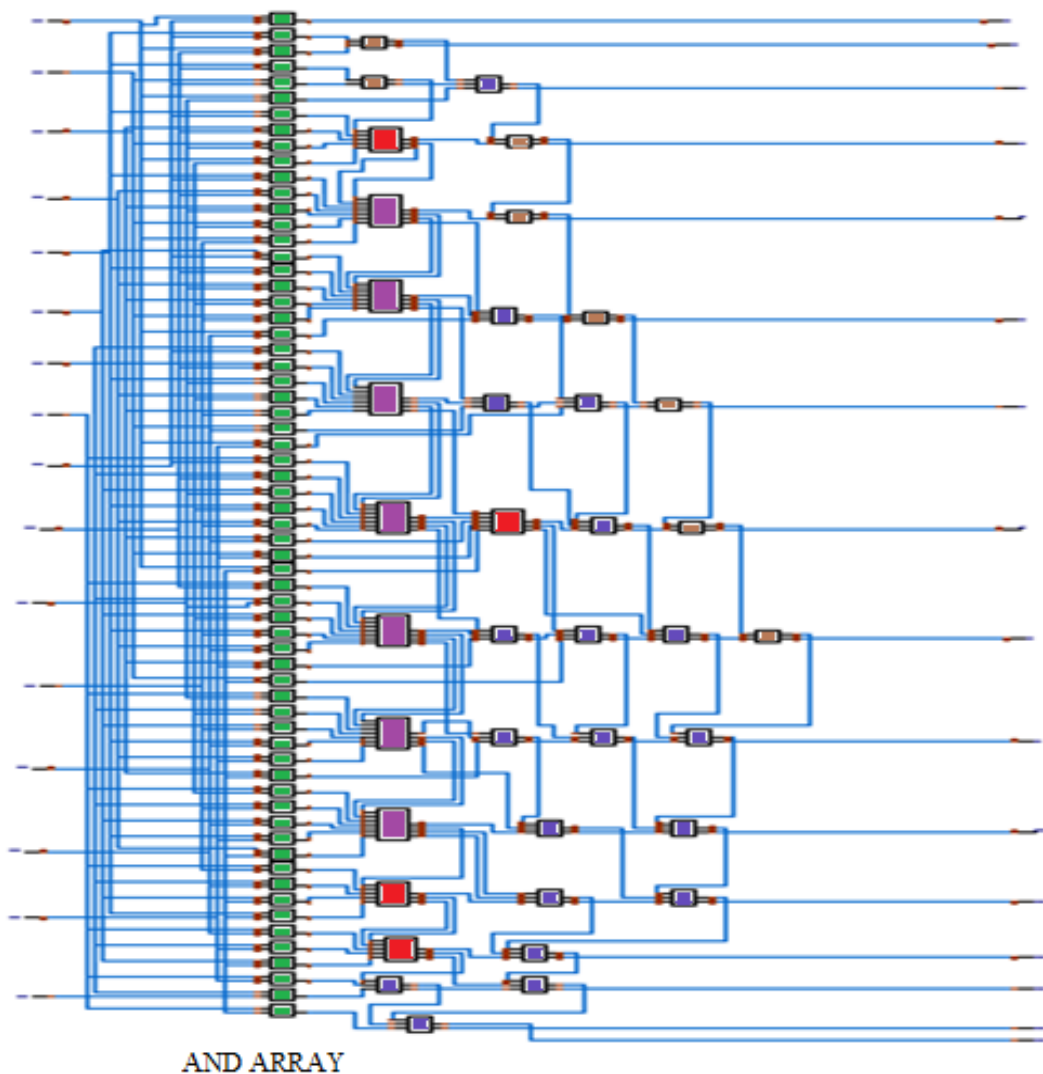
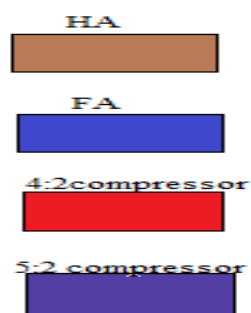


Fig5: 8-Bit Multiplier



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III. SIMULATION RESULT AND ANALYSIS

8-BIT Multiplier

Simulated waveform of 8-bit GDI based multiplier is shown in fig 6. Multiplier and multiplicand inputs each are of 8 bits. After multiplication 16-bit partial products are generated.

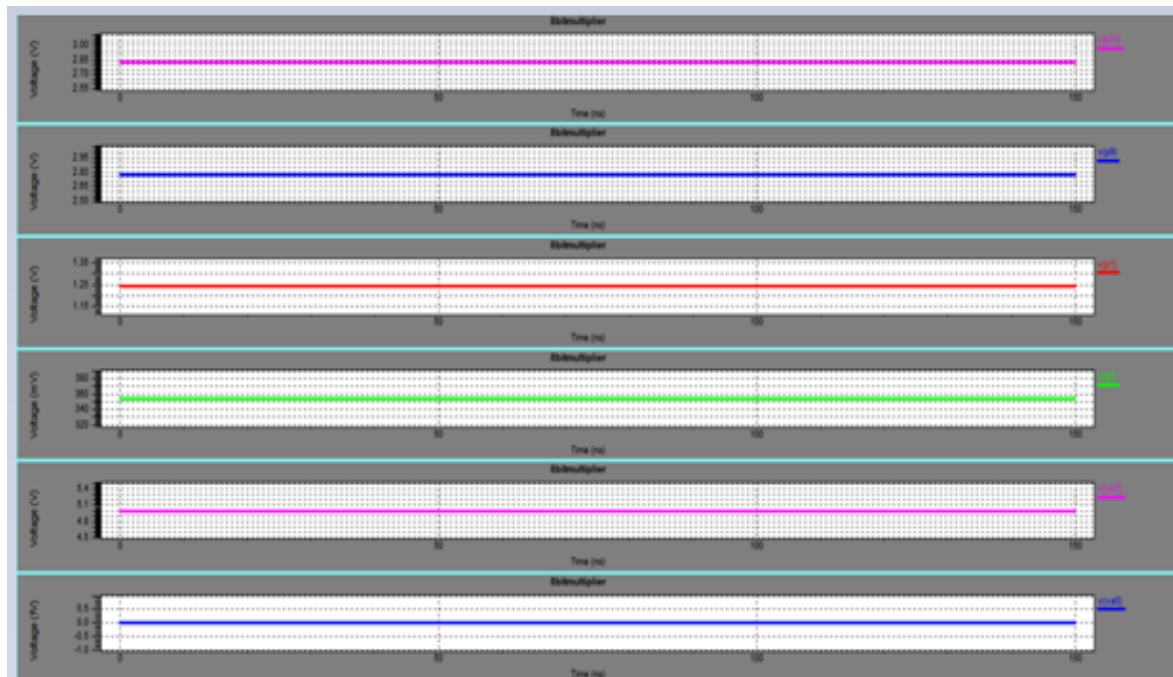


Fig 6: Waveform of 8-bit GDI based Multiplier

Propagation delay and power dissipation of both 4-bit CMOS multiplier and 4-bit GDI multiplier is listed below in table 1 and table 2 respectively.

Table 1
Parameter of 8-bit GDI multiplier

Vdd(V)	Delay(ns)	Power Dissipation (mW)
1.8	0.02	8.854
1.6	0.40	8.395
1.4	0.65	7.975
1.2	0.72	7.414
1.0	0.82	6.756

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Table 2
Parameter of 8-bit CMOS multiplier

Vdd(V)	Delay(ns)	Power Dissipation(mW)
1.8	0.17	9.64
1.6	0.56	9.19
1.4	0.70	8.57
1.2	0.80	7.84
1.0	0.95	6.95

IV. CONCLUSION

Multiplier is one of the most important components of many digital signal processing, general purpose processing, image processing and other digital application. Multiplier performance can be measured by using performance factors like Power, Delay and area. In efforts to identify the most efficient multiplier, this research makes the following conclusions.

The GDI based wallace tree multiplier occupies smaller silicon area with higher resolution than the conventional wallace tree multiplier. Various parameters like delay and power dissipation of other circuits are also calculated with respect to different power supply. Result shows that Power dissipation and delay of GDI based Wallace tree multiplier at 1.8V power supply is 8.8mW and 0.02 nS respectively and total transistor count is 912

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