

Design of Subthreshold Adiabatic Logic based Combinational and Sequential Circuits using Fin-FET

N. Sunmathi, G. Sariga

UG Student, Dept. of ECE, Builders Engineering College, Tirupur, Tamilnadu, India

ABSTRACT: Power consumption is most important for VLSI circuits. Adiabatic is an energy conserving logic for ultra-low power circuits. Adiabatic logic is an energy efficient logic. Subthreshold adiabatic logic (SAL) is an approach for low power consumption and works at low frequency. In this paper combinational and sequential circuit is designed using CMOS SAL and Fin-FET SAL in LTspice software. Power relation table says that the Fin-FET SAL consumes less power compared to CMOS SAL.

KEYWORDS: Subthreshold Adiabatic Logic (SAL), Halfadder, D- Flipflop, Half subtractor, 2bit binary multiplier, Low power consumption.

I. INTRODUCTION

The primary concern of portable device is high power consumption than performance. For VLSI circuit low power consuming capability is the most important parameter. There are many methods used to reduce the power consumption. Adiabatic logic is one of those methods. Adiabatic circuit works effectively at low frequencies but fail to function at high frequencies. Subthreshold adiabatic logic performs below threshold voltage. Fin-FET SAL consumes less power compared to CMOS SAL.

II. CMOS TECHNIQUE

CMOS stands for Complementary Metal-Oxide-Semiconductor. It is a technology for constructing integrated circuits. It is the pair of p-type and n-type MOSFETs. Two important characteristics of CMOS devices are high noise immunity and low static power consumption. It is also widely used for RF circuits. It consumes low power.

III. Fin-FET TECHNIQUE

Fin-FET technology is booming in the integrated circuits and chip manufacturing industries. It is a 3D transistor. It is mainly used in the smart phones. The Fin-FET devices have significantly faster switching times and higher current density than the CMOS technology. It consumes low power than CMOS technology.

IV. ADIABATIC LOGIC

An adiabatic process occurs with transfer of heat or mass of substances between a thermodynamic system and its surroundings. In an adiabatic process energy is transfer to the works.

Adiabatic process doesn't follow the second law of thermodynamics. Adiabatic circuits reuse the energy stored in the load capacitor.

Fin-FET technology consumes less power compared to conventional CMOS. Fin-FET uses DC voltage source to charge load capacitor, total energy drawn from power supply, half of energy stored in load capacitance and remaining

International Journal of Innovative Research in Science, Engineering and Technology

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Visit: www.ijirset.com

Vol. 8, Issue 2, February 2019

half of energy dissipated in PMOS network. During discharging time energy stored in capacitive load and dissipated in NMOS network.

In adiabatic logic circuits energy dissipation is less than normal Fin-FET technology. If capacitor charging time is increased automatically reduce the energy dissipation.

Now adiabatic logic has new diversion that circuits are designed to operate in subthreshold and weak inversion region. Subthreshold logic works at ultra-low power.

V. SUBTHRESHOLD LOGIC

Subthreshold circuit operates below the threshold voltage.

$V_{GS} < V_{th}$ --Subthreshold region

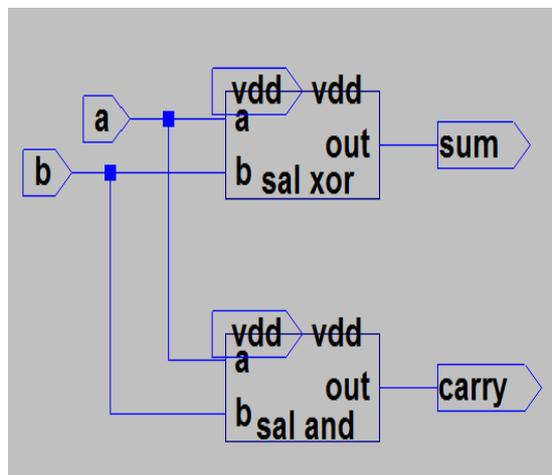
It is a novel approach for low energy consumption. It widely used low frequency applications.

VI. RESULTS

I. HALF ADDER

Adder is most important block for arithmetic and logic circuits. The half adder has two inputs and two outputs, sum(S) and carry(C). The half adder designed using XOR gate to generate sum, AND gate for carry.

Half adder with CMOS subthreshold adiabatic logic (SAL) is designed and simulated by LTspice 45nm technology. For supply voltage 200mv and operating frequency 1 kHz is analyzed.



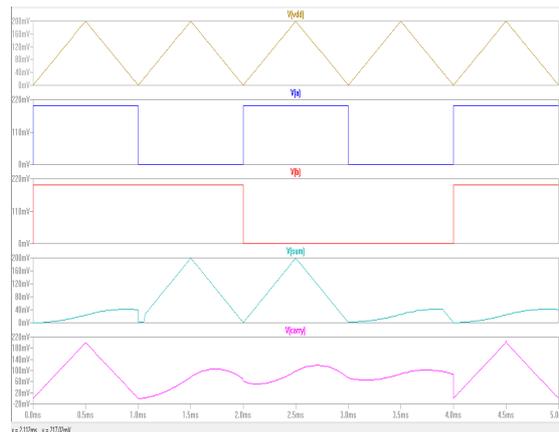
The first, second and third waveforms from top to bottom shows three input signals. The fourth waveform shows sum signal and fifth signal shows carry signal.

International Journal of Innovative Research in Science, Engineering and Technology

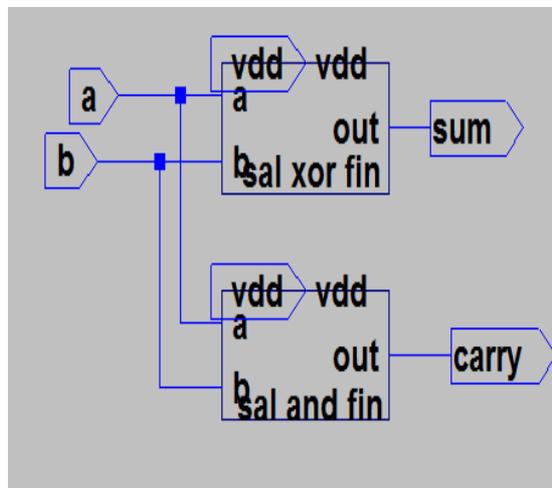
(A High Impact Factor, Monthly, Peer Reviewed Journal)

Visit: www.ijirset.com

Vol. 8, Issue 2, February 2019



Half adder with Fin-FET SAL is designed and simulated by LTspice 45nm technology. For supply voltage 200mv and operating frequency 1 kHz is analyzed.



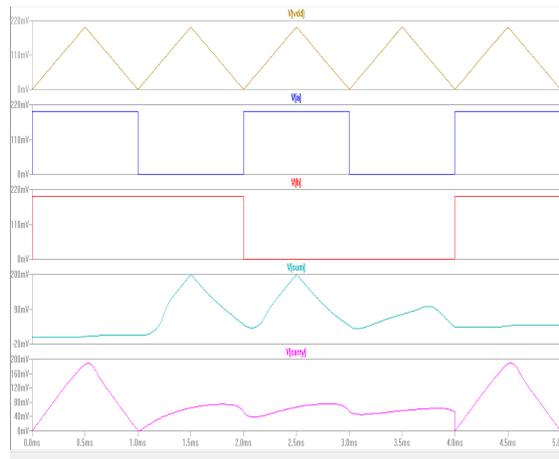
The first, second and third waveforms from top to bottom shows three input signals. The fourth waveform shows sum signal and fifth waveform shows carry signal.

International Journal of Innovative Research in Science, Engineering and Technology

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Visit: www.ijirset.com

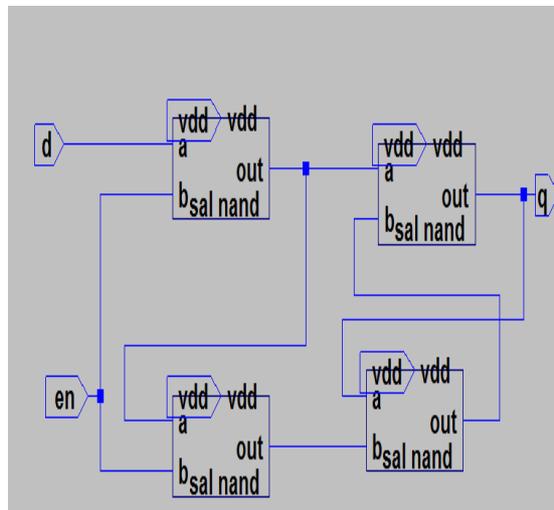
Vol. 8, Issue 2, February 2019



II. D-FLIPFLOP

D-Flipflop has two inputs(enable, data) and one output(Q) signal.

D-Flipflop with CMOS SAL is designed and simulated by LTspice 45nm technology. For supply voltage 200mv and operating frequency 1 kHz is analyzed.



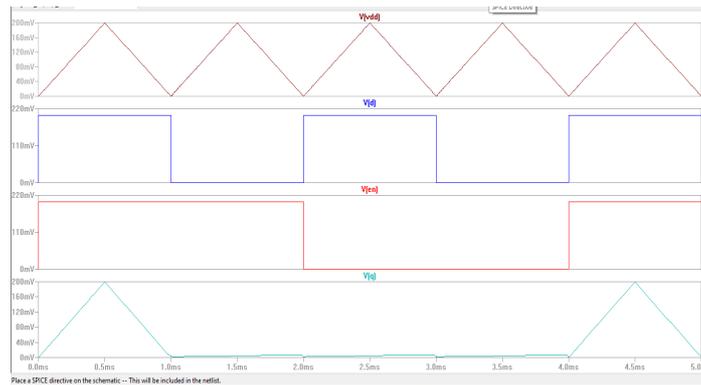
The first, second and third waveforms from top to bottom shows three input signals are vdd, enable and data. The fourth waveform shows output of the D-Flipflop.

International Journal of Innovative Research in Science, Engineering and Technology

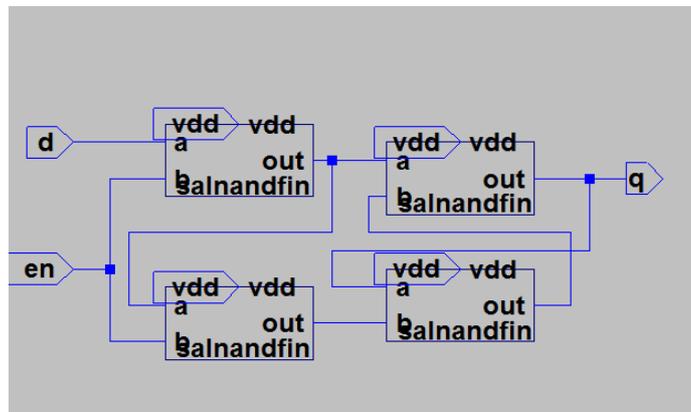
(A High Impact Factor, Monthly, Peer Reviewed Journal)

Visit: www.ijirset.com

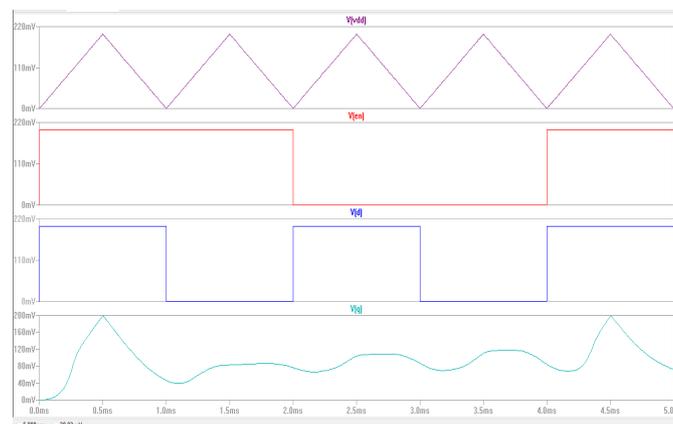
Vol. 8, Issue 2, February 2019



D-Flipflop with Fin-FET SAL is designed and simulated by LTspice 45nm technology. For supply voltage 200mv and operating frequency 1 kHz is analyzed.



The first, second and third waveforms from top to bottom shows three input signals are vdd, enable and data. The fourth waveform shows output of the D-Flipflop



International Journal of Innovative Research in Science, Engineering and Technology

(A High Impact Factor, Monthly, Peer Reviewed Journal)

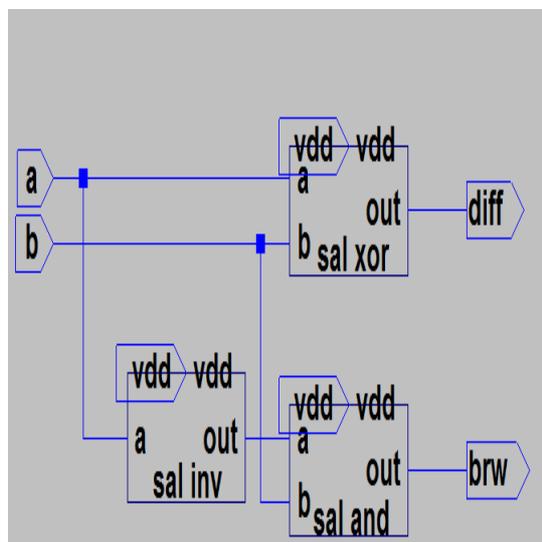
Visit: www.ijirset.com

Vol. 8, Issue 2, February 2019

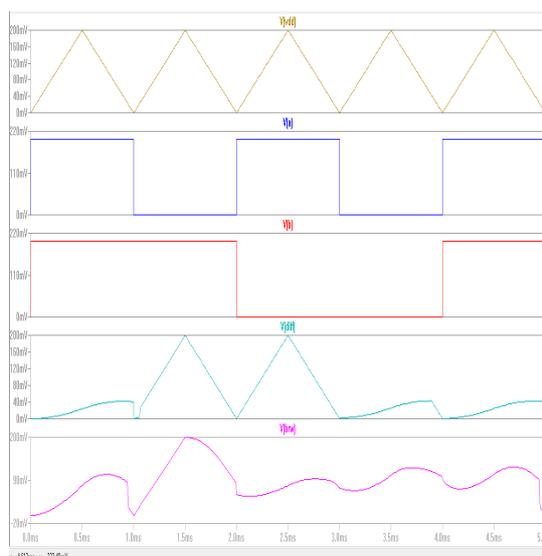
III. HALF SUBTRACTOR

Half subtractor has two input (A,B) signals and two output(difference, borrow) signals.

Half subtractor with CMOS SAL is designed and simulated by LTspice 45nm technology. For supply voltage 200mv and operating frequency 1 kHz is analyzed.



The first, second and third waveforms from top to bottom shows three input signals. The fourth waveform shows difference signal and fifth signal shows borrow signal.



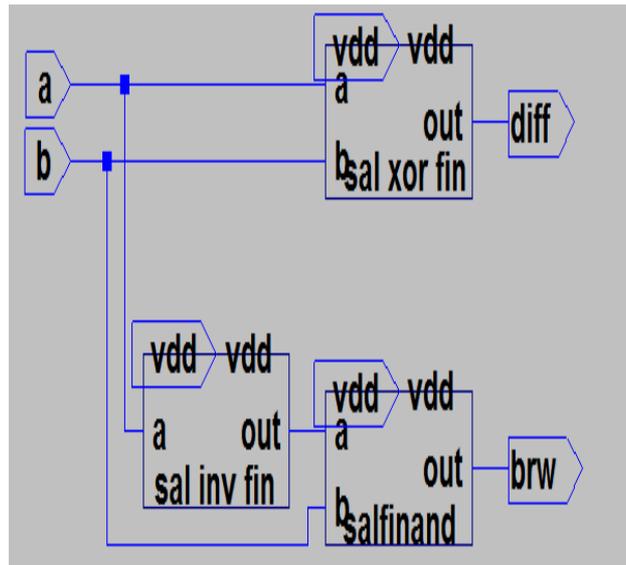
Half subtractor with Fin-FET SAL is designed and simulated by LTspice 45nm technology. For supply voltage 200mv and operating frequency 1 kHz is analyzed.

International Journal of Innovative Research in Science, Engineering and Technology

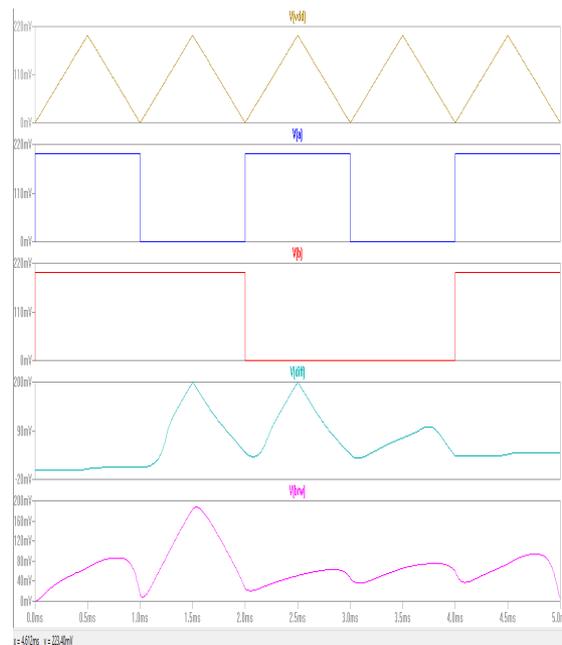
(A High Impact Factor, Monthly, Peer Reviewed Journal)

Visit: www.ijirset.com

Vol. 8, Issue 2, February 2019



The first, second and third waveforms from top to bottom shows three input signals. The fourth waveform shows difference signal and fifth signal shows borrow signal.



IV. 2-BIT BINARY MULTIPLIER

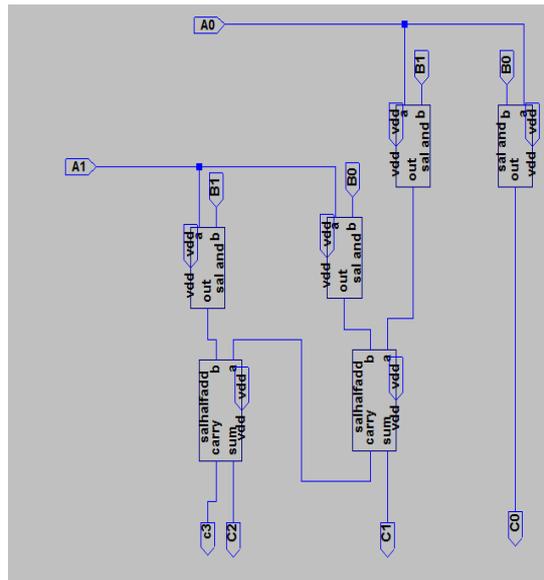
2-bit binary multiplier with CMOS SAL is designed by LTspice 45nm technology. For supply voltage 200mv and operating frequency 1 kHz is analyzed.

International Journal of Innovative Research in Science, Engineering and Technology

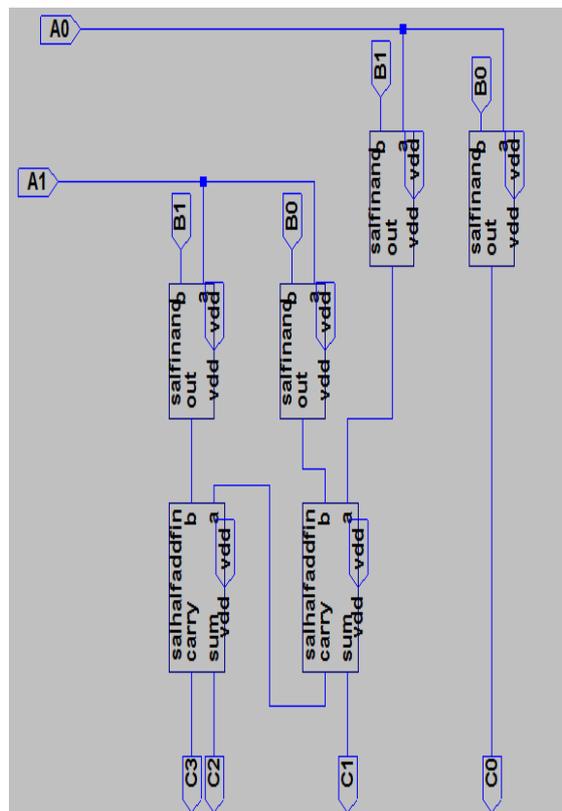
(A High Impact Factor, Monthly, Peer Reviewed Journal)

Visit: www.ijirset.com

Vol. 8, Issue 2, February 2019



2-bit binary multiplier with Fin-FET SAL is designed by LTspice 45nm technology. For supply voltage 200mv and operating frequency 1 kHz is analyzed.



International Journal of Innovative Research in Science, Engineering and Technology

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Visit: www.ijirset.com

Vol. 8, Issue 2, February 2019

V. POWER RELATION TABLE

The power relation table says Fin-FET SAL consumes less power compared to CMOS SAL.

| | Average power | | Peak power | |
|------------------------|---------------|------------|------------|------------|
| | CMOS | Fin FET | CMOS | Fin FET |
| Half adder | 4.0059E-13 | 7.6238E-14 | 3.1134E-12 | 5.0278E-12 |
| D-Flip flop | 1.8857E-12 | 4.2295E-15 | 5.9690E-11 | 1.9400E-13 |
| Half subtractor | 4.2450E-13 | 8.9776E-14 | 4.4887E-12 | 2.2739E-12 |
| Multiplier | 6.2352E-09 | 4.1772E-15 | 1.1534E-08 | 3.2296E-14 |

VII. CONCLUSION AND FUTURE PLAN

In this paper half adder, D-Flipflop, Half subtractor and 2-bit binary multiplier are designed using conventional CMOS SAL and Fin-FET SAL. From the above observations Fin-FET SAL consumes less power than CMOS SAL. Power dissipation is reduced in adiabatic circuit by recycling energy stored in capacitive load. SAL works at low frequency applications. Some variations occur in 2-bit binary multiplier circuit. In future correct the variations and to design 4-bit multiplier.

ACKNOWLEDGEMENT

Mr. T. Velmurugan,
Assistant Professor,
Department of ECE,
Builders Engineering College,
Tirupur.
N. Sunmathi,
UG Student,
Department of ECE,
Builders Engineering College,
Tirupur.
G. Sariga,
UG Student,
Department of ECE,
Builders Engineering College,
Tirupur.



ISSN(Online): 2319-8753
ISSN (Print): 2347-6710

International Journal of Innovative Research in Science, Engineering and Technology

(A High Impact Factor, Monthly, Peer Reviewed Journal)

Visit: www.ijirset.com

Vol. 8, Issue 2, February 2019

REFERENCES

1. P. Kalyani Ph. D Scholar, P. Satish Kumar Professor, P. Chandra Sekhar Associate Professor, "Design of Subthreshold Adiabatic Logic based Combinational and Sequential Circuits" Pune Institute of Computer Technology, Pune, India, 2017.
2. Manash Chanda, Sankalp Jain, Swapnadip, and Chandan Kumar Sarkar, "Implementation of Subthreshold Adiabatic Logic for Ultralow-Power Application" in IEEE trans. Very Large Scale Integrated(VLSI) Syst, vol.23, no.12, pp.2782-2790, 2015
3. Sakshi Goyal, Gurvinder Singh and Pushpinder Sharma, "Variation of Power Dissipation of Adiabatic CMOS and Conventional CMOS Digital Circuits", in International Conference on Electronics and Communication System, 2015
4. Rakesh Kumar Yadhav, Ashwani k.Rana, "Adiabatic Technique for Energy Efficient Logic Circuits Design", IEEE conf ICETECT(2011)